Service Manual

H 52382 - 900A
Vol. 2

Spectrum Analyzer
100 Hz - 400 MHz RF Unit
2382

Code No. 52382-900A

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Serial number prefix
-	June 86	152031

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Printed in the UK

Part No. 46881-490V
Print code : A - 6/86, 2c

CONTENTS

PRELIMINARIES

Title page
Contents
Notes and Cautions

CHAPTERS

1 General information
2 Installation
3 Operation
4-1 Brief technical description
4-2 Technical description
5 Maintenance
6 Replaceable parts
7 Servicing diagrams
8 Modifications and supplements

These chapters are contained in Vol. 1: Operating Manual

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment:

Symbol	Type of hazard	Reference
⚠	Static sensitive device	Page (iv)
⚠	Dangerous voltages present	Page (iii)
⚠	Supply voltage	Page (iii)

Note ...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ .... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers ⚠

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be allowed to discharge through the bleed resistors fitted for the purpose; do not attempt to remove the safety covers from the power supply until the lamp under the top cover stops blinking. Should the unit be reconnected to the supply with the safety covers removed then disconnected, do not attempt to discharge the power supply unit's main reservoir capacitors using a shorting link as the equipment may be damaged. Discharge should always be allowed to occur gradually.

Note also that the 12 kV e.h.t. circuit for the cathode ray tube retains its charge for a considerable time after switch off. Therefore before any handling is carried out in the vicinity of the cathode ray tube or e.h.t. unit it is essential that the supply is disconnected from the instrument and the final anode lead is shorted to the chassis several times immediately after unplugging. The residual charge on the c.r.t. itself must also be removed by shorting the anode connection to ground.

AC supply plug ⚠

The supply plug shall only be inserted in a socket outlet provided with a protective ground contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses - primary and secondary

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided. A number of secondary fuses are fitted to boards in the upper and lower units. For details of both primary and secondary fuses, refer to Performance data in the Operating Manual.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange disks, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disk or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with a grounded conductive surface.

Metallic tools grounded either permanently or by repeated discharges.

A low-voltage grounded soldering iron.

A grounded wrist strap and a conductive grounded seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

Cathode ray tube. When exposing or handling the tube take care to prevent implosion and possible scattering of glass fragments. Handling should only be carried out by experienced personnel and the use of a safety mask and gloves is recommended. A defective tube should be disposed of in a safe manner by an authorized waste contractor.

WARNING : TOXIC HAZARD

Many of the electronic components used in this instrument employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of IEC Directive 76/889 as to limits of r.f. interference.

Chapter 4-2

TECHNICAL DESCRIPTION

CONTENTS

Para.
1 Introduction
3 Circuit summary
3 Signal path, data conversion and tracking generator
10 Microprocessor and control
11 Synthesizer
20 Signal path
26 Unit AA1 - Input attenuator assembly &
Board AA1a - Input attenuator
30 Board AB8 - Overload detector
41 Unit AA2 - Input low-pass filter &
Board AA2a - Input filter & mixer
44 Unit AA3 - Band-pass filter &
Board AA3a - 502.6 MHz i.f. filter & 2nd mixer
45 Board AA9 - 2nd LO VCO
47 Board AA10 - Sampling gate
51 Board AC2 - 47.4 MHz i.f. amp
54 Board AC3 - 2.6 MHz LC filter
60 Board AC4 - 100 kHz i.f. xtal filter
64 Board AC5 - 2.6 MHz xtal filters
67 Data conversion
70 Board AD1 - log amp
79 Board AD2 - log amp interface
108 Synthesizer
115 Board AA4 - Sampling gate
120 Board AA5 - Master VCO
124 Board AA6 - Divider
125 Board AA7 - Slave VCO
129 Board AA8 - Master/slave phase detector
134 Board AB1 - D-A
145 Board AB2 - Interpolation oscillator
147 Board AB3 - Master VCO
151 Board AB4 - Sampling gate
153 Board AB5 - Slave VCO
156 Board AB6 - Phase detector
161 Board AB7 - Oscillator select
162 Board AC1 - 50 MHz xtal oscillator
164 Board AC6 - Phase detector
165 Board AD4 - 10 MHz calibrator
169 Microprocessor and control
172 Board AA11 - Line cleaner
174 Board AD3 - Microprocessor
195 Board AF1 - Front panel keyboard
197 Board AF2 - Front panel logic

CONTENTS (continued)

Para.
203 Board AR1 - Signal interface
207 Board AR2 - Power supply interface
215 Board AZ1 - Optical encoder
216 Board AZ2 - Span switch
217 Tracking generator (optional)
219 Board AE1 - 47.4 MHz xtal oscillator
221 Board AE2 - Buffer
222 Unit AE3 - Band-pass filter &
Board AE3a - Narrow band mix/buff
223 Board AE4 - TG buffer
224 Unit AE5 - Output low level filter &
Board AE5a - Wideband mix/buff
225 Board AE6 - Amp/leveller
235 Board AE7 - Switch

Table Page
1 RLA, RLB operation - AA1a 10
2 Trip logic - AB8 11
3 Attenuator settings - AD1 21
4 Trigger mode selector IC2 - AD2 24
5 4-input to binary conversion - AD2 26
6 Zero span sampling - AD2 29
7 Frequency sweep settings - AD2 37
8 Sweep integration - AB1 43
9 Detector operation - AB6 48
10 FET switch selection logic - AE6 69

Fig. Page
1 Block schematic of 2382 System 3
2 Block schematic of 2382 Synthesizer 4
3 Signal path block diagram 8
4 Data conversion block diagram 18
5 Conversion waveforms - AD2 25
6 Zero span operation summary - AD2 28
7 Synthesizer block diagram 35/36
8 Microprocessor and control block diagram 52
9 MARKER direction detector operation 59
10 Tracking generator block diagram 64
11 Sampling gate pulse generation waveforms - AE6 68

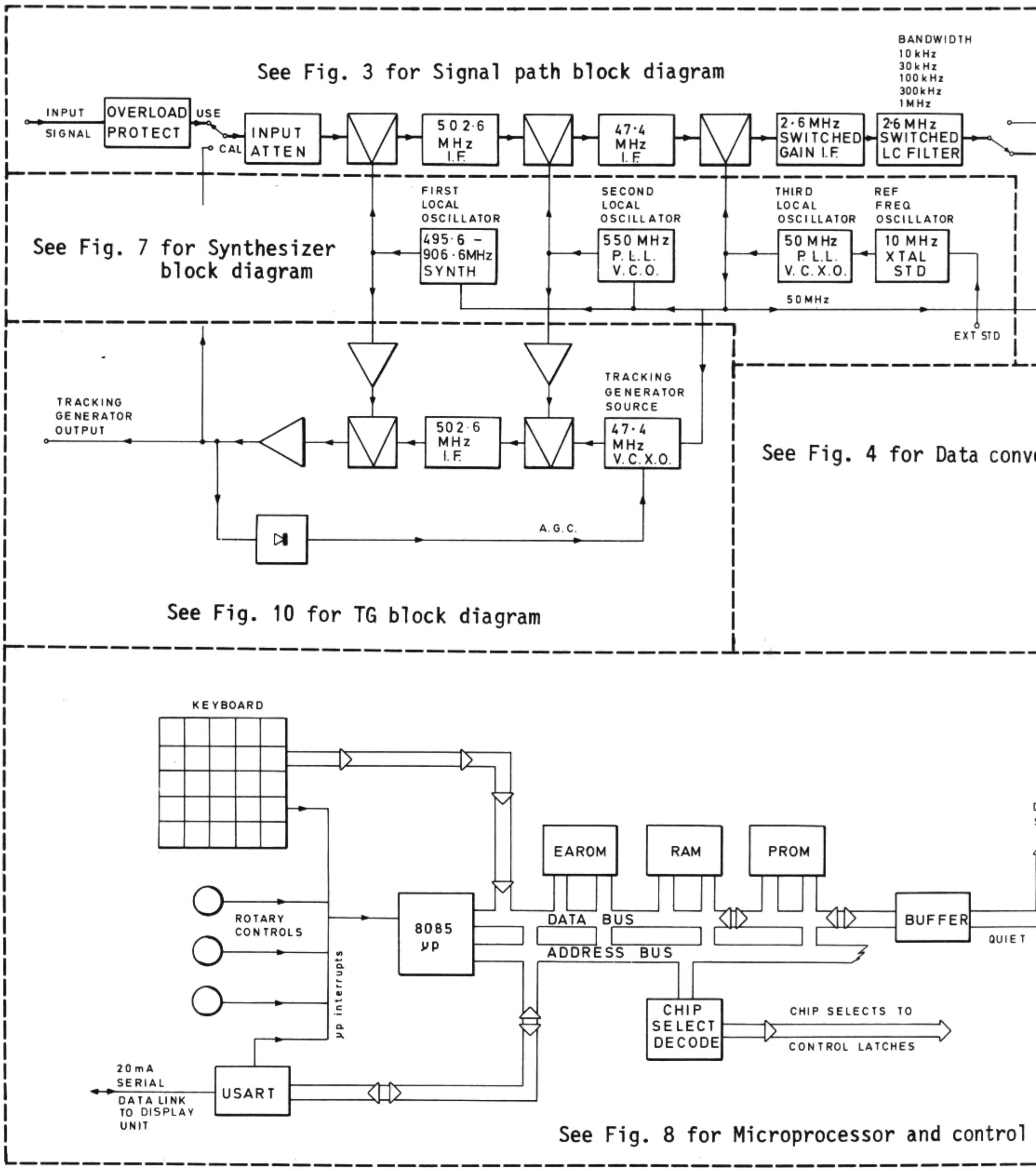

Fig. 1 Block schemat

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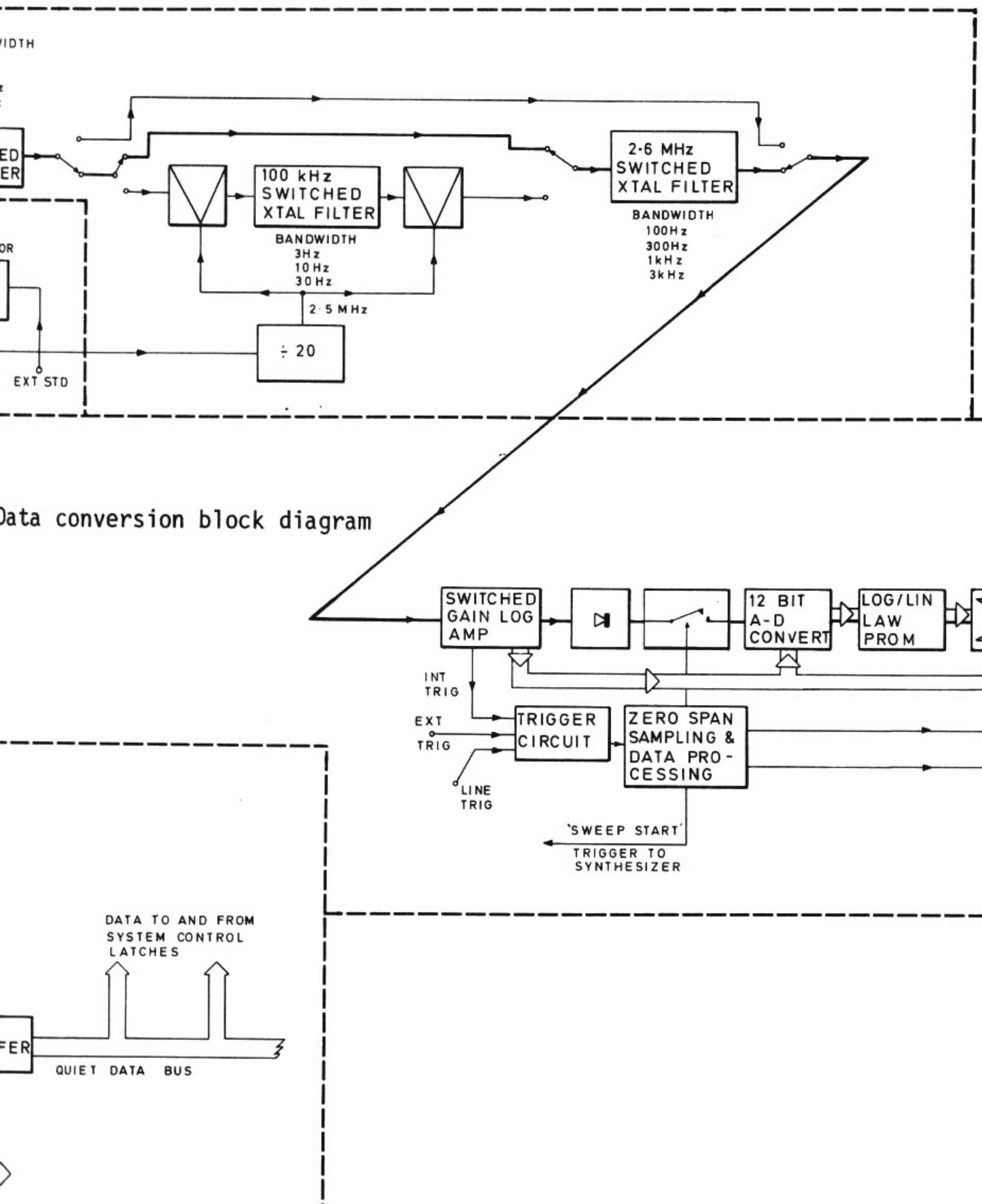

Data conversion block diagram

control block diagram

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k schematic of 2382 system

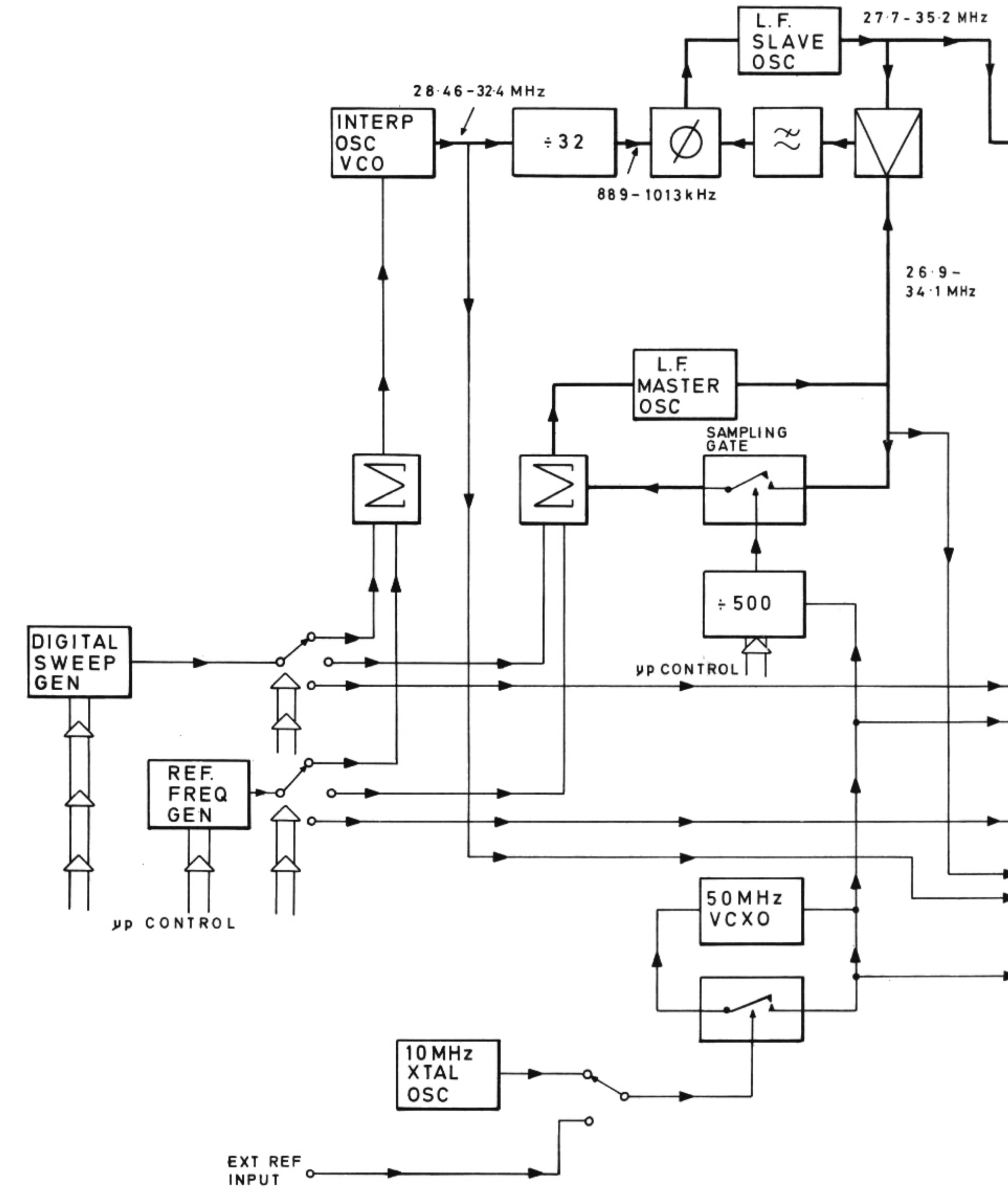
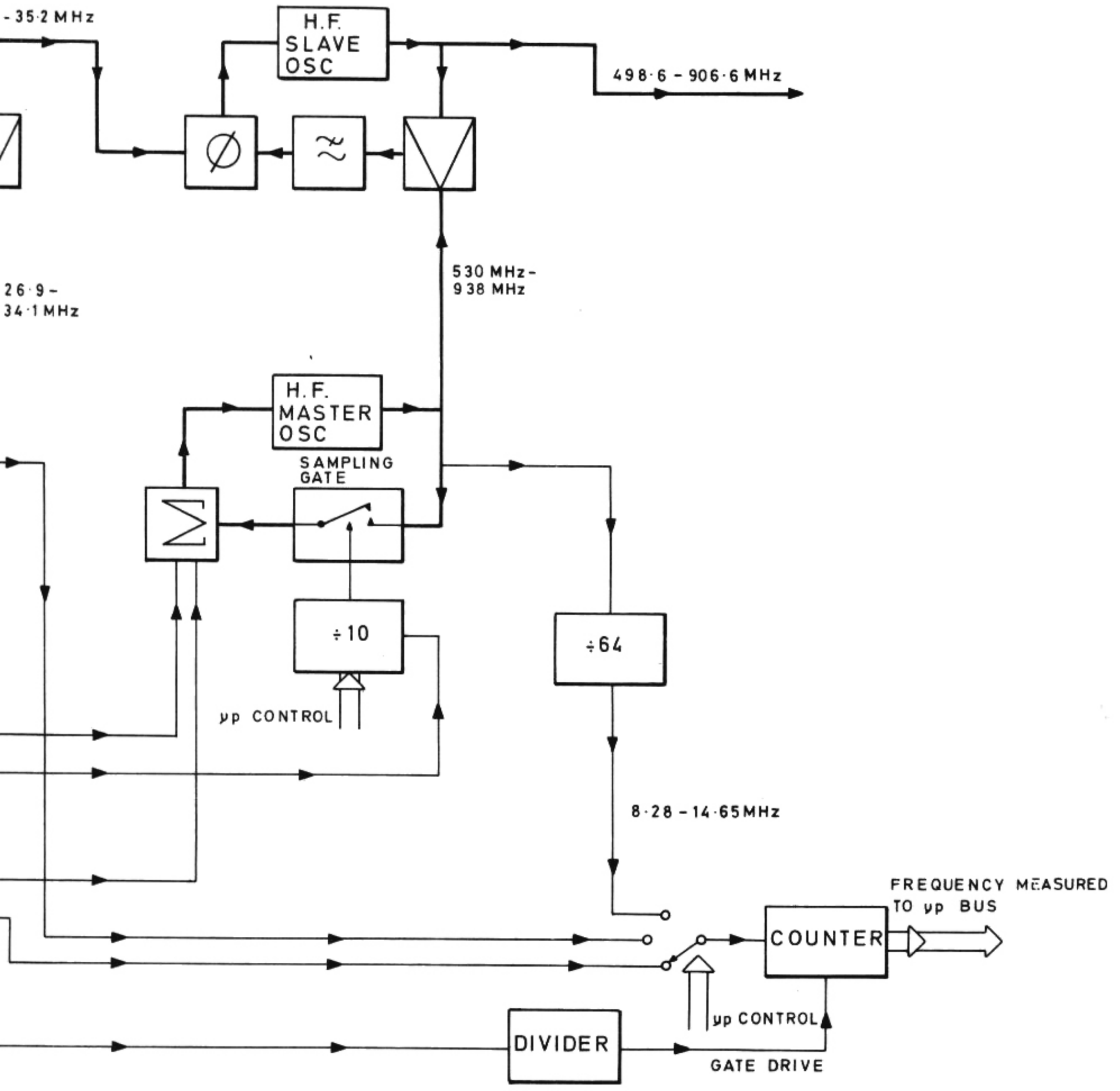


Fig. 2 Block schematic of 238



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tic of 2382 synthesizer

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INTRODUCTION

1. The following description should be read in conjunction with the appropriate diagrams in this chapter and with the circuit diagrams in Chap. 7. The circuits are summarized in paras. 3 to 19 and then described in detail in paras. 20 onwards.

2. The spectrum analyzer comprises one or more lower units containing the frequency synthesizer plus a common upper unit containing the display and power supply. Communication is via a two-way serial 9600 baud 20 mA current loop for house-keeping data whilst a one-way high speed serial link is used for the display data. The upper unit's power supply will power up to two lower units with only one selected at any one time. The lower units are internally wired to be self-addressing, therefore any configuration of units may be controlled via the front panel or remotely via a single GPIB socket as if it were a single instrument.

CIRCUIT SUMMARY

Signal path, data conversion and tracking generator

3. The 400 MHz RF Unit 2382 has an optional integral tracking generator and forms with display unit 2380 a swept filter spectrum analyzer covering the range 100 Hz to 400 MHz. A block schematic of the 2382 is shown in Fig. 1. With reference to this diagram, the signal to be measured enters via the overload protection circuit. This is a latched change-over relay which is tripped out by any signals over 1 W and protects for overloads of up to 50 W. An appropriate annotation is displayed on the screen that this has occurred, and the tripped condition remains until it is cleared by means of a front panel button.

4. The signal is then processed via a conventional up-down multi-stage superheterodyne configuration using a chain of phase coherent oscillators derived by phase locked loop synthesis techniques from the basic 10 MHz reference frequency oscillator. An additional phase coherent oscillator at 47.4 MHz provides the source signal for the tracking generator facility. This signal is frequency translated in a reverse, but otherwise identical, manner to the input signal by means of the second and first local oscillators.

5. The tracking generator signal is amplified by a broad band amplifier and amplitude levelled by an overall a.g.c. loop and is then available for use internally for system calibration via an internal change-over switch, or externally as the stimulus for passive or active frequency domain network analysis.

6. After frequency translation, the input signal is resolved by either a switched bandwidth LC filter, or a switched bandwidth crystal filter, both at 2.6 MHz, depending on the bandwidth required. Bandwidths of 30 Hz and below require the signal to undergo a further down-up frequency translation to 100 kHz to ensure that the filter shape will be sensibly independent of ambient temperature.

7. The translated, filtered input signal is applied to a switched gain logarithmic amplifier system. This switches in extremely accurate attenuator sections to keep the output signal within a 12.8 dB range for an input variation of 89.6 dB. The seven possible values of attenuation needed to achieve this form a 3-bit code to indicate the instantaneous status of this setting. The remaining 12.8 dB of output is detected and A-D converted to an

11-bit word which is processed by a linear-to-logarithmic law PROM and overlapped with the previously mentioned 3-bits of data to form a 13-bit word describing the instantaneous signal level to a resolution of 0.025 dB in a dynamic range of 102.4 dB. A linear data table in the PROM is selected when the 'Volts' display mode is in use.

8. The trigger circuit can select either an internal, external or supply frequency source. The output triggers the sweep start for both frequency and time displays. This facility is essential on the 'Zero Span' mode where the demodulated signal is displayed instead of the frequency spectrum.

9. Finally, the 13-bit word is parallel-to-serial converted and transmitted to the display unit via a single lead at a 2.5 MHz bit rate. A sync out signal is also fed to the upper unit to synchronize the upper unit serial-to-parallel converter.

Microprocessor and control

10. Front panel controls and the serial link to the upper unit are serviced via microprocessor interrupt procedures organized by a software Real Time Executive residing in the main program. All system switching, control and flag reads are done via a two-way buffer on the microprocessor bus. In this way, the bus wiring in the receiver area is free from the continuous data train of pulses on the normal microprocessor bus thus reducing the possibility of interference to the analogue circuits.

Synthesizer

11. This is a major sub-system of the 2382 Unit and comprises three master varactor controlled oscillators (see Fig. 2) whose outputs are offset one from the other by linking them via two slave varactor controlled oscillators in a phase locked loop configuration.

HF master oscillator

12. This covers the range 530 to 938 MHz and can be swept for spans of 5 MHz to 400 MHz, or locked at 5 MHz intervals anywhere over this band. Its output is divided by 64 to enable a counter to monitor its frequency.

LF master oscillator

13. This covers the range of 26 to 34 MHz and can be swept for spans of 50 kHz to 2 MHz or locked at 100 kHz intervals anywhere over this band. Its output is directly counted to monitor its frequency.

HF slave oscillator

14. This oscillator combines with two masters to form a phase locked combination that synthesizes an output frequency range of 498.6 to 906.6 MHz.

Interpolation oscillator

15. This is a very stable free running varactor oscillator covering the range 28.46 to 32.4 MHz. Before being used as the fine offset frequency in the total system, the output is divided by 32 giving an operational range of 110 kHz at an offset frequency of 950 kHz. This oscillator is swept for spans of 100 Hz to 20 kHz and can be set to a final resolution of 1 Hz anywhere over its 110 kHz of range. By counting its output frequency before

division, the divided output can be measured to 1 Hz in a counter gate time of 31.25 ms instead of the 1 second gate time required for direct measurement of the output.

LF slave oscillator

16. This oscillator is used to add the output of the interpolation oscillator into the other synthesized loop such that the overall system covers the range 498.6 to 906.6 MHz to a resolution of 1 Hz with sweep capability of 100 Hz to 400 MHz spans.

50 MHz VCXO

17. This is a high purity varactor controlled crystal oscillator used, after division, to drive the sampling gates which lock the l.f. and h.f. master oscillators to precise frequencies when they are not being swept. It, itself, is locked back to the 10 MHz reference frequency standard (either the internal one or the user's external one, if connected) by means of another sampled feedback loop. The 50 MHz oscillator is also used to provide the time base gate period for the counter.

Control voltages

18. The microprocessor system, in conjunction with variable ratio dividers, a digital-to-analogue converter and a tracking integrator, provide a non-linear ramp. This has a magnitude and shape that will produce a linear frequency sweep from the chosen oscillator over the span and reference frequency currently being used.

19. By means of a further microprocessor controlled A/D converter each of the three controlled oscillators is refreshed with its correct tuning voltage during each sweep retrace, the value being retained during the subsequent sweep.

SIGNAL PATH

20. The signal in the range 100 Hz to 400 MHz at the INPUT socket is connected to the input attenuators by the input selection switch on board AAla (see Fig. 3). When CAL is selected on the display unit, the processor selects the calibrator input in preference to the signal input. The processor then checks to see whether the tracking generator option is fitted, and if it is, the calibration sequence includes a check of the frequency response of the instrument since the calibration signal covers the full frequency range. If the tracking generator is not fitted, the processor selects the 10 MHz, -10 dBm input from board AD4.

21. The inputs are monitored by overload detector board AB8 and if an overload occurs, the input to the following attenuators is disconnected and INPUT OVERLOAD is signalled to the processor. The inputs are also disconnected by the processor, as part of the f.m. demodulation sequence, to calculate the required filter offset. For this purpose, DC MARKER ENHANCE is sent from AB8 to the first mixer on board AA2a. This injects a current into the mixer increasing the d.c. marker which is then used by the processor as a zero frequency reference.

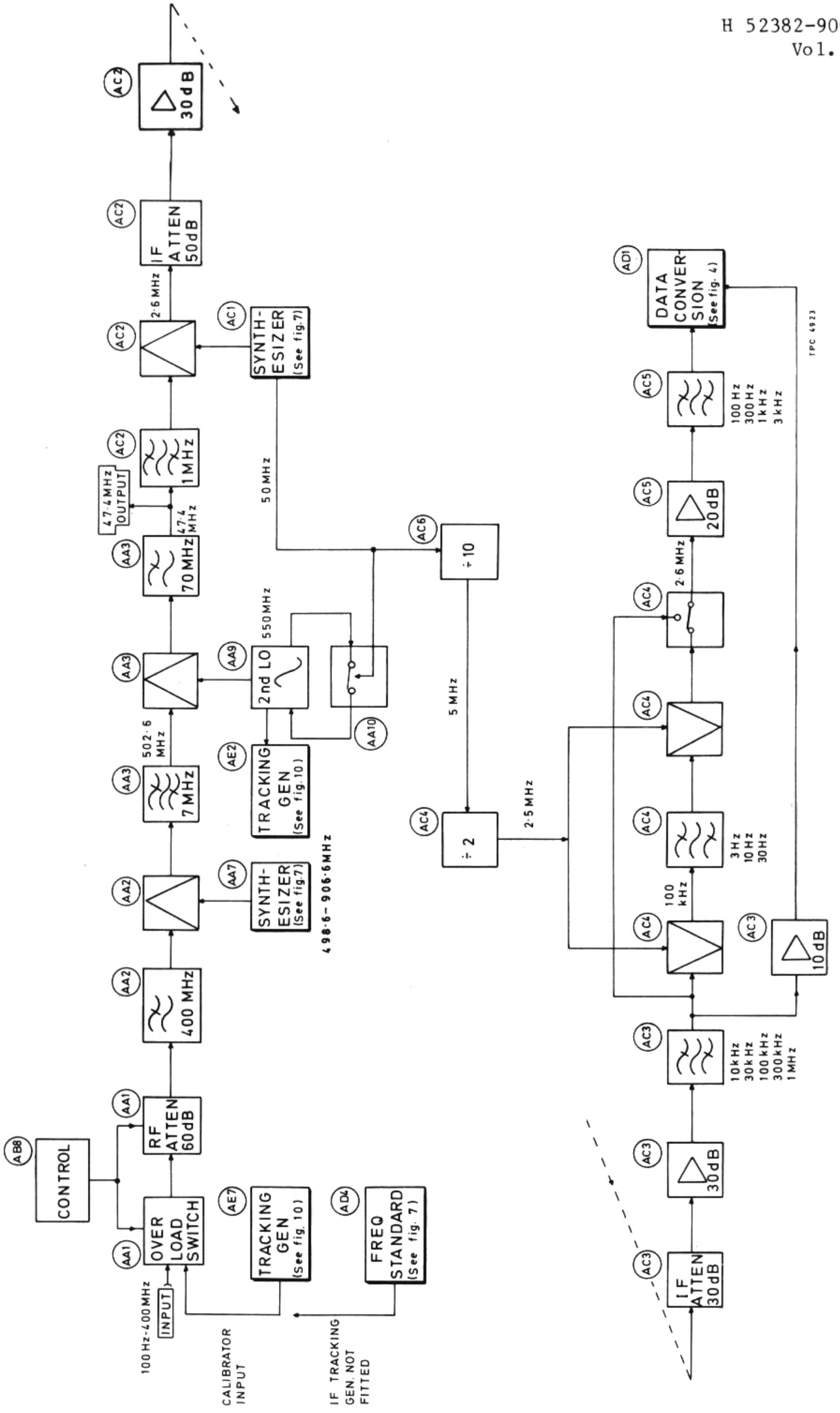


Fig. 3 Signal path block diagram showing main functions of boards

22. There are four input attenuators on AA1a. The first is a 3 dB attenuator used as a check for intermodulation products when INTMD IDENT is pressed, while the remaining three provide attenuation in the range 0 to 60 dB so that the input to the amplifier/mixer circuit can be kept below -20 dBm for any input signal.

23. The signal is next passed via 400 MHz low-pass filter AA2 to the input amplifier and first mixer on AA2a. Next, the r.f. input is mixed with a 498.6 to 906.6 MHz input from synthesizer board AA7. The difference frequency of 502.6 MHz is selected by the 7 MHz band-pass filter AA3 and fed to the second mixer on AA3a. Here the first i.f. is mixed with a 550 MHz input from the second local oscillator on board AA9. AA9 with AA10 phase locks the second l.o. with the third l.o. on board AC1. The AA3 70 MHz l.p. filter selects the 47.4 MHz difference frequency for output.

24. The 47.4 MHz second i.f. to AC2 is fed to the third mixer via an amplifier, a notch filter and a band-pass filter. An auxiliary output is tapped off and taken to the 47.4 MHz OUTPUT socket on the rear panel. The 50 MHz varactor controlled crystal oscillator on AC1 is normally locked to the fifth harmonic of the 10 MHz standard oscillator on AD4 by means of circuitry on AC6. If an external standard is in use, the sampling gate on AC6 produces an output that will cause the 50 MHz oscillator to lock on the appropriate harmonic. This 50 MHz signal is amplified and drives the l.o. port on the third mixer. The resulting 2.6 MHz difference frequency forms the third i.f. which is passed for level control to a three stage 50 dB attenuator and a 30 dB amplifier as well as to a further 30 dB attenuator and 30 dB amplifier on AC3. Together these control the i.f. gain in 10 dB steps from -20 to +60 dB.

25. Board AC3 contains 5 LC filters providing selected signal bandwidths of 10,30,100,300 and 1000 kHz. For the narrow bandwidths of 3,10 and 30 Hz board AC4 down-converts the 2.6 MHz i.f. to 100 kHz and, after feeding the signal through the required crystal bandwidth filter, up-converts it back to 2.6 MHz. The 2.5 MHz used by the mixer is derived from a divided 5 MHz from AC6. A filter bypass is provided for broader bandwidths. The 20 dB amplifier on AC5 is followed by 4 crystal filters which provide bandwidths of 100,300,1000 and 3000 Hz. For data conversion prior to display, a switch on AD1 selects the input from either AC3 or AC5 appropriate to the selected filter path.

Unit AA1 - Input attenuator assembly & Board AA1a - Input attenuator

Circuit diagram : Chap. 7, Fig. 4

26. This board contains the relays for the attenuators, for input selection and for the overload detector.

Input selection

27. Relays RLA and RLB select inputs in accordance with Table 1.

Overload detector

28. The INPUT socket is continually monitored by the overload protection circuit; via R2, R3 when RLA is energized and CAL is selected; via R4,R5 when RLB is energized and INPUT is selected. Detectors D1 to D4 which follow provide positive and negative outputs which are each compared for an overload with the thresholds set on AB8.

TABLE 1 RLA, RLB OPERATION - AA1a

State	Relay energized	
	RLA	RLB
Select INPUT		✓
Select CAL INPUT	✓	
Overload detected		
Zero mode	✓	✓

Input attenuators

29. Four 50 Ω pads provide 3,10,20 and 30 dB of attenuation. The 3 dB pad is switched in as a check for intermodulation products within the instrument. The remaining three are switched in to give 10 dB steps from 0 to 60 dB in the sequence :- 10,20,10+20,10+30,20+30,10+20+30.

Board AB8 - Overload detector

Circuit diagram : Chap. 7, Fig. 4.

Summary

30. This board provides three functions :-

a) Interfaces D/A board AB1 to the input attenuators on AA1.

b) Detects attenuator overloads i.e input signals above 1/2 W peak, and takes protective action.

c) In zero input mode provides a voltage which unbalances the first mixer on AA2 to ensure adequate d.c. marker amplitude.

Operation

31. The circuit functions in one of two states, normal or tripped. In the normal state, the attenuator solenoids are energized as specified by control signals received from AB1, a high signal causing the corresponding solenoid to be energized. To reduce power dissipation the solenoid drive voltage is normally less than the pull-in voltage. If a change in attenuator setting is required, the drive voltage is briefly increased. Such a change in setting is signalled by a falling edge on control line CHANGE.

32. If the solenoids of both RLA and RLB are energized (zero input mode) a voltage source of high output resistance is connected to the first mixer, otherwise this line, DC MARKER ENHANCE, is effectively open circuit.

33. In the tripped state, i.e. due to an overload being detected, the solenoids of RLA and RLB are de-energized regardless of their control signals. This state is entered when the instantaneous power input to the attenuator exceeds 27 dBm (provided that OVERLOAD CLEAR is not asserted). The circuit will return to the normal state when OVERLOAD CLEAR is asserted and no overload is detected. Thus OVERLOAD CLEAR is normally high, going low then high to return from tripped to normal state. On clearing, the solenoid drive voltage is briefly increased to pull in any solenoids which have dropped out on overload.

Overload threshold

34. ICs 2 and 3, forming part of the overload threshold circuit, are inverting and non-inverting Schmitt triggers respectively. Their input voltages are provided by IC1a and c which compensate for the effects of temperature on the AA1 overload protection diodes. Reference voltages for the Schmitts are derived from the -15 V line by R6, R7 and IC1b. Trigger levels correspond to ±5 V (27 dBm in 50 Ω) at the attenuator and hysteresis is about 3 dB for each trigger. R2 and R9 provide the 10 kΩ loads required by the detectors. The wired-OR output on pins 7 of ICs 2 and 3 goes t.t.l. low on the occurrence of an overload.

Trip logic

35. The gates of IC4 and half of IC5 form a two-state sequential logic network with two inputs, from the overload detector and the OVERLOAD CLEAR line, and two outputs, to the overload switches and the INPUT OVERLOAD line. The trip logic for this circuit is shown in sequence in Table 2. In the normal state (i.e. no overload detected), the output from the cross-coupled R-S latch at TP2 is high to enable the solenoid drivers to respond to input selection logic. A pulse on the OVERLOAD CLEAR line is sent at power-on to set the gates to their normal states. To select the signal at the INPUT socket, the microprocessor applies a high on the D5 line. This takes IC5 pin 11 low to comparator IC6c which switches on TR3 to energize the RLB solenoid.

TABLE 2 TRIP LOGIC - AB8

OPERATING SEQUENCE	IC4 pins					IC5 pins			
	1	9	10	11	13	1	2	5	6
Normal operation	H	L	H	L	H	L	H	H	H
Assert overload	L	H	H	H	L	L	L	H	L
Remove overload	H	L	H	H	H	L	H	H	L
Assert overload clear	H	L	L	L	H	H	H	L	H

Note : Ringed levels occur only during assertion of the operating signal

36. When an overload is detected, a low results from the overload comparator which sets the latch to take IC5 pin 6 low. IC5 pins 8 and 11 immediately go high which respectively cause TR2 or TR3 to switch off thus disconnecting the input. The high output from IC4 pin 11 is used to assert INPUT OVERLOAD to the processor which then displays the input overload message on the screen. With the input automatically disconnected by the overload protection circuit, the threshold comparator output now goes high so that when the overload is cleared, causing a negative pulse to be generated on line D7, the latch is reset. This reopens the gates to the input selection logic on lines D4 and D5 and the input is reconnected to the overload detector. If the overload has not been removed the protection process repeats.

Solenoid selective drivers

37. Comparators IC6 and IC7 which follow the trip logic circuit are used as level shifters to enable the relay solenoids to be controlled by t.t.l. via drivers TR2 to TR7. The 1.5 V threshold level Vb for all comparator inputs is derived from R18 and R19 connected between +5 V and ground. Signal input selection is provided by TR2 and TR3 while TR4 to TR7 select the input attenuators.

Solenoid pulser

38. Dual monostable IC8, comparator IC7d and switch TR1 form the solenoid pulser circuit. This connects the common solenoid line to -20 V for about 30 ms when either CHANGE or OVERLOAD CLEAR makes a high-low transition; otherwise this line is at -9.5 V. D3 prevents a short circuit when TR1 is on.

39. If the input level is within 6 dB of overload, spurious overload detection could occur on changing the attenuator setting because the moving switch contacts are temporarily open-circuit. This is prevented by gating the 30 ms pulse initiated by CHANGE onto the OVERLOAD CLEAR line, thus preventing overload tripping for this period.

Marker enhance

40. The d.c. marker enhance gate is formed by IC6a with diodes D4, D5 and D6. D4 and D5 form an AND-gate for the two low inputs when in zero input mode so that only in this mode is the DC MARKER ENHANCE line taken to 5 V at 10 kΩ; otherwise output is -20 V at >6 MΩ.

Unit AA2 - Input low-pass filter & Board AA2a - Input filter & mixer

Circuit diagram : Chap. 7, Fig. 5

Input amplifier

41. The input signal from attenuator board AA1a is fed through 400 MHz low-pass filter AA2 to the input amplifier on AA2a. Overload protection for the amplifier is provided by D1, D2 and R9. TR1 to TR3 form the amplifier which provides 8 dB gain from 100 Hz to 400 MHz to improve the overall noise performance of the analyzer. HF compensation for mixer and l.p. filter roll-off is provided by preset C12.

Mixer

42. Local oscillator input in the range 502.6 to 902.6 MHz from AA7 is connected to the first local oscillator driver. This is formed by TR5 to TR8 and provides +20 dBm drive for the mixer. Mixer X1 output feeds to 502.6 MHz signal buffer TR10 which recovers the mixer loss. Its high impedance output drives the following AA3 band-pass filter directly.

DC marker suppression & output

43. Based on D3, T1 this circuit uses feedforward to cancel the local oscillator leak in the vicinity of 502.6 MHz so that as the l.o. sweeps through this frequency the level seen on the screen is as low as possible. T1 normally gives 180o phase shift and since it is self-resonant at near 500 MHz it can be tuned, for one set of operating conditions, to cancel the leak. Similarly, R35 adjusts D3 to correctly set the level. When operating in the zero input mode, the DC MARKER ENHANCE signal from AB8 is used to disable this circuit. Output is via signal buffer TR10 which provides 12 dB of gain.

Unit AA3 - Band-pass filter & Board AA3a - 502.6 MHz i.f. filter & 2nd mixer

Circuit diagram : Chap. 7, Fig. 5

44. Band-pass filter AA3, which has a bandwidth of 7 MHz, selects the 502.6 MHz output from mixer board AA2a for passing to board AA3a. The signal supplies one input to dual-gate m.o.s. f.e.t. mixer TR1 whose other input is from second l.o. board AA9. Local oscillator input at 550 MHz is applied to the buffer formed by TR2 and TR3 and then to the mixer via driver TR4. Trimmer C8 allows the output matching network to be tuned for maximum gain at the resulting second i.f. of 47.4 MHz selected by the 70 MHz l.p. filter.

Board AA9 - 2nd LO VCO

45. This board contains the 550 MHz fixed oscillator with buffers and power splitters to provide gain and isolation for three 550 MHz outputs. The board also contains two voltage regulators.

46. The signal from AA10 on the V TUNE line feeds to varactor diodes D1,D2,D3 to control the frequency of the 550 MHz Clapp oscillator TR1. Frequency setting is by preset L3. Output from common emitter buffer TR2 is split by T1,T2; one output going via buffer TR9 to AE2, the other to one-transistor buffer TR3 and then into a second power splitter T3,T4. From here one output goes through a 3 dB pad to two-transistor buffer TR4,TR5 and out to AA3 at +5 dBm, while the other output goes through a 3 dB pad to a similar two-transistor buffer TR6,TR7 and out to AA10 at +5 dBm. The two-transistor buffers have approximately 60 dB of isolation and the one-transistor buffers have approximately 20 dB of isolation. This isolation is necessary to stop tracking generator and sampling gate harmonics from leaking into the receiver. To provide the oscillator with clean supply lines voltage regulators IC1,IC2 supply +10 V and -10 V respectively.

Board AA10 - Sampling gate

Circuit diagram : Chap. 7, Fig. 11

47. This board takes a 550 MHz signal from AA9 and a 50 MHz signal from AC1, mixes them in a sampling gate to provide an error signal, which is then fed back onto AA9 to phase lock the two signals.

Sampling gate

48. Buffer TR1 amplifies the 550 MHz signal from AA9 to give +10 dBm into the sampling gate. C8 reduces high order harmonics to prevent false locking of the loop. The 50 MHz input from AC1 to amplifier TR2 feeds to transformer T1 which provides the drive for the sampling gate mixer formed by D1 to D4. Step recovery diode D5 operates into a tuned circuit in order for the 11th harmonic (i.e. 550 MHz) to be selected to switch the sampling gate. R15 across D5 prevents double pulse generation. The mixer has a low mark/space ratio, the junctions of D1, D2 and D3, D4 being held positive and negative respectively with the diodes only being forward biased at the occurrence of the very narrow switching pulses. The sampled error signal, which has a bandwidth of approximately 2 MHz, is stored in C10.

Search oscillator

49. Voltage follower IC1 feeds the error signal via switched gain amplifier IC2c to the search oscillator IC2d. With the signal correctly phaselocked there is sufficient loop gain to suppress the search oscillator IC2d, but if an incorrect lock is obtained the loop gain will be insufficient and the Wien bridge oscillator IC2d, no longer suppressed, will produce a 14 Hz signal of 3.5 V p-p to move AA9 v.c.o. to the correct frequency. Final lock is achieved with the lead/lag filter.

Correct lock detector

50. IC2a and b form a window detector which ensures that the output voltage is within + or -1 V of 0 V, when the oscillator is locked to the correct 50 MHz tooth. If during switch on the oscillator locks to 500 MHz, the level at TP6 will be less than -1 V and the window detector will produce an output of 0 V at TP3, switching on TR4, so reducing the loop gain. This in turn starts the search oscillator and the AA9 frequency is swept until a correct phase lock is found.

Board AC2 - 47.4 MHz i.f. amp

Circuit diagram : Chap. 7, Fig. 21

51. This board mixes the 47.4 MHz second i.f. with 50 MHz from the crystal oscillator on AC1 to produce the 2.6 MHz third i.f. The 50 dB switched attenuators form part of the i.f. level control system.

Mixer

52. The 47.4 MHz input from AA3a is applied to 7 dB amplifier TR1 as well as to output buffer TR2 which supplies the rear panel 47.4 MHz OUTPUT socket. TR1 connects the signal to the mixer through a notch filter operating at the mixer image response of 52.6 MHz; the notch is tuned by C4 and the null depth is set by R21. The following 1 MHz band-pass filter consists of four coupled

resonators whose output is fed via TR5 to the sources of dual f.e.t. TR6. TR5 with TR7 and TR8 form a single balanced mixer. R29 at the emitter of TR5 provides compensation to prevent variation between f.e.t's affecting the intermodulation performance. Drive for the mixer is supplied by 50 MHz from AC1 via tuned buffer TR3 which supplies the antiphase switching signals to the gates of the mixer f.e.t's.

Level control

53. Output from the mixer passes into a three stage attenuator operating under processor control. Output from the mixer passes through unattenuated when high logic levels applied on the control lines to level shifters IC4b, IC4d and IC2a switch on f.e.t's IC1a, IC1c and IC3a respectively. Low logic levels on these lines are used to switch on f.e.t's IC1b, IC1d and IC3b which insert 20 dB, 10 dB and 20 dB of attenuation respectively. The i.f. level control of this board and of the 30 dB attenuator and amplifier on the following AC3 board enables the i.f. gain to be controlled in 10 dB steps from -20 to +60 dB.

Board AC3 - 2.6 MHz LC filter

Circuit diagrams : Chap. 7, Figs. 22 & 23

54. This board provides the 10 kHz, 30 kHz, 100 kHz, 300 kHz and 1 MHz resolution bandwidths at a centre frequency of 2.6 MHz. The filter is always in circuit regardless of overall resolution bandwidth, its output being routed to the log amp or other filters as required. The board also contains part of the i.f. variable gain system the remainder of which is on 47.4 MHz i.f. board AC2.

Attenuator and variable gain amp

55. The output signal at the 2.6 MHz third i.f. from AC2 is connected to the switched 0/30 dB attenuator formed by R1, R2 and switches IC1a,b. A high logic level from AD3 to drivers IC2a,b switches on IC1a to enable the signal to pass through unattenuated, a low switches on IC1b to route the signal via potential divider R1, R2 attenuating the signal by 30 dB.

56. The following 30 dB variable gain amplifier consists of feedback pair TR1, TR2 with gain control from pin diodes, D1, D2 in TR1 emitter. The diodes operate as current controlled resistors to the GAIN ADJUST input from AB1 and provide about 12 dB of control over the stage. Output to the following switched bandwidth filters is via buffer amplifier TR3, TR4.

Switched bandwidth filters

57. By driving the LC sections of the five filter stages from four switched impedances, bandwidths of 30 kHz, 100 kHz, 300 kHz and 1 MHz are produced. Control logic on the bandwidth select lines to drivers IC8a,b,c and d operate switches IC3,4,5,6 and 7 to route the input signal through the appropriate impedance. For the 10 kHz bandwidth all switches are open. For example, for the first switched BW filter, a low on the 30 kHz SELECT line to the inverting input of IC8a switches on IC3a and the input signal is routed through R35 in parallel with R34. Each LC filter includes a varactor diode connected to the CENTRE FREQ ADJ line to enable the processor to correct frequency drift, for bandwidths of 10 kHz and above, via a D-A converter on AB1.

Buffers

58. Each stage is buffered by a 'white emitter follower' which provides the very low output impedance necessary for wide i.f. bandwidths. Each stage uses a positive feedback circuit which makes the dynamic resistance of the LC section effectively infinite at resonance, so no insertion loss compensation is required when changing bandwidths. Thermistors in the feedback loop compensate for changes in inductor Q, and thus filter insertion loss, with temperature.

Output routeing

59. Output is connected to either log amp board AD1 or, if a bandwidth narrower than 10 kHz is required, to 100 kHz crystal filter board AC4. Connection is by quad switch IC9 driven from level shifter IC10. A low logic level from the microprocessor to IC10b inverting input switches on IC9b and c to select output to AD1, and switches on TR17 to enable centre frequency tuning. If this board is not controlling the overall i.f. bandwidth, TR17 is off and the filter's centre frequency is set by potential divider R147 and R148. When the LC filters are defining the bandwidth, the top of screen level is 10 dB lower than that required by the log amp. For this reason, output to AD1 is via 10 dB series feedback amplifier TR18.

Board AC4 - 100 kHz i.f. xtal filter

60. This board provides the 3,10 and 30 Hz bandwidths at a centre frequency of 2.6 MHz. The signal is mixed down to 100 kHz, amplified and passed through 5 crystal filter stages before being mixed back up to 2.6 MHz. Overall gain to signals at 2.6 MHz is +10 dB. A signal bypass route for the broader resolution bandwidths is provided.

Down mixer and switched gain amp

61. Signal input from AC3 at the third i.f. of 2.6 MHz is selected either for input to the mixer or to bypass the crystal filters. Selection is by logic from AD3 on the BYPASS CONTROL line to level shifters IC11a,b. For a low logic level, f.e.t's IC1c at the input and IC7c at the output switch on to route the signal past the filters as well as to inhibit mixer drive. For a high logic level, IC1d enables mixer operation and connects the bypass line to ground while IC7d selects output from the filters. Drive for the down mixer is derived from the 5 MHz input from AC6 applied via a 1 MHz high-pass filter. The signal is divided by IC2a and the resulting 2.5 MHz is applied to mixer f.e.t's IC1a and b. The difference frequency of 100 kHz is fed to switched gain amplifiers TR1,TR6 and TR7 which recovers mixer loss and is switched via IC3a and b to compensate for changes in filter insertion loss with changes in bandwidth. TR1 and TR6 form a series/shunt combination with feedback buffered by emitter follower TR7. Amplifier gain is varied by switching the emitter load of TR1 and this is accomplished using the same logic from AD3 on the BANDWIDTH lines that is used for filter selection. Gain for 30 Hz, 10 Hz and 3 Hz is set respectively by presets R17, R15 and R13.

Crystal filters

62. There are five crystal filter stages. The crystals are adjusted for centre frequency by the preset capacitors C23,43,63,83,103 and then trimmed by varactor diodes D1 to D5 under microprocessor control on the CENTRE FREQ ADJUST line from AD3. Each crystal is buffered by an emitter follower (TR7,9,13,15,19). The crystal parallel capacitance is nulled by the variable

gain inverting stage TR8,10,14,16,20 which feeds forward around the crystal. Stray capacitance on the crystal load resistor is tuned out by L2 to L6 and C32,52,72,92,112. The bandwidth of each stage is varied by resistors switched into circuit by open-collector t.t.l. gates. To ensure that the 'off' impedance of the gates is high, the load resistors are returned to +5 V and d.c. blocked by C30,50,70,90,110. In between stages 4 and 5, amplifier TR18 boosts the level to give the required overall 10 dB gain. Filter selection is by logic on the BANDWIDTH selection lines to gates IC3,4 and 5.

Up mixer and output

63. Filter output is taken via buffer TR21,TR22 to the up mixer. Mixer drive, supplied at 2.5 MHz from IC2b, is applied from isolators IC6 to switches IC7a and b. Mixer output reconverts the 100 kHz used for the bandwidth filters to the 2.6 MHz third i.f. Also at the output are f.e.t. switches IC7c and d. These enable the signal to bypass the filters when IC7c is switched on and IC7d is switched off.

Board AC5 - 2.6 MHz xtal filters

Circuit diagrams : Chap. 7, Figs. 26 & 27

64. This board provides the 100 Hz, 300 Hz, 1 kHz and 3 kHz resolution bandwidths at a centre frequency of 2.6 MHz by means of 5 crystal filter stages.

Switched gain amplifier

65. The input signal at the 2.6 MHz third i.f. from AC4 is connected to the 20 dB switched gain amplifier. This consists of TR1 and TR4 in a series/shunt feedback combination with feedback buffered by emitter follower TR5. Amplifier gain is varied by switching the emitter load of TR1 and this is accomplished using the same logic from AD3 on the SELECT lines that is used for filter selection. A low on either the 100 Hz or 300 Hz SELECT line switches on TR2 or TR3 respectively. Respective gain settings are by presets R7 and R11.

Crystal filters

66. There are five crystal filter stages. The crystals are adjusted for centre frequency by the preset capacitors C12,22,33,42,53 and then trimmed by varactor diodes D1,6,11,16,21 under microprocessor control on the CF ADJUST ENABLE line from AD3. This is taken low to switch on TR16 to enable the CENTRE FREQ ADJUST output from the D-A converter on AB1 to be used to optimize the filter tuning. Each crystal is buffered (TR5 to TR13). Stray capacitance on the crystal load resistor is tuned out by L2 to L6. Filter selection is by logic on the bandwidth SELECT lines to drivers IC1a,b and c which control diode switches D2-4,7-9,12-14,17-19,22-24. Output to AD1 is via buffer TR14,TR15.

DATA CONVERSION

67. The 2.6 MHz third i.f. from AC5 is selected at the required bandwidth at the input of AD1 (see Fig. 4). Here, an output is taken to AD2 to provide the video trigger used for display synchronizing purposes. The main path leads to paired attenuators and amplifiers. The attenuators are switched in or out of circuit as required to produce an analogue signal of 12.8 dB or less at the output. The attenuator settings necessary to produce this result

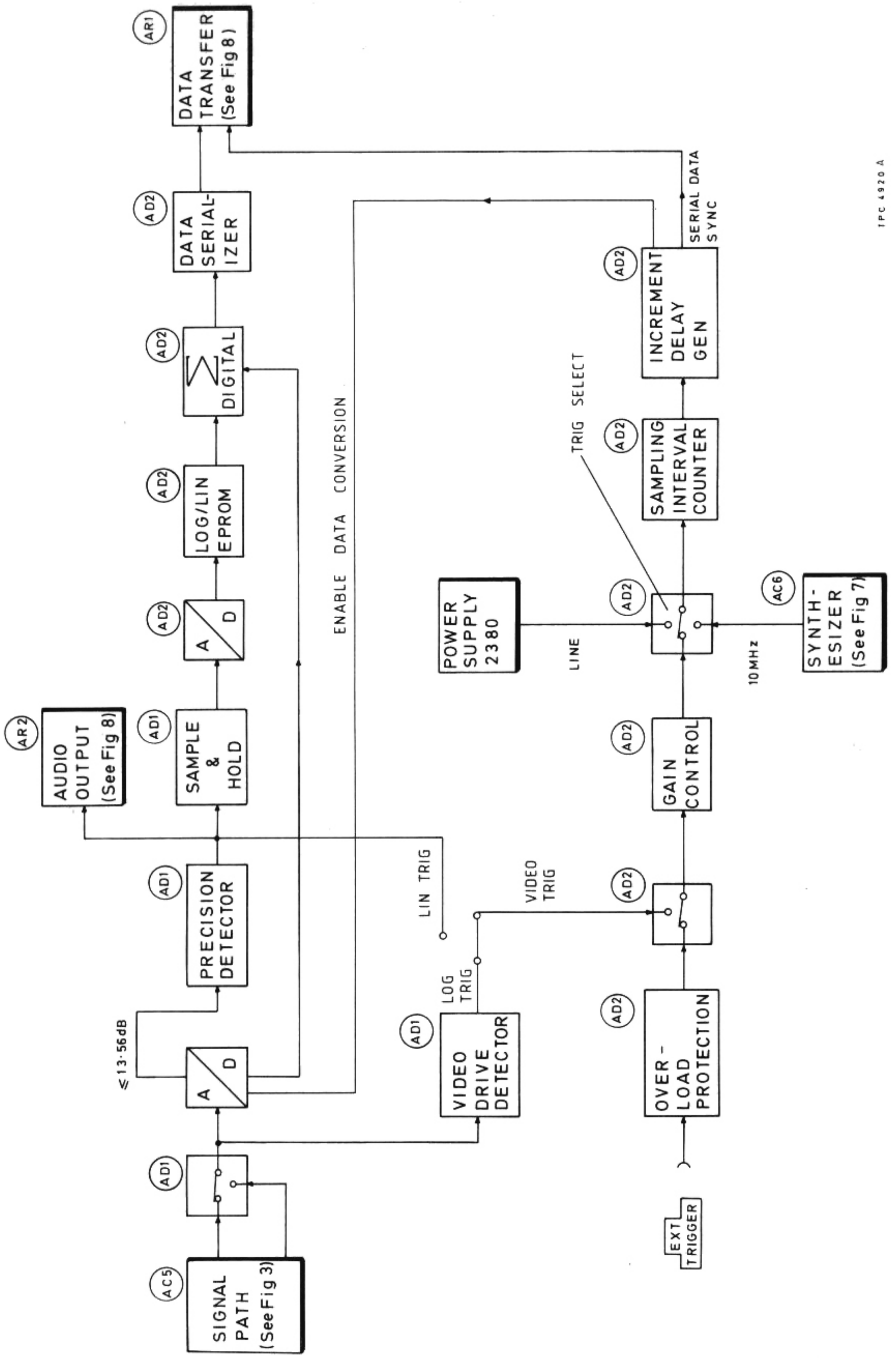


Fig. 4 Data conversion block diagram showing main functions of boards

provide a digital output capable of indicating 7 multiples of 12.8 dB. Total resolution, analogue and digital, is thus 102.4 dB. Additionally, a signal output, squared and at t.t.l. levels is supplied to AD2 for frequency measurement purposes. A precision detector connects the output to the audio amplifier on AR2 as well as to a sample and hold circuit for A/D conversion by AD2.

68. Board AD2 contains the A/D converter which changes the analogue input from AD1 to an 11-bit word. Depending upon mode of operation, this accesses the logarithmic or linear field of a look-up table held in EPROM. In the logarithmic case, the result is summed with the digital input from the AD1 attenuators. Additionally, when INTMD IDENT is pressed, the summer compensates for the 3 dB pad inserted on board AA1a. The parallel output from the summer is converted to a 23-bit data word which is serially clocked out for display by 2380.

69. The various display modes used in both frequency and time depend upon the occurrence of synchronizing pulses. These are produced from the external, video, line or 10 MHz trigger inputs. The synchronizing pulses cause the data for display to be sampled either at a constant rate or at intervals determined by the sampling interval counter and the incremental delay generator.

Board AD1 - log amp

Circuit diagrams : Chap. 7, Figs. 29 & 30

General

70. The logarithmic amplifier works by auto-ranging the input signal producing an analogue voltage output linearly proportional to the amplitude of the 2.6 MHz input signal over a 12.8 dB window, and a digital output which tells log amp interface AD2 into which of 8 such windows the signal fits. Thus the log amp is capable of reading an 8 x 12.8 dB dynamic range i.e. 102.4 dB. In the logarithmic mode the analogue output is converted to a log scale by a look-up table on AD2 to give a final resolution of 0.025 dB. For linear, voltage measurements, the logarithmic function is over-ridden and the amplifier stages are preset. For linear scales of 1 V, 2 V, 10 V etc., amplification is set to 25.6 dB while for scales of 5 V, 50 V etc., amplification is set to 13.56 dB. Auxiliary outputs are provided at the 2.6 MHz third i.f. for accurate frequency measurements on the user input signal, and at the detected output for audible-monitoring of the detected/demodulated output.

Input selection

71. Logic from AD3 on the BYPASS SELECT line to the level shifters forming IC1 controls the operation of f.e.t. switches TR2 and TR3. A low logic level switches on TR3 to select input from LC filter board AC3, a high switches on TR2 to select input from crystal filter board AC5. The selected input at the 2.6 MHz third i.f. is amplified by TR4, TR5 and buffered by TR6. An output from the emitter of TR4 to the precision trigger drive detector formed by TR39 to TR41 provides the LOG TRIG output to the AD2 board which is used for data transfer synchronizing purposes.

Overrange detectors

72. These detect the input level at each amplifier stage and switch each stage to 0 dB gain if the level exceeds -9.6 dBm, since this would correspond to an output level of +16 dBm from a stage with +25.6 dB gain. The first level detector consists of C9 with switch TR7 which operates as a fast response detector. Hold capacitor C9 is charged from TR7 and is discharged by the conduction of TR8 via D4. Thus the voltage on C9 applied to comparator IC3 is caused to track the input signal. The detectors have a very fast 'attack' speed but decay is slow, so it is necessary to reset them just before each conversion is made. This is carried out by TR8 for the 25.6 dB stages and by TR30 for the 12.8 dB stage. The reference for the non-inverting input of comparator IC3 is supplied by the potential divider R33, R34. IC3 output forms the data input for D-type latch IC4a. The remaining overrange detectors are similarly configured.

Attenuators and amplifiers

73. There are three switched 25.6 dB attenuators and one switched 12.8 dB attenuator, all of which operate in a similar manner. Transformer T1 and the associated resistors form the first resistive ratio attenuator which is controlled from latch IC4a by means of the four f.e.t. switches comprising IC2. Attenuation is by the high-precision divider R37 and R40 with adjustment provided by R39 - range of control is limited by R38. To select the attenuator, IC4a Q(L) output goes low to switch IC2d off and IC2b on. IC4a Q output is taken on the G1 OUT line to inform AD2 of attenuator selection.

74. Three 25.6 dB amplifiers and a switched 12.8/13.56 dB amplifier complement the attenuators. Each of the first three amplifying stages is configured similarly. The first stage comprises TR10 and TR11 which form a series/shunt feedback pair and have additional components C13, R52 in the feedback line to reduce the bandwidth and so aid noise suppression. Amplifier output is buffered by emitter follower TR12 to prevent loading effects on the following attenuator. TR13 is the level detector amplifier whose output is clamped by D10, D12 and buffered by TR14. The 12.8 dB amplifier consists of feedback pair TR33 and TR34 whose gain is switched by TR32 to provide an additional 0.76 dB when required.

Logarithmic operation

75. Log. amp. conversion period is 10 µs. Conversion starts with the 1 µs RESET 1-3 pulse which switches on TR8 to charge the first three hold capacitors. For the next µs the capacitors discharge (to their previous levels for a steady signal) after which the rising edge of the CLOCK 1-3 pulse clocks out the attenuator selection setting for the first three D-latches. The fourth stage has separate clock and reset lines since it finds its correct operating state later in the conversion cycle. The D-latch Q outputs indicating attenuator selection are fed out on the G1, G2, G3, G4 OUT lines to AD2 and then latched ready to be added to the logged output of the detector.

76. For a signal increasing in amplitude from zero, the fourth stage 12.8 dB attenuator is first activated followed by the third stage 25.6 dB attenuator. The fall in signal level due to the operation of the third stage attenuator is sensed by the fourth stage comparator and the 12.8 dB attenuator then switches out. Attenuation insertion continues in the sequence shown in Table 3 until at maximum signal level all the attenuators are inserted and up to 12.8 dB of signal is fed out to the sampling gate. To ensure that the attenuator selection sequence operates in reverse for a falling signal level, the first

and second latches' Q(L) outputs provide the set inputs for each succeeding stage. Thus an attenuator in one of the first three stages cannot be deactivated before that in the preceding stage.

TABLE 3 ATTENUATOR SETTINGS - AD1

	G1 (25.6)	G2 (25.6)	G3 (25.6)	G4 (12.8)	AMP (dB)
LOG					
	L	L	L	L	89.6
	L	L	L	H	76.8
	L	L	H	L	64.0
	L	L	H	H	51.2
	L	H	H	L	38.4
	L	H	H	H	25.6
	H	H	H	L	12.8
	H	H	H	H	0
LIN 1,2,10 etc.					
	L	H	H	H	25.6
LIN 5,50 etc.					
	H	H	H	L	13.56

Linear operation

77. For linear, voltage, measurements the clock inputs to the latches are overridden by the set and reset inputs. These preset the attenuation and amplification according to range. When settings of LIN 1,2,10,20 etc., are selected, reset is asserted which inserts all attenuators except the first thus providing an overall gain of 25.6 dB. When settings of LIN 5,50 etc., are selected, set is asserted which inserts all the 25.6 dB attenuators and switches out the 12.8 dB attenuator as well as switching on TR32 to increase the fourth stage amplifier gain. In this case, gain is set to 13.56 dB.

Output stages

78. To provide an output for frequency measurement purposes, the output signal is squared and shifted to t.t.l. levels by limiter IC13 and passed out on the IF COUNT OUTPUT line to AD2. The main signal path is to the mean level detector which is a precision rectifier type. It comprises high gain amplifier TR36 to TR38 with a full-wave diode rectifier D24,D25 in the feedback loop. The balanced output is fed through low-pass filters to remove the common mode r.f. signal and then via voltage followers IC14a and b to the

balance to unbalance amplifier IC15. Thermistor R206 compensates for temperature effects while offset and gain are adjusted by R202 and R207 respectively. Here an output is taken to AD2 to provide LIN TRIG. This signal is also routed from AD2 to AR2 to provide an audio signal. Sample and hold IC16 samples the output 2 µs after the occurrence of the CLOCK 4 pulse to allow time for the data to settle. IC16 operation is controlled by the SAMPLE/HOLD line from AD2 and the output is connected to this board by the SAMPLED DATA line.

Board AD2 - log amp interface

Circuit diagrams : Chap. 7, Figs. 31-34

General

79. This board and log amp board AD1 together form a system which converts the third i.f. analogue output of maximum 4 V pk-pk to a 13-bit data word. The board provides the synchronizing signals which enable the data to be displayed in either frequency or time in a number of ways. Frequency displays are the most often used and are selected when the FULL SPAN, /DIV or LOG buttons are pressed. Time display is selected when ZERO SPAN is pressed. Real zero span modes are only available on certain timebase ranges due to speed limitations in the data conversion process. To cover the faster timebase settings a sampling process is used. As well as being configured to enable the various display modes to be implemented, the board incorporates the trigger circuit essential for the sampling modes. The functions performed by this board are summarized as follows :-

(1) Trigger selection
(2) Data conversion
(3) Zero span display modes :
  a) Sampled
  b) Sampled with overlays
  c) Real
(4) Per div sweeps

Each of these functions is explained in turn.

Trigger selection

80. User-selectable trigger sources are line (supply frequency), video or external. Auto triggering is also available so that in the absence of any of the above triggers the circuit will default to a 10 MHz trigger. Positive and negative edge triggering is also available as a shift function on the front panel. The video trigger is a detected signal from log amp AD1. The signal is obtained from either LOG TRIG at AD1's input or LIN TRIG at AD1's output. The maximum frequency of this signal, limited by the i.f. bandwidth, is around 300 kHz, while loop time constants limit the lowest frequency to about 10 Hz. These frequency limits are extended by large amplitude signals. Since the external signal follows the same path as the video signal it has the same frequency constraints. Amplitude of mid-band triggering is 40 mV pk-pk and allows triggering to any signal which is 20 dB from the top of the screen.

81. Microprocessor controlled latch IC24 latches out trigger mode selection data from the quiet data bus on the occurrence of a rising edge on chip select line CS50. When either of the two LOG/LIN latch outputs is taken low by the processor, IC1a selects the LOG TRIG input, otherwise the LIN TRIG input is selected. LIN TRIG also provides the AUDIO signal to the rear panel volume

control. The selected input, in the range 10 Hz to 300 kHz, provides the VIDEO TRIG input to a second selector. When latch IC24 takes VIDEO or EXT low, either the VIDEO TRIG or the EXT TRIG input is respectively selected. For the latter input, overload protection is supplied by clamping diodes D1,D6 and D2, D8 on the gate of source follower TR1.

82. The selected signal is a.c. coupled to input amplifier IC4a and fed in parallel to a Schmitt trigger and to a centring amplifier. The variable hysteresis Schmitt trigger consists of Schmitt IC5 and amplifiers IC4c and IC4d which respectively supply IC5 with positive and negative power. References for the amplifiers are set by the sum of the voltages from potential dividers and peak detectors D3 and D4. The dividers ensure that for no signal input the amplifiers supply ±3 V in order to maintain IC5 operation. Since IC5 has positive feedback, its output switches between the positive and negative levels of the supplied power. IC4 and IC5 thus enable the Schmitt window to be controlled so as to be small for low level signals and as large as possible for high level signals.

83. The signal path to IC5 is via centring amplifier IC4b. Its purpose is to convert an asymmetrical input to a symmetrical output suitable for triggering purposes. This is needed because of the effect of a.c. coupling on non-unity mark/space ratio signals. To do this, half the sum of the voltages from the peak detectors is applied to the non-inverting input of differential amplifier IC4b, while the incoming signal is applied to the inverting input. Thus for an input on pin 6 varying between +5 V and -2 V, +1.5 V is applied to pin 5 and the output varies by ±3.5 V. IC5 output is converted to t.t.l. by driver TR2 before being applied as one of the three trigger signals to selector IC2. D5 protects against reverse bias breakdown.

84. Triggering detector IC6 is a retriggerable monostable which detects when the VIDEO or EXT TRIG signal has failed. Its pulse duration is set by R37, C64 so that providing the triggering rate does not fall below 10 Hz its pin 8 is held continuously high to pin 2 of trigger selector IC2. In this condition, IC2 allows trigger selection in the normal way (which also applies if AUTO is unasserted high to pin 2). But if the triggering signal fails and AUTO has been selected, IC2 pin 2 is taken low. Trigger selection then defaults to the 10 MHz input in order to maintain the trace.

85. IC2 is a dual 4 line to 1 line multiplexer configured to select 2 out of 3 trigger sources. The sources are; VIDEO TRIG/EXT TRIG from TR2, LINE TRIGGER from AR1 (both signals are available normal or inverted) and 10 MHz derived from the 50 MHz crystal oscillator on AC1. IC2 is controlled by latch IC24 using the AUTO and +ve lines to select two outputs (see Table 4). One of the two is then chosen by quad NAND gate IC3 to supply the TRIG signal used for data synchronizing. IC24 also controls IC3 so that when, for example, LINE is asserted low the supply frequency supplies the TRIG.

Data conversion

86. Data conversion involves both AD1 which supplies the level data in analogue and digital form and this board which provides overall control of AD1 operation, data conversion and the display mode. AD1 performs as a very accurate 4-stage switched gain amplifier supplying an analogue input of up to 12.8 dB and a 4-bit word giving the amount of inserted attenuation (and hence of amplification) as three amounts of 25.6 dB and one of 12.8 dB. A/D conversion of the analogue input to AD2 provides an 11-bit word which is then used to address a memory array held in two EPROMs. Here the data is split into two fields, one log and one linear. In the log case where the output

code is logarithmic, it is added without error to the 4-bit word representing the four gain blocks. In the linear case AD1 gain is preset and therefore is not added. With all input data now in a digital form it undergoes parallel to serial conversion before being synchronously clocked out to the upper unit.

TABLE 4 TRIGGER MODE SELECTOR IC2 - AD2

Selection Logic		Input Selected	Outputs	
A	B		1Y	2Y
L	L	C0	10 MHz	LINE
H	L	C1	10 MHz	$\overline{\text{LINE}}$
L	H	C2	VIDEO/EXT	LINE
H	H	C3	$\overline{\text{VIDEO/EXT}}$	$\overline{\text{LINE}}$

87. An analogue signal present at the input of log amp AD1 will after 3 conversions, each taking 10 µs, appear in the input of the display unit. The three stages are as follows :-

a) Set up AD1 switched gain amplifier
b) Convert last 12.8 dB of analogue signal to an 11-bit word.
c) Serially clock out 23-bits of data at 2.5 MHz.

All three stages of conversion rely upon sequence generator IC9 which is a 10-line decoder whose outputs are taken low in sequence for 1 µs. All three stages of data conversion run simultaneously.

Setting up AD1 switched gain amplifier

88. The sequence of operations performed by AD1 (detailed under the board heading) is controlled by the sequence of 10 pulses generated by IC9 on AD2 (see Fig. 5). When pulse 1 is generated, the three 25.6 dB detectors are reset following which pulse 2 autoranges the first three amplifiers and the attenuator settings are sent to AD2 on the G1 to G3 lines. Pulse 3 supplies a 1 µs delay to let the amplifier outputs settle and then pulse 4 resets the 12.8 dB detector. Pulse 5 sets the gain of the final amplifier and the attenuator setting is sent on the G4 line, after which pulses 6,7,8 and 9 provide a further 4 µs settling time. Pulses 10 and 1 hold the SAMPLE/HOLD line low giving the analogue output 2 µs in which to charge the hold capacitor. On AD2, the 4-bit word on lines G1 to G4 is converted to 3-bit binary by quad NAND gate IC16 (see Truth Table 5) and applied to bistable latch IC17. At this time the analogue input is connected on the SAMPLED DATA line to 12-bit A/D converter IC12.

A/D conversion

89. When IC9 pin 1 goes low it produces the SEQUENCE START pulse which performs several functions. It is taken via IC56a to provide the second half of the 2 µs SAMPLE/HOLD signal in order to continue the AD1 analogue sampling process. It is inverted by IC51a and used to enable latch IC17 to accept the AD1 attenuator setting data, and provides the CONVERSION START pulse for A/D converter IC12. When pulse 1 returns high it latches out the IC17 3-bit word while the analogue signal, held on AD1, is asynchronously converted to an 11-bit word by IC12 for the next 6 µs.

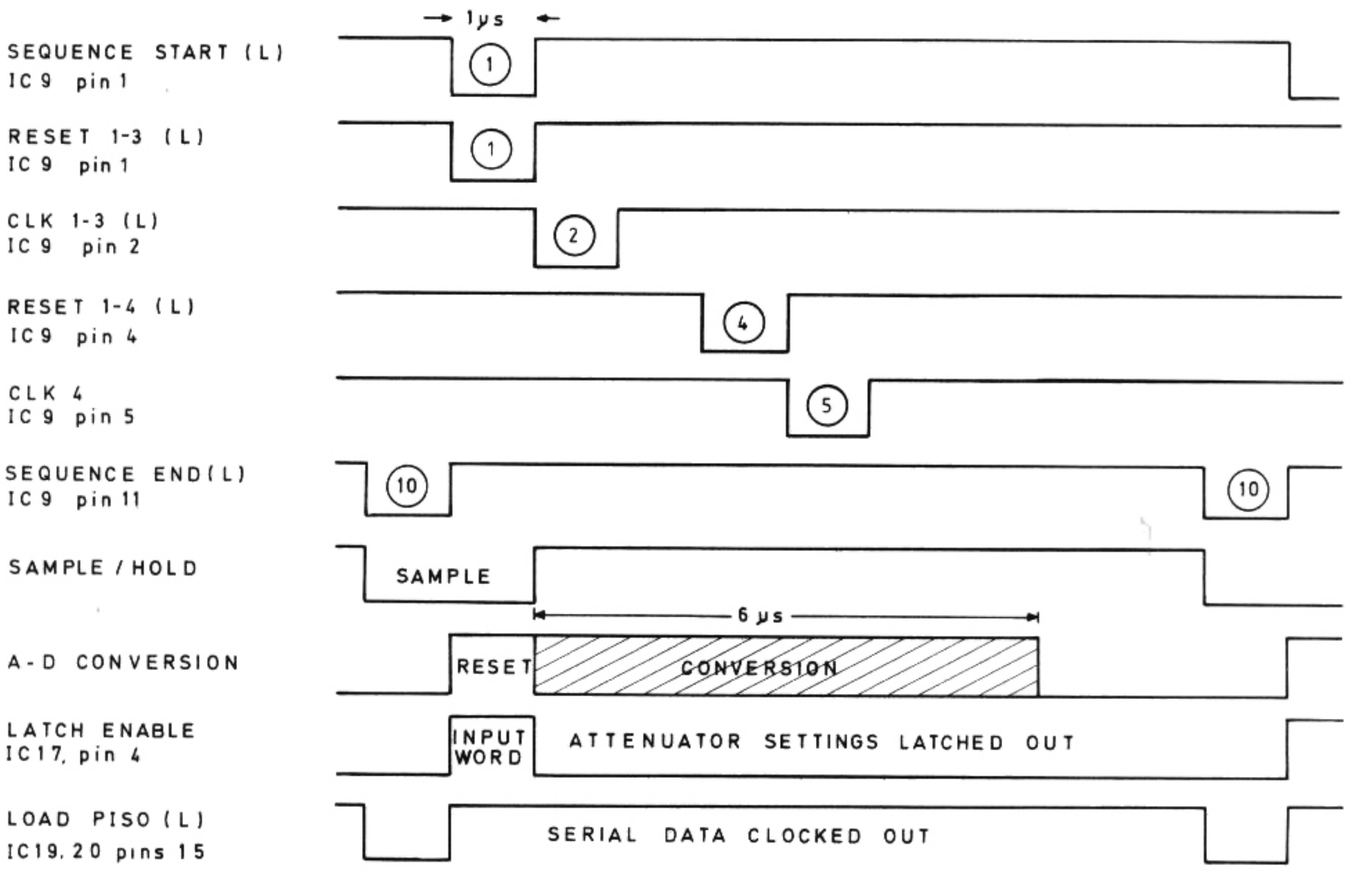


Fig. 5 Conversion waveforms - AD2

90. The purpose of IC8a is to detect an analogue overload condition occurring when SAMPLED DATA exceeds 5 V. When this occurs, the 12 output bits from A-D IC12 change from 0111 1111 1111 to 1000 0000 0000. But since bit 1 is ignored and only 11 bits are passed on to provide data for the display, the system reads a transition from all '1's to all '0's. The top of screen analogue value is 4 V and when the above transition occurs, unless corrective action is taken, the display top edge would appear to drop by the equivalent of 4 V. To

prevent this, the 5 V overload is detected by IC8a so as to cause bits 2 to 11 to be clamped at all '1's. IC8a does this by its data input on pin 2, provided by the A-D bit 1 output, being clocked out on the rising edge of the inverted SEQUENCE END pulse. IC12 pin 21 is then taken high to start conversion upon which the internal approximation register takes all the output bits initially high. Since the conversion process, initiated by SEQUENCE END, has occurred 1 µs earlier than normal - during the period reserved for data conversion - bits 2 to 11, now all high are accepted as the corrected output for the display.

TABLE 5 4-INPUT TO BINARY CONVERSION - AD2

Input lines				IC16 pins				IC17 pins		
G1	G2	G3	G4	8	11	6	3	6	3	2
L	L	L	L	H	H	H	L	L	L	L
L	L	L	H	H	H	H	L	L	L	H
L	L	H	L	H	L	H	H	L	H	L
L	L	H	H	H	L	H	H	L	H	H
L	H	H	L	L	H	H	L	H	L	L
L	H	H	H	L	H	H	L	H	L	H
H	H	H	L	L	H	L	H	H	H	L
H	H	H	H	L	H	L	H	H	H	H

91. At the end of the A/D conversion period, the resulting 11-bit word is used as an address to access two locations in the 20 dB range log law/linear look-up table held in EPROMs IC14 and IC15. Which of the two locations provides the output is determined by the logic level of the LOG/LIN line. For log operation LOG/LIN is held high, and when the SEQUENCE END pulse is generated the EPROMs output their data in logarithmic form. The high LOG/LIN signal also opens gates IC23 to allow the attenuator selection logic data to be summed with that from the EPROMs in the digital summer formed by IC18, IC21 and IC22. For linear operation the LOG/LIN line is low which causes the EPROMs to output their data in linear form and also closes gates IC23 since the attenuators are preset for this mode (see AD1) and the data is not required. An additional input to the summer is from the IP IDENT line which compensates for the loss in level caused by the 3 dB inserted in the r.f. path when checking for intermodulation products. The data is applied from the summer to two 8-bit shift registers IC19 and IC20 which are parallel in, serial out (PISO) registers. These load the data when pins 15 are taken low by the SEQUENCE END pulse.

Serial output data

92. The low SEQUENCE END pulse which caused the data to be loaded into the PISOs is also used to reset IC13b. This IC has its Q(L) output connected to its D input so that it divides the 5 MHz output from IC11 by 2 to supply the 2.5 MHz clock for the PISOs. The clock stops for 800 ns until the next 1 MHz clock pulse from IC11 removes the IC13b reset. When the 2.5 MHz clock restarts, it is synchronized to the 800 ns pulse providing the SERIAL DATA SYNC signal, and the 23-bit word representing the detected third i.f. is clocked out from the PISOs to the display unit on the SERIAL DATA OUT line.

Zero span

93. In zero span, the horizontal axis of the display is graduated in time instead of frequency, and produces an oscilloscope-type display rather than the usual spectral lines. The maximum i.f. bandwidth of 1 MHz determines the maximum resolvable modulation frequency resulting in a fastest timebase setting of 5 µs/div. Relating this to the 500 vertical lines (ordinates) of resolution on the display means that minimum ordinate separation is 100 ns. This however, cannot be used for the display of real time signals since the fastest conversion rate in zero span mode is limited by the display unit input board to 200 µs/ordinate. Thus only for sweeps of 10 ms/div (1 division = 50 ordinates i.e. one tenth of the screen) or greater, can real time analysis take place. For faster sweeps a sampling technique is used which itself has two modes of operation, sampled and sampled with overlays. These modes are distinguished by the number of ordinates per trigger that are transmitted to the display. In sampled mode, one ordinate per trigger is transmitted. In sampled with overlays mode, between 5 and 250 ordinates per trigger are transmitted resulting in the picture being updated in bands rather than sequentially as in sampled mode. Zero span modes with associated timebases are as follows :-

ZERO SPAN MODE	TIME BASE/DIV RANGE
Sampled	5 µs - 50 µs
Sampled with overlays	100 µs - 5 ms
Real	10 ms - 20 s

Zero span operation is summarized in Fig. 6 while the parameters for each of the 3 modes are given in Table 6.

Sampled zero span

94. The principle behind this mode is that the modulation being viewed is periodic and that an accurate trigger pulse is generated to predetermine a fixed point on the waveform. Just as in sampling oscilloscope technology, this mode uses the trigger to send the first sample of data and then retriggers a short time later but adds a delay before sending the second sample of data. The delay is equal to one ordinate on the screen (i.e. 1/50th of the timebase). This delay increases by one ordinate period per trigger until 503 delays have accumulated beyond the trigger point. It is now that the display store is full and the whole sequence can be repeated.

Sampled zero span with overlays

95. In this mode, the display unit is configured to accept from the r.f. unit both real and sampled signals occurring in an interleaved fashion. Due to this, two data samples transmitted sequentially between units will not appear adjacently on the display. As an example, it might be required to display one cycle of a 1 kHz sinewave. Since its period is 1 ms and there are 10 divisions a time base of 100 µs/div is selected. And since the fastest conversion rate is 200 µs/ordinate, after the trigger point 5 samples of data are allowed to transfer between units before another trigger is requested Sample 1 is transferred to ordinate 1 but samples 2,3,4 and 5 are transferred to ordinates 101,201,301 and 401 respectively. In order to fill in the gaps between these samples a delay of 1 ordinate is introduced and samples 6,7,8,9 and 10 are transferred to ordinates 2,102,202,302 and 402. This process occurs 100 times to form a fully overlayed display produced by 100 triggers with 5 samples per trigger.

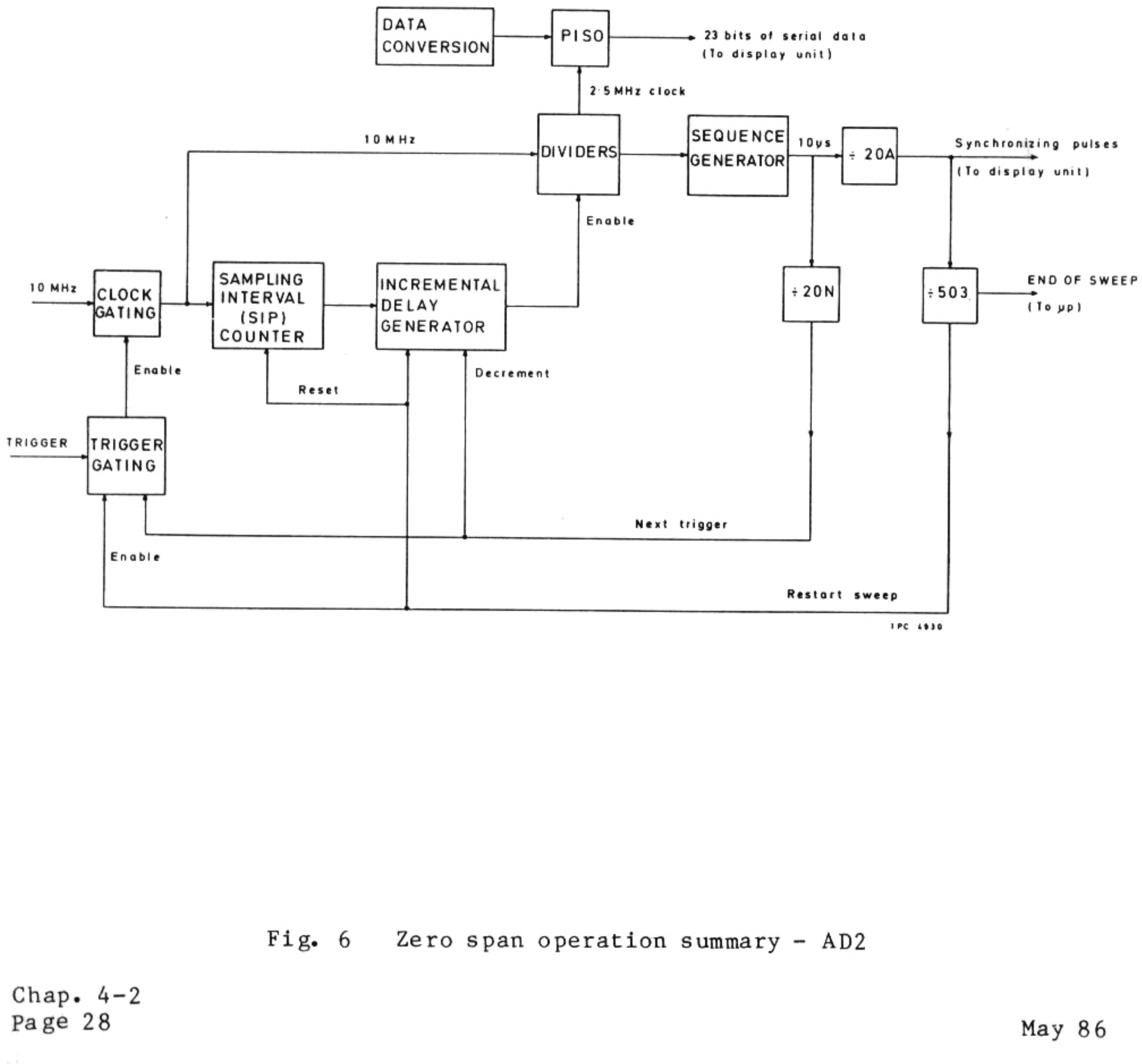


Fig. 6 Zero span operation summary - AD2

TABLE 6 ZERO SPAN SAMPLING - AD2

Time/div	SIP counter ratio	Overlay increment	Triggers	Division ratios		Ordinate separation	Mode
				A	N		
20 s	-	-	1	2000	1	400 ms	
10 s	-	-	1	1000	1	200 ms	
5 s	-	-	1	500	1	100 ms	
2 s	-	-	1	200	1	40 ms	
1 s	-	-	1	100	1	20 ms	
500 ms	-	-	1	50	1	10 ms	REAL
200 ms	-	-	1	20	1	4 ms	
100 ms	-	-	1	10	1	2 ms	
50 ms	-	-	1	5	1	1 ms	
20 ms	-	-	1	2	1	400 µs	
10 ms	-	-	1	1	1	200 µs	
5 ms	1000	100 µs	2	1	250	200 µs	
2 ms	400	40 µs	5	1	100	200 µs	SAMPLED
1 ms	200	20 µs	10	1	50	200 µs	WITH
500 µS	100	10 µs	20	1	25	200 µs	OVERLAYS
200 µs	40	4 µs	50	1	10	200 µs	
100 µs	20	2 µs	100	1	5	200 µs	
50 µs	10	1 µs	500	1	1	200 µs	
20 µs	4	400 ns	500	1	1	200 µs	SAMPLED
10 µs	2	200 ns	500	1	1	200 µs	
5 µs	1	100 ns	500	1	1	200 µs	

Real zero span

96. For real mode, the slower timebases of 10 ms/div to 20 s/div are available giving date conversion longer to process the information. In this mode data is transferred at the ordinate rate. For the fastest timebase of 10 ms/div ordinate separation is 200 µs for the 500 ordinates so that the transfer rate is 5 kHz. In the case of the slowest timebase of 20 s/div the data transfer rate is reduced to 2.5 Hz.

/D IV frequency sweeps

97. The sweep times available for this mode are the same as for real zero span. In this mode however, the data is transferred at 10 µs intervals each time accompanied by a synchronizing pulse. For the fastest timebase of 10 ms/div, ordinate separation is maintained at 200 µs but the upper unit performs averaging processes on adjacent data before displaying the amplitude information for each ordinate.

Serial data sync pulse generation

Circuit summary

98. The various zero span and frequency sweep display modes are determined by the circuit producing the serial data sync pulses since only when the data from the PISOs is accompanied by a sync pulse is it accepted by the display unit for display. The circuit may be divided into 5 functional areas :-

(1) Microprocessor control via IC47 and latch IC36 : The various counter sections of IC47 perform the following functions :- ÷100 generates the 100 µs CLOCK which provides the INT 7.5 signal to the processor; ÷20 A generates SERIAL DATA SYNC pulses at multiples of 200 µs; ÷20 N increments the delays between SERIAL DATA SYNC pulses; ÷503 generates END OF SWEEP pulses at the conclusion of each screenful of information. Latch IC36 asserts the control signals which define the mode of operation.

(2) Sequence start/stop by latches IC30 to IC32 : When required, the latches and associated gates interrupt the clock pulses to the sampling interval programmable counter and the sampling incremental delay generator until the occurrence of the next TRIG pulse.

(3) Sampling interval control via up counters ICs 33 to 35 and latch IC37 : The sampling interval programmable counter is preset by processor data mainly from latch IC37 with the 2 least significant bits from IC36. The preset defines the unit of delay, multiples of which are counted by (3) above to introduce a delay between the generation of one SERIAL DATA SYNC pulse and the next.

(4) Incrementing sampling intervals by up counters ICs 40 to 42 and down counters ICs 43 to 45 : The sampling incremental delay generator is clocked by the sampling interval programmable counter. The down counters provide an incrementing preset for the up counters so that SERIAL DATA SYNC pulses are generated after an increasing delay (e.g. if the delay from (3) above is 200 ns and the counter is sequentially decremented from 0 to 3 the interval between sync pulses is respectively increased by 200, 400 and 600 ns).

(5) Sequence generator IC9 and counter ICs10 & 11 : Operating details with respect to data output are given earlier. In the present context, the output from (4) above is used to enable the counters after an appropriate delay. The counter clocks the sequence generator whose every 10th pulse supplies SERIAL DATA SYNC pulses either directly at 10 µs intervals or at multiples of 200 µs.

Operation

Sampled mode

99. The simplest form of operation is zero span sampled mode in which IC9 generates a sequence of 10 negative-going 1 µs pulses with every 10th pulse counted by the ÷20 A and ÷20 N counter sections of IC47, and with every 7th pulse in the sequence clocking D-latch IC46b. In sampled mode, ratios A and N are both set to 1 so that whenever a SERIAL DATA SYNC pulse is transmitted to the display unit, the Q output of IC46b is set and serial data transfer takes place at the output of the PISOs. The sequence is terminated 7 µs later when the 7th pulse from the sequence generator clocks IC46b.

100. The rising edge of the 7th pulse clocks IC46b Q output low to assert DISABLE 10 MHz CLOCK while the Q(L) output removes DISABLE PROGRAMMABLE COUNTERS. The latter signal removes the reset to IC31b controlling the enable signal for the two sets of up counters IC33 to IC35 and IC40 to IC42, while DISABLE 10 MHz affects a number of D-latches. It clocks IC31a which resets IC30a which, in turn, resets IC30b to close gate IC53b. The gate halts the GATED 10 MHz clock to the sequence generator and to the first set of up counters. Having been reset, IC30a automatically reboots itself when its Q output goes low, by setting IC30a so that the reset is removed. IC30a Q output also resets latch IC46a which removes ENABLE DATA CONVERSION to counters IC11 causing them to reset to zero ready for a new sequence.

101. At this stage both sets of counters are disabled along with the GATED 10 MHz clock and the circuit is waiting for the next TRIG input to restart the sequence. In this, the simplest form of operation, ICs 33 to 35 are programmed to divide by 1,2,4 or 10 (depending upon timebase) while the number of previous triggers is recorded as an accumulated count in ICs 40 to 42. IC30b has been reset; its purpose is to provide a delay to ensure that the first GATED 10 MHz pulse does not reach the first set of up counters before they are enabled. If this were to happen, incorrect loading on terminal count would occur.

102. When TRIG is received from the trigger circuit it clocks IC30a which in turn clocks IC31b to assert ENABLE DIVIDERS to both sets of counters, as well as removing the resets to both IC46a, controlling the counter input to the sequence generator, and IC30b. Assuming that the sampling interval programmable counter has all 1s on its inputs (to divide by 1) then when the enable goes high a ripple carry will cascade through to pin 2 of IC53c to open the gate. Latch IC30b is now enabled to respond to the 10 MHz clock input by opening NAND gate IC53b. The resulting GATED 10 MHz clock signal commences on a falling edge which ensures that the first set of up counters is not clocked by the rising edge until at least 50 ns (i.e. half a clock period) after they have been enabled. The clock signal is gated through IC53c to provide the low RELOAD ON TERMINAL COUNT signal which allows the counters to reload, as well as providing the SAMPLING PERIOD CLOCK for the following sampling incremental delay generator. These counters count up to their maximum count at which a ripple carry occurs taking pin 13 of IC53d high to gate through the next clock pulse. This clocks IC46a which asserts ENABLE DATA CONVERSION to enable counter ICs10 and 11. Sequence generator IC9 which drives all the data conversion circuits, then recommences operation. The net result of the above actions is to accurately define the time at which data conversion starts with respect to the trigger pulse and hence of the analogue signal to be displayed.

103. When 20 pulses have been counted from the sequence generator by the ÷20 A and ÷20 N sections of IC47 the former sends a SERIAL DATA SYNC pulse to the display unit while the latter sets IC46b. IC46b Q(L) output asserts DISABLE PROGRAMMABLE COUNTERS low resetting IC31b which removes ENABLE DIVIDERS and stops the counting operation of both sets of up counters. The Q output takes DISABLE 10 MHz CLOCK unasserted high which decrements down counters ICs 43 to 45 by 1 and also holds open gates IC53c and IC53d. The opened gates allow the 10 MHz clock signal to continue through in order to provide the RELOAD ON TERMINAL COUNT signal. This enables both sets of counters to reload; the sampling interval programmable counter loads the data latched from IC36 and IC37, while the sampling incremental delay generator loads the decremented count from the down counters. Thus with the generation of each sync pulse the latter counters load a decremented count. This means that each time, they require an extra SAMPLING PERIOD CLOCK pulse to cause the overflow which

re-enables the sequence generator. Since the clock period is defined by the sampling interval counter (in this case to 100,200,400 or 1000 ns) the sequence generator is re-enabled - and hence the sync pulse is generated - after an increasing delay.

104. When the display store is full, 503 sync pulses will have been transmitted and the ÷503 counter section of IC47 clocks D-latch IC32b. The Q(L) output going low asserts END OF SWEEP to AD3 and the processor. The Q output asserts DISARM TRIGGER high which, after inversion, enables the down counters to load with their initial count of all 1s (i.e. to maximum) and also takes IC52b pin 8 high as a preliminary to halting the sync pulse generation process. This happens when DISABLE 10 MHz CLOCK goes low which clocks IC31a and IC32a. IC31a halts the GATED 10 MHz counter clock signal in the manner previously described which stops the sequence generator. IC32a Q(L) output goes high to close gate IC54a to the TRIG input, while the low Q output resets the END OF SWEEP latch IC32b. The processor responds to END OF SWEEP (after a delay) by setting SWEEP ARM high from IC36. This signal to IC54b provides an additional TRIG inhibit, and to IC47 counter sections resets both the ÷20 N and ÷503 counters. Then the processor pulses REFRESH RETRACE low from IC36 which takes D-latch IC32a Q(L) output low to remove its TRIG inhibit. The ÷20 N and ÷503 counters as well as the TRIG input, are still inhibited by SWEEP ARM and when this signal is taken low, IC30a is ready to respond to the next TRIG pulse. The data present in the display unit will now appear on the display. When the next TRIG pulse appears it will cause the generation of the first of the 503 pulses synchronizing the transfer of the data used to form the next waveform to be displayed.

Sampled with overlays

105. For the sampled with overlays mode the circuit functions as for the sampled mode except that several samples are taken per trigger. This is defined by the division ratio N for the ÷20 N section of IC47. For example, for 100 µs/div N is set to 5 which means that IC46b is set coincident with every 5th SERIAL DATA SYNC pulse.

Real

106. In real mode, every valid sample of data is accompanied by a SERIAL DATA SYNC pulse and is displayed at the ordinate rate. To achieve this, A is adjusted according to timebase for the ÷20 A counter section of IC47. Thus for the 20 ms/div timebase, A is set to 2 so that SERIAL DATA SYNC pulse separation is 400 µs. Unlike for the other zero span modes the ÷20 N counter and the up counters play no important part, merely dividing by 20 and 1 respectively.

/DIV frequency sweeps

107. For /DIV mode the FREQ/ZERO SPAN line from IC36 is latched high. After inversion, this causes a low to be applied to pin 9 of NAND gate IC57c which then closes to prevent the ÷20 A counter from providing the SERIAL DATA SYNC pulses. The high applied to pin 1 of IC57a opens the gate to the output from the sequence generator so that SERIAL DATA SYNC pulses are generated at 10 µs intervals. Since many more samples will be received than can be displayed, the samples are averaged before being displayed at the ordinate rate. For the fastest timebase, where ordinate separation is 200 µs, 20 data samples are averaged before the result is displayed. As for zero span mode the up counters are ineffective.

SYNTHESIZER

108. The frequency standard for the synthesizer is provided either internally from the 10 MHz temperature compensated crystal oscillator on AD4, or externally from a 1,2,5 or 10 MHz input to the EXT STD socket (see Fig. 7). Connection of an external standard automatically disables the internal one. The standard drives the sampling gate on AC6 to phase lock the 50 MHz varactor controlled crystal oscillator on AC1. Oscillator output feeds to the third mixer on AC2 as well as driving the sampling gate on AA10 to phase lock the second local oscillator. Oscillator output is divided to 10 MHz to provide a trigger source for AD2, the gating period for the frequency counter on AD4 and the calibration signal source for AD4. A further divided output provides 5 MHz used by both the up and down mixers on AC4 and for pulse generation on tracking generator board AE1. The main output at 50 MHz is used to phase lock the h.f. and l.f. master oscillators to the frequency standard when the masters are not being swept.

109. The h.f. master oscillator on AA5 covers the frequency range 530 to 938 MHz and is phase locked to the frequency standard by the sampling gate on AA4. This is driven by a divided output from AC1 which enables the oscillator to be locked at 5 MHz intervals over the band 530 to 935 MHz. Frequency setting and sweeping voltages from AB1 are summed in AA5 for the varactor diodes controlling the oscillator. Output is fed to the mixer on AA8 as well as being divided by AA6 to provide a frequency capable of being measured by the counter on AD3.

110. LF master oscillator AB3 covers the frequency range 26 to 34 MHz and is phase locked to the frequency standard by the sampling gate on AB4. Driven by the divided output from AC1, it enables the oscillator to be locked at 100 kHz intervals over the band 26 kHz to 34 MHz. Frequency setting and sweeping voltages from AB1 are summed with the phase correction voltage in AB3. Oscillator output feeds to the mixer on AB6.

111. The free-running interpolation oscillator on AB2 forms a third master oscillator and covers the range 28 to 32.5 MHz. Output is divided by 32 in AB6 to give an operational range of 110 kHz and an offset frequency of 950 kHz. The oscillator is swept from spans of 100 Hz to 20 kHz and can be set to a resolution of 1 Hz anywhere within the operational range. Frequency setting and sweep voltages from AB1 are summed in AB2. Because of the divider, the actual oscillator sweep range is 32 times greater than the selected span.

112. Output from the l.f. master oscillator on AB3 is mixed in AB6 with the output from the l.f. slave oscillator on AB5 and the difference frequency is compared for phase with the divided output from the interpolation oscillator on AB2. Any difference in phase causes an error voltage to be generated which adjusts the frequency of the varactor controlled l.f. slave. The l.f. slave is thus permanently phase locked to the sum of the l.f. master frequency and the interpolation oscillator frequency divided by 32.

113. For frequency translation purposes, the output from the h.f. master on AA5 is mixed in AA8 with the output from the h.f. slave on AA7 and the difference frequency is phase compared with the output from the l.f. slave. The h.f. slave is thus permanently phase locked to the difference frequency of the l.f. slave and h.f. master oscillators.

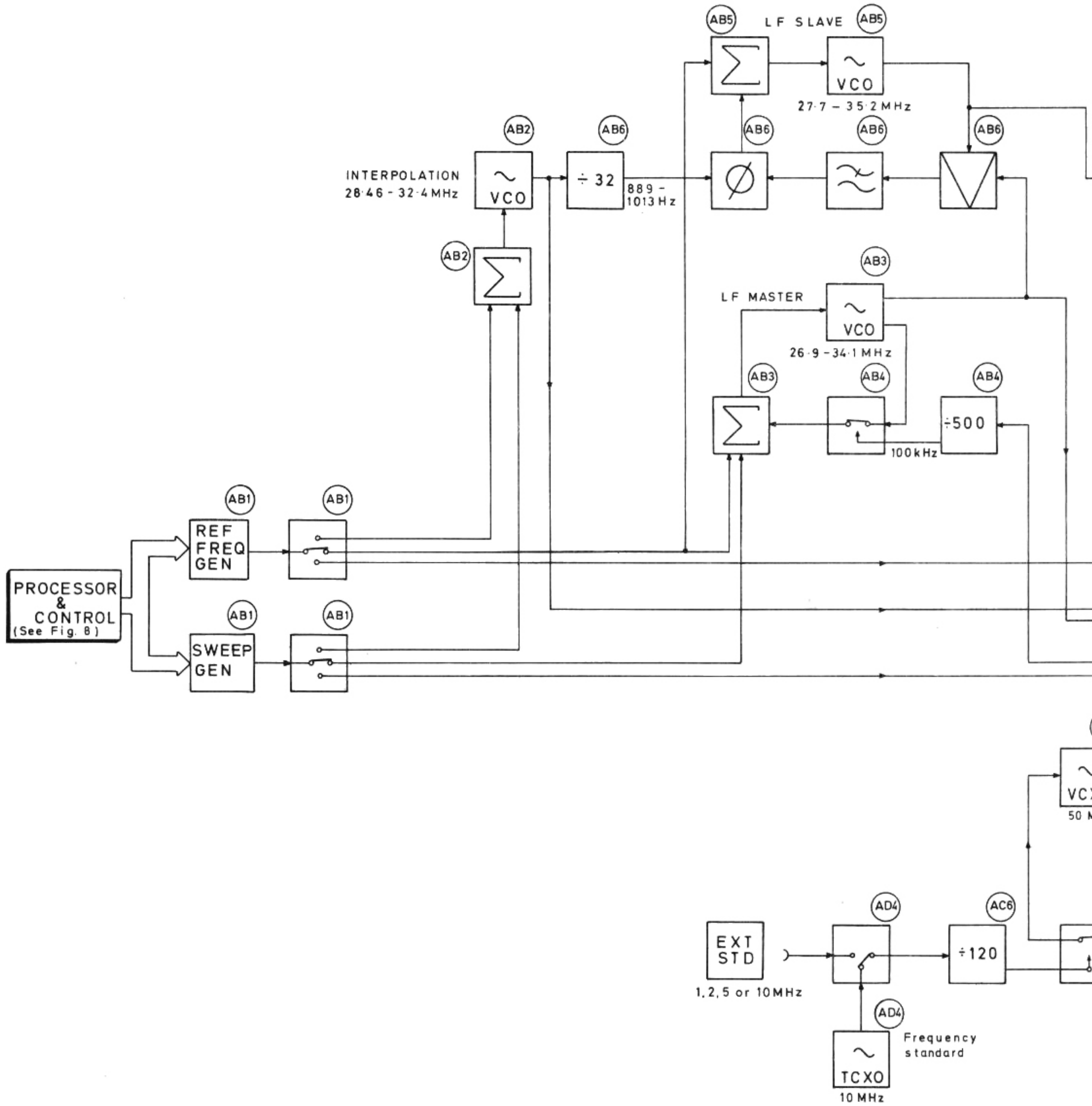
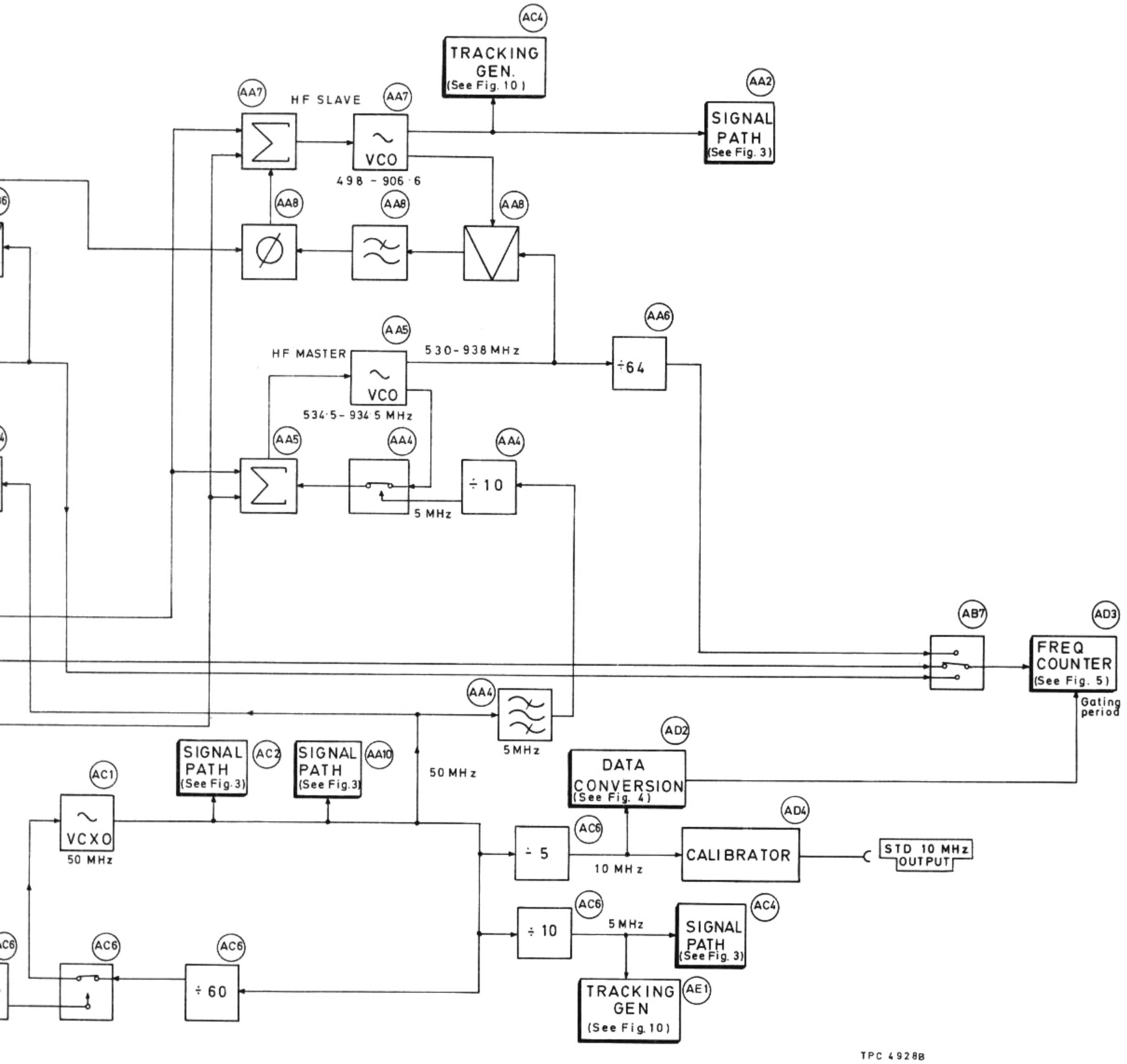


Fig. 7 Synthesizer block diagram



k diagram showing main functions of boards

114. When a new frequency is entered on the keyboard, the frequency settings of the interpolation, l.f. and h.f. master oscillators are each measured by means of the frequency counter on AD3. Computed reference frequency voltages are generated on AB1 and used to reset each oscillator, breaking phase lock as necessary. If the oscillator is to be phase locked, the voltage applied is just enough to pull the oscillator within loop acquisition range. Either one or both master oscillators may be phase locked, AA5 to 5 MHz increments, AB3 to 100 kHz increments. For frequency sweeping, a sawtooth voltage is generated on AB1 followed by attenuators which determine the sweep limits. To achieve the larger spans of 50 to 400 MHz, a x5 amplifier is used; for the smaller spans of 2 kHz and below an additional attenuator, on AB2, reduces the sweep by a factor of 10. Oscillator and attenuator settings for the various sweep spans are shown in Table 7.

TABLE 7 FREQUENCY SWEEP SETTINGS - AD2

Sweep span	Gain (AB1)	Attenuation (AB1)	Attenuation (AB2)	Interp. osc (AB2)	LF master osc (AB3)	HF master osc (AA5)
400 MHz	x5	x1		Fixed at 28.8 MHz	Locked on 100 kHz teeth at 30.5 MHz	Swept
200 MHz	x5	x2				
100 MHz	x5	x4				
50 MHz	x5	x8				
20 MHz	x1	x4				
10 MHz	x1	x8				
5 MHz	x1	x16				
2 MHz	x1	x1		Fixed at 28.8 MHz	Swept	Locked on 5 MHz teeth
1 MHZ	x1	x2				
500 kHz	x1	x4				
200 kHz	x1	x10				
100 kHz	x1	x20				
50 kHz	x1	x40				
20 kHz	x1	x1	x1	Swept	Locked on 100 kHz teeth	Locked on 5 MHz teeth
10 kHz	x1	x2	x1			
5 kHz	x1	x4	x1			
2 kHz	x1	x1	x10			
1 kHz	x1	x2	x10			
500 Hz	x1	x4	x10			
200 Hz	x1	x10	x10			
100 Hz	x1	x40	x10			

Board AA4 - Sampling gate

Circuit diagram : Chap. 7. Fig. 6

115. This board forms the phase detector for the master phase locked loop completed with AA5. A 5 MHz comb is produced from the 50 MHz reference and used to drive a sampling gate whose input is a buffered drive from the master

oscillator on AA5. The gate output, after being filtered, is applied to the summing input of the master oscillator. Also contained on the board is a high gain/low frequency response amplifier used for maintaining centre frequency drive when the oscillator is phase locked.

116. The 50 MHz reference frequency from AC1 is fed to a 5 MHz band-pass filter, is amplified by TR5 then shaped and further amplified by TR6 to drive t.t.l. divider IC3. The divider reduces the reference frequency to 5 MHz and the square wave is applied to long-tailed pair TR7, TR8 forming part of the pulse generator circuit. The amplifier preserves the fast rise time edges from the divider and drives a step recovery diode comb generator via an impedance matching transformer T2. Diode D6 output is shaped by L7, L8, C27, C28 and D7 into two antiphase pulses and these are used to switch the sampling gate. T1 passes these without attenuation but presents a high impedance to any common mode signals.

117. The 530 to 930 MHz signal from the master oscillator on AA5 is fed through a 5 dB pad and then amplified by 2-stage buffer TR1, TR2 which provides a forward gain of 10 dB and a reverse isolation of 70 dB. Sampling gate D1 to D4, switched at 5 MHz by the pulse generator, feeds into hold capacitor C15 and out to sample stretcher IC1. After passing through a 500 kHz low-pass filter the signal is amplified by IC2 which provides 6 dB of gain to overcome filter loss as well as providing a low impedance input for the summing amplifier on AA5. FET switches TR3 and TR4 respectively enable the loop to be opened and the output to be grounded when the oscillator is used either free running or during centre frequency setting. Drive for the switching f.e.t's is derived from the t.t.l. levels by means of level shifter IC4.

118. For free running operation the loop is disabled, the LOOP OPEN and the SAMPLING GATE DRIVE ON lines from AB1 being taken respectively high and low by the microprocessor. The LOOP OPEN line switches TR3 off to open the loop and TR4 on to ground the output, (as well as switching on the noise filter on AA5) The SAMPLING GATE DRIVE ON line inhibits divider IC3 operation. To set the oscillator centre frequency, the microprocessor takes the REF FREQ ENABLE line from AB1 high which switches TR10 on. This enables the output from the D/A converter on the REF FREQ IN line from AB1 to be connected to filter and storage capacitor C31. The voltage across the capacitor is then applied via voltage follower IC5b to x5 amplifier TR11 to TR14 which provides a 0 to 60 V drive on the REF FREQ OUT line to the master oscillator.

119. For phase locked loop operation, the AB1 D/A converter output is used only to set the oscillator to within the master p.l.l. capture range. To change to this mode, divider IC3 is enabled by a high from AB1 (which also switches in the loop filter on AA5). Switch TR10 connects the voltage on the REF FREQ IN line to C31 until the oscillator centre frequency is within the p.l.l. acquisition range when the switch is opened by a low on the REF FREQ ENABLE line. With the control voltage now stored in the capacitor, the LOOP OPEN line is taken low to switch off TR4 and switch on TR3 to complete the loop. Lock will be maintained until a further change in centre frequency is required, whereupon the loop will be switched off and REF FREQ ENABLE taken high allowing the oscillator centre frequency to be adjusted, and the sequence repeated. Any leakage into or out of C31 will cause a change in drive level to the master oscillator resulting in a compensating change in the sampling gate output.

Board AA5 - Master VCO

Circuit diagram : Chap. 7, Fig. 7

120. The master oscillator board consists of a v.c.o. with a frequency range of 530 to 938 MHz, a summing amplifier/lineariser for the oscillator drive, buffer amplifiers feeding three outputs and two series regulators providing low noise power lines for the oscillator.

121. TR6 is a common collector Clapp oscillator with frequency control achieved by three varactor diodes. The tuned circuit consists of L3, C8 and varactors D8 to D10 which enable the oscillator to achieve a frequency range of 530 to 938 MHz. DC voltages are applied to both ends of the varactor chain; at the anode end R35 sets the oscillator lower frequency, while at the cathode 0 to 60 V is required to swing the oscillator over its full range. The output from the emitter of TR6 is via level correcting network R41, C13, C14 to buffer amplifier TR7. Oscillator and buffer are shielded by a metal box mounted on the board.

122. Oscillator control voltages, for loop to R1, for centre frequency to R2 and for sweep to R3, are summed by the amplifier formed by TR1, TR2, TR3 and TR16. An 8-step diode shaper D1 to D7 changes amplifier gain as the input voltage rises in order to compensate for the oscillator's change in sensitivity over its operating range. Amplifier gain for the top of the oscillator's frequency range is set by R8. The summing amplifier is followed by a switched filter; R24, R25 and C1 form the loop filter for phase locked operation.

123. One output from power splitter T1, T2 feeds to isolating amplifier TR8, TR9 and the master/slave phase detector on AA8 while the other is taken via buffer TR10 to a second power splitter. The single stage buffers have a gain of 5 dB and a reverse isolation of 30 dB. The two-stage isolating amplifiers double this performance. Power splitter T3, T4 provides two outputs through 3 dB pads. One output via TR11, TR12 to AA6 enables the microprocessor to detect when it has set the oscillator centre frequency within the p.l.l. acquisition range while the second output via TR13, TR14 to AA4 completes the phase locked loop.

Board AA6 - Divider

Circuit diagram : Chap. 7, Fig. 8

124. Input from AA5 in the range 530 to 938 MHz is fed via a 16 dB pad to amplifier TR1, TR2 which provides 60 dB of isolation. Following division by 64 in IC1 the signal is passed by output buffer TR3 to oscillator selection board AB7. Output from this board enables the microprocessor to detect when it has adjusted the AA5 master oscillator to within the acquisition range of its phase locked loop.

Board AA7 - Slave VCO

Circuit diagram : Chap. 7, Fig. 9

125. The slave oscillator board consists of a v.c.o. with a frequency range of 498.6 to 906.6 MHz, a summing amplifier/lineariser for the oscillator drive, buffer amplifiers feeding two outputs and two series regulators providing low noise power lines for the oscillator.

126. TR5 is a common collector Clapp oscillator with frequency control achieved by three varactor diodes. The tuned circuit consists of L3, C6, C7 and varactors D8 to D10 which enable the oscillator to achieve a frequency range of 498 to 906.6 MHz. DC voltages are applied to both ends of the varactor chain, at the anode end R30 sets the oscillator lower frequency, while at the cathode 0 to 60 V is required to swing the oscillator over its full range. The output from the emitter of TR5 is via level correcting network R36, C11, C12 to buffer amplifier TR6. Oscillator and buffer are shielded by a metal box mounted on the board.

127. Oscillator control voltages, for loop to R1, for centre frequency to R2 and for sweep to R3, are summed by the amplifier formed by TR1, TR2, TR3 and TR13. An 8-step diode shaper D1 to D7 changes amplifier gain as the input voltage rises in order to compensate for the oscillator's change in sensitivity over its operating range. Amplifier gain for the top of the oscillator's frequency range is set by R8. TR4 provides active pull-down on the output of the amplifier.

128. One output from power splitter T1, T2 feeds via a 7 dB pad to tracking generator board AE4 while the other is taken via buffer TR7 to a second power splitter. The single stage buffers have a gain of 5 dB and a reverse isolation of 30 dB. The two-stage isolating amplifiers double this performance. Power splitter T3, T4 provides two outputs through 3 dB pads and isolating amplifiers. One is to AA2 while the other to AA8 completes the phase locked loop.

Board AA8 - Master/slave phase detector

Circuit diagram : Chap. 7, Fig. 10

Circuit summary

129. AA8 forms the phase detector for the master/slave phase locked loop. The loop ensures that the AA7 slave oscillator frequency is always offset below that of the AA5 master oscillator and that both are phase locked to the low frequency section. The signal from the l.f. section is split into two paths with a phase difference of 90^0, each path driving a phase discriminator. The discriminators compare these inputs with the h.f. section master/slave oscillator difference frequency. One discriminator output supplies the loop control voltage while the other checks for correct sideband lock and initiates the search oscillator when required.

Discriminator inputs

130. The low frequency section input signal from AB5 at 26.6 to 35.1 MHz takes two paths. One supplies the l.o. input of loop phase discriminator IC2, while the other is integrated by TR1 to produce a phase shift of 90^0 before being applied to the l.o. input of check phase discriminator IC4. HF section slave oscillator AA7 input at 503 to 903 MHz passes through a 10 dB pad and is then amplified by isolating amplifier TR4, TR5 and applied to the l.o. port of double-balanced mixer X1. The second h.f. input, that from the master oscillator on AA5 at 530 to 930 MHz is attenuated by 15 dB before amplification by TR6 and TR7 to drive the r.f. port of X1. Output is split into two and applied to the 90^0 out of phase r.f. ports of IC4 and IC2.

Loop phase discriminator

131. Loop phase discriminator IC2 ensures that the h.f. section is phase locked to the l.f. section. Discriminator output is fed to active loop filter IC1 whose gain is controlled during the search sequence by R51 which is switched into circuit by TR3 to prevent limiting of the amplifier.

Check phase discriminator

132. The 90^0 phase shifted output from the l.f. section and the master and slave oscillator difference frequency from the h.f. section are compared in IC4. Output from check phase discriminator IC4 is negative when phase lock is made to the correct sideband and positive for incorrect lock. For the latter condition, master and slave are either not in lock or lock is made to the incorrect sideband i.e the slave is higher in frequency than the master. These conditions are detected by IC3b which compares the mixer output with the reference set on its non-inverting input. For incorrect lock, comparator output goes negative which triggers Schmitt IC3a, switches TR2 off and switches OUT OF LOCK lamp D2 on.

133. Schmitt trigger IC3a switches TR3 on to reduce the gain of active loop filter IC1 as a preliminary to the search operation. With TR2 off, ramp generator IC3d commences operation producing a search signal which is amplified by IC3c to give a ±8 V 10 Hz ramp. IC1 combines loop filter and search oscillator outputs to sweep the AA7 slave oscillator through to the frequency at which lock is obtained. When this happens, the resulting negative signal from IC4 extinguishes the OUT OF LOCK lamp, switches off the search oscillator and restores the loop filter gain thus ending the search operation.

Board AB1 - D-A

Circuit diagrams : Chap. 7, Figs. 14-16

134. This board provides, by means of D-A converters, the analogue voltages enabling the microprocessor to control the operation of the h.f. master, l.f. master and interpolation oscillators. Front panel frequency selection is implemented by generating reference voltages for each of the voltage controlled oscillators. To enable frequency sweeping, a voltage ramp is generated through attenuators which define the sweep limits. Control signals are produced for controlling tracking generator operation, for setting i.f. gain and tuning the i.f. filters, for selecting input attenuation and for routeing oscillator output to the frequency counter for display. The board also contains the +70 V and +15 V line regulators.

Sweep voltage generation

135. When chip select lines CS60 and CS61 are sequentially taken high by the microprocessor, the data present on the quiet data bus at that time, consisting of all 1s is latched out from IC10 and IC11 respectively. This data provides the binary preset for down counters IC12 to IC14 which are loaded when the processor pulses IC11 pin 19 low. The counter outputs supply the changing inputs to the 12-bit sweep D-A converter IC15. When the LOAD line returns high, the counters are clocked by the square wave on the SWEEP CLOCK line, converted to t.t.l. by TR1, and the count down commences. Clock

rate is variable to compensate for oscillator non-linearity. Output from the converter is a sawtooth of 2^{12} = 4096 discrete steps and this is summed by IC17 with the output from D-A converter IC16. The 8-bit D-A produces a step to eliminate error due to an integrator's inability to track a sawtooth waveform. The amount of this offset is related to the sweep D-A clock rate. The sawtooth is used to sweep the synthesizer v.c.o's. Oscillator full sweep is set by the following sweep attenuator. This is formed from the potential divider R30 to R37 and the 8 output selection switches comprising quad f.e.t's IC21 and IC22. Switch control is exercised by IC18 whose selection data is latched out when clocked by the CS63 line. The appropriate line is latched high via one of the level shifters formed by IC19 and IC20 which causes the selected f.e.t. to switch on. For example, when IC21a is switched on it enables a full sweep of 400 MHz for h.f. master v.c.o. AA5, of 2 MHz for 1.f. master oscillator AB3 and of 640 kHz for interpolation oscillator AB2. If, instead, IC21b is switched on these frequency ranges are halved.

136. The sweep integrator consists of a D-latch operating various switches to select the RC components providing the time constant appropriate to the sweep time selected. When chip select line CS64 goes high, selection data is clocked out from IC24 via level shifters IC25,26 to control f.e.t. switches TR2, TR3 and IC27. These switch into circuit combinations of resistors R52 to 55 and capacitors C34 to 3[illegible] For example, for a sweep time of 200 ms IC24 pins 5 and 12 are taken high which switch on TR3 and IC27c respectively. The switches select R55 in parallel with R52 and C35 in parallel with C34 to provide an integration time constant of 2.2 ms (see Table 8). During sweep flyback, TR2 is switched on to bypass the resistors and allow the capacitors to discharge.

137. The sawtooth output from the sweep integrator is next fed to the rate limiter formed by IC28, TR4 and TR5 whose purpose is to slow the rate of fall of the ramp which would otherwise allow phase lock to be broken. The rising ramp charges C41 through diode D2 until on the occurrence of the falling edge the diode is reverse biased. This shuts off the input and enables C41 to discharge at a constant rate through current drain TR4. The modified sawtooth is fed from emitter follower TR5 to the output selection switches.

138. When line CS65 clocks D-latch IC29, output selection logic on pins 2,5 and 6 is fed via the level shifters comprising IC30 to operate one of the three f.e.t. output switches TR6, TR7 or TR8. When TR7 or TR8 is switched on, the sweep signal is routed respectively to either the master v.c.o. on AB3 or the interpolation v.c.o. on AB2. When TR6 is switched on, the sweep signal is fed to the master v.c.o. via the switched gain amplifier TR9 to 13 with gain switch TR14. Gain selection is controlled from latch IC24; When pin 19 is low, TR14 is switched off and gain is unity, when this pin is taken high, TR14 switches on and gain is increased 5 times. The higher gain is selected to achieve sweep spans of 50 to 400 MHz.

TABLE 8 SWEEP INTEGRATION - AB1

Sweep time	IC24 pins 2	5	6	9	12	15	Integrator Time constant
100 ms	L	H	L	L	L	L	1.1 ms
200 ms	L	H	L	L	H	L	2.2 ms
500 ms	L	H	L	L	H	H	5.6 ms
1 s	L	L	H	L	L	L	11.1 ms
2 s	L	L	H	L	H	L	22.2 ms
5 s	L	L	H	L	H	H	55.5 ms
10 s	L	L	L	H	L	L	111 ms
20 s	L	L	L	H	H	L	222 ms
50 s	L	L	L	H	H	H	555 ms
100 s	L	L	L	L	L	L	1.12 s
200 s	L	L	L	L	H	L	2.24 s
500 s	L	L	L	L	H	H	5.61 s
Bypass	H	L	L	L	L	L	-

Reference level generator

139. IC50 supplies the 5 V reference which is used for the reference level D-A converter, the 70 V line regulator and, via potential divider R100, R101, the 1.5 V reference for the board level shifters. The D-A converter consists of three 8-bit converters ICs 52,55 and 58 whose input data is applied from D-latches ICs 53,56 and 59. The latches are sequentially clocked by chip select lines CS70 to 72 to load the binary data from the quiet data bus. Output from the first converter is voltage converted by IC54, attenuated by R106 and then summed with the output from the second converter. This process is repeated by IC57, R112 and IC60. Due to the attenuation, each preceding converter output is one sixtyfourth that of the following thus enabling the REF FREQUENCY VOLTAGE output to AA4, AB2 and AB3 to be accurately set. The voltage to AB2 is applied when IC29 pin 16 is taken high. This supplies the reference frequency voltage enable signal which switches on TR32 (similar enable switches are fitted on boards AA4 and AB3). For the two lowest used sweep ranges of 100 Hz and 200 Hz, IC29 pin 19 is also taken high to switch on TR31 to supply additional low-pass filtering. The corresponding reference frequency voltage enable signals for AA4 and AB3 are supplied from IC29 on pins 12 and 15 respectively.

140. The INTERP OSC ATTEN CONTROL line to AB2 controls the sweep limits of the interpolation oscillator. When this line is taken high by IC24 pin 19, sweep span is 10 times greater than when the line is low.

Control signals

141. Microprocessor control signals are applied by means of three additional D-A converters. Tracking generator output level is controlled by 8-bit D-A converter IC4. The selected level is clocked out by CS75 then amplified by 2 by IC2d before being applied, to a maximum of 10 V, to AE6. IC3 and IC2c are similarly configured and clocked by CS74 to control the i.f. gain setting for AC3. A third 8-bit D/A converter, IC1 with filter IC2a provides i.f. filter tuning. When clocked by CS73, the output voltage on the CENTRE FREQ ADJUST line controls the varactor diodes providing filter tuning on AC3.

Control latches

142. Oscillator control latch IC70, clocked by CS66, provides control signals for tracking generator operation, for h.f. or l.f. master oscillator phase locking and for selecting input to the frequency counter from the h.f. or l.f. master oscillators or from the interpolation oscillator. Input attenuator latch IC40, clocked by CS67, provides input signal selection, input attenuator selection and the overload clear signal.

+70 V and +15 V line regulators

143. The +80 V line from AR2 is connected to series-pass transistor TR24 which supplies a regulated +70 V for board AB3 and all h.f. amplifiers as well as the X1/X5 amplifier on this board. The output is potential divided by R97, R98 and the junction sampled on pin 3 of comparator IC41. If, for example the output current rises, comparison with the 5 V reference on IC41 pin 2 causes output pin 6 to become more positive so increasing the conduction of TR22. This decreases the base drive for TR24 and hence decreases the output current. IC41 pin 6 going low switches on l.e.d. D4 to indicate the out of regulation condition. Short circuit protection is provided by TR20 and TR21. In this case the increased current through R95 develops enough potential to forward bias TR20 which then switches on. This causes TR21 to switch on and take TR24 base to ground and thus to disable the output. TR21 also switches on for standby operation due to the -5.5 V line being taken to 0 V, and the output is disabled.

144. The +20 V line from the display unit via AR2 is converted to a regulated +15 V for AA11. The regulator has a low-pass filter at its input, D6 protects against reverse transients, and preset R76 provides control of the output voltage setting. For standby operation, the -15 V line is taken to 0 V which causes TR19 to switch on. This applies 0 V to VADJ IC6 and since the regulator maintains VOUT at 1.2 V higher than VADJ, the +15 V output drops to +1.2 V, effectively disabling the output to AA11.

Board AB2 - Interpolation oscillator

Circuit diagram : Chap. 7, Fig. 8

Oscillator

145. Frequency control of Colpitts oscillator TR1, in the range 28 to 32.5 MHz, is by the voltages on the REF FREQ IN and SWEEP lines to varactor diodes D1 to D4 which tune the tank circuit formed by T1, C2 and C3. The

basic operating frequency, determined by the keyboard-selected frequency, is set by the voltage on the REF FREQ IN line from the D-A converter on AB1. Oscillator sweeping is implemented by the voltage from the ramp generator on AB1. Attenuators on AB1 define the sweep limits and are complemented by the switched attenuator on this board. For a selected span of between 100 Hz and 2 kHz the SWEEP voltage is fed through attenuator R10, R11 and R12. For spans of between 5 kHz and 20 kHz the SWEEP ATTEN CONTROL line switches on f.e.t. TR2. This causes R10 to be bypassed thus reducing attenuation by a factor of 10 to make the sweep limits ten times greater. T1 provides coarse control of the frequency, while D8 and R12 together with C2 and C3 reduce the temperature coefficient of the oscillator. The oscillator operates at a frequency 32 times higher than required to allow subsequent division by 32 on AB6. This is in order for the noise components present in the output from a free-running oscillator to be reduced by a factor of 32. The division also affects the sweep operation; for a selected span of 20 kHz the actual oscillator sweep is 640 kHz.

146. Output from TR1 source drives into an amplifying stage formed by TR3 with series feedback and TR4 with shunt feedback. The stage provides a gain of 23 dB. After limiting by diodes D6, D7 the signal at 1.1 V p-p is divided in power splitter T2, T3 which has 40 dB of isolation between output ports and a loss of 4 dB. 9 dB of gain is provided by output buffer amplifiers TR5 and TR6 which are grounded-base stages having a reverse isolation of 60 dB. Output level is 2 V p-p into 50 Ω. This is fed to AB6 for frequency division by 32, and to AB7 for selection purposes.

Board AB3 - Master VCO

Circuit diagram : Chap. 7, Fig. 17

147. This board contains the master v.c.o. which covers the frequency range of approximately 30 MHz ± 4 MHz and can either be swept, or phase locked in 100 kHz increments by AB4.

Oscillator

148. Frequency control of Colpitts oscillator TR1 in the range 25.75 to 34.25 MHz is by voltages on the REF FREQ IN, SWEEP and PLL CONTROL lines to varactor diodes D1 to D3. The basic operating frequency of the v.c.o. is determined by the voltage on the REF FREQ IN line from the D-A converter on AB1. This voltage is stored in C42. When the oscillator is operating in the p.l.l. mode, frequency setting is by the D-A output being momentarily applied to C42 when the REF FREQ ENABLE line from AB1 goes high to switch TR9 on. The stored voltage is then sent by voltage follower IC2a to varactor diodes D1 and D2 which control the frequency of master oscillator TR1 as well as out on the REF FREQ OUT line to AB5 to coarse tune the slave oscillator. For phase locking, the voltage on the PLL CONTROL line from AB4 is fed to varactor D3. Any tendency for frequency drift due to leakage by C42 is compensated for by a proportion of the PLL CONTROL voltage monitored by IC2b being used to recharge the capacitor. When the oscillator is operated in the sweep mode, the phase locked loop is disabled on AB4 and frequency control of the v.c.o. is taken over by the voltage on the SWEEP line from AB1. In this mode, f.e.t. switch TR9 is held on and the REF FREQ IN voltage is applied continuously.

149. Reduction of phase noise is achieved by decoupling both the internal reference of supply regulator IC1 by R42, C36 as well as the -12 V supply rail by R8, C9.

Output

150. Output from TR1 source drives into an amplifying stage formed by TR3 with series feedback and TR4 with shunt feedback. The stage provides a gain of 23 dB. After limiting by diodes D4, D5 the signal at 1.1 V p-p is divided in a power splitter having 40 dB of isolation between output ports and a loss of 4 dB. 9 dB of gain is provided by output buffer amplifiers TR5,6 and 8, which are grounded-base stages having a reverse isolation of 60 dB. Output level is 2 V p-p into 50 Ω.

Board AB4 - Sampling gate

Circuit diagram : Chap. 7, Fig. 17

151. Input from the master v.c.o. on AB3 in the range 26 to 34 MHz to balanced buffer TR1, TR2 is fed to the first sampling gate formed by D1 to D4. Drive for the mixer originates in the 50 MHz input from AC1. Following division by 500 by ICs 4,5 and 6 the resulting 100 kHz is connected to the pulse shaper. TR8 and TR9 provide a high-level drive for the pulse shaping components C10 and L2. The circuit is basically a differentiator and produces positive and negative pulses from the respective leading and trailing edges of the square wave input. The leading, positive pulse switches on n.p.n. pulse driver TR5 for 50 ns and this produces two antiphase pulses from the outputs of T2. T1 passes these without attenuation to the sampling gate but presents a high impedance to any common mode signals. This prevents any loading of the input signal during the gate open time. C8 is the hold capacitor and the gate output is buffered by f.e.t. input IC1. IC1 has a stretcher capacitor C9 which increases the loop bandwidth by compensating for the slew-rate limitation of the op-amp. The buffer formed by TR3, TR4 follows which lowers the source impedance for the second sampling gate.

152. The negative pulse from the pulse shaper switches on p.n.p. pulse driver TR6 to operate the second sampling gate formed by D8 to D11. Since the negative pulse is derived from the trailing edge of the divider output the second gate operates in antiphase to the first. It also has a larger hold capacitor whose effect is to reduce the 100 kHz ripple otherwise present on the PLL CONTROL line. A second pulse stretcher IC2 follows which has an offset control to centralize the capture range of the loop. An attenuator adjusts the loop gain before the PLL CONTROL signal is fed out from the lead/lag filter to AB3. For v.c.o. sweep operation, the p.l.l. is disabled by a high logic level on the PHASE LOCK ON line from AB1. This switches on TR7 to take the output from the second sampling gate to ground as well as disabling first counter stage IC4.

Board AB5 - Slave VCO

Circuit diagram : Chap. 7, Fig. 18

153. The AB5 oscillator is permanently phase locked to the sum of the frequency of AB3 and the frequency of AB2 divided by 32.

Oscillator

154. Frequency control of Colpitts oscillator TR1 in the range 26.65 to 35.15 MHz is by the voltages on the REF FREQ IN, SEARCH SIGNAL and PLL CONTROL lines to varactor diodes D1 and D2. Operating frequency is roughly set by the voltage on the REF FREQ IN line from the master oscillator on AB3 which operates approximately 1 MHz lower than the slave. Main loop control is by the voltage from AB6 on the PLL CONTROL line to IC2. IC2 sums this voltage with that from AB6 on the SEARCH SIGNAL line which ensures that the master/slave frequency relationship is maintained. The latter line is decoupled by R55 and C36 to reduce any noise component when the loop is locked.

Output

155. Output from TR1 source drives into an amplifying stage formed by TR3 with series feedback and TR4 with shunt feedback. The stage provides a gain of 23 dB. After limiting by diodes D3,D4 the signal at 1.1 V p-p is divided in power splitter T1,T2 having 40 dB of isolation between output ports and a loss of 4 dB. 9 dB of gain is provided by output buffer amplifiers TR5 and TR6 which are grounded base stages having a reverse isolation of 60 dB. Output level is 2 V p-p into 50 Ω.

Board AB6 - Phase detector

Circuit diagram : Chap. 7, Fig. 18

156. This board phase locks the AB5 slave oscillator to the sum frequency of the AB3 master oscillator and the AB2 interpolation oscillator divided by 32. A search oscillator sweeps the slave until the correct lock is found when search is disabled. The board also contains the detector which ensures that the frequency of the slave v.c.o. is maintained higher than that of the master.

157. The 27 to 35 MHz input from the slave v.c.o. on AB5 is mixed by X1 with the 26 to 34 MHz input from the master v.c.o. on AB3. The difference frequency of approximately 1 MHz is fed to the buffer formed by TR2,TR3. TR2 provides 20 dB of gain and feeds into emitter follower TR3 which gives a low impedance drive for the following two phase discriminators. Filter L1, C6 isolates the input from discriminator switching signals.

158. TR1 buffers the 28 to 32 MHz input from AB2 to t.t.l., and the signal is first divided by 16 in IC1 before being applied to two parallel divide by 2 stages formed from IC3. These are D-type bistables whose data inputs are supplied from the Q(L) output of IC3a so that each bistable divides by 2. IC3a outputs are used to operate f.e.t. switches IC4c and d in antiphase in the loop phase discriminator in the main loop. Similarly, IC3b operates switches IC4a and b in antiphase in the check loop discriminator. Thus four output signals are available with 90^0 phase shifts; the antiphase drive signals for one discriminator being in quadrature with the antiphase drive signals for the other.

159. A mean positive level results from the check phase discriminator when lock is correct, and a zero or negative level for an incorrect lock (see Table 9). For the latter condition, comparator IC5a forward biases D3 causing the OUT OF LOCK l.e.d. D1 to illuminate, switches TR5 on and switches TR6 off. Switching TR6 off starts relaxation oscillator IC5d which produces a 10 Hz triangular waveform. The output from the search oscillator is buffered and amplified by IC5c before passing it out to sweep the v.c.o. on AB5. When TR5 is switched on it, in turn, switches TR4 on to reduce the loop gain during the search operation. A 0.3 µs delay is introduced by R18, R19 and C20 to provide sufficient time for the loop to achieve complete lock.

160. The check phase discriminator output is positive for correct mixer operation, but negative when the master oscillator is incorrectly higher in frequency than the slave (see Table 9). During the fault condition the out of lock condition is also detected causing f.e.t. TR4 to be switched on. This shorts C13 so that IC5b acts as an amplifier and inverter for the negative output from the phase detector. The resulting positive signal is fed to the PLL CONTROL line and prevents lock being achieved by the slave v.c.o. until sufficient negative voltage has been applied by the search oscillator to shift the slave to about 1 MHz above the master. During normal operation switch TR4 is off and IC5b acts as an integrating loop filter.

TABLE 9 DETECTOR OPERATION - AB6

Loop signal/AB2 phase	$+90^0$	0^0	-90^0
Mean loop phase discriminator output voltage	-ve	0	+ve
Mean check phase discriminator output voltage	0	+ve	0

Board AB7 - Oscillator select

Circuit diagram : Chap. 7, Fig. 8

161. TR1 and 2, TR3 and 4, TR5 and 6 form converter stages to amplify the input signals from AB2, AB3 or AA6 to t.t.l. levels. The three signals are fed to OR-gates IC1a,b and c for gating with the OSC SELECT lines from AB1. When the required line is taken low by the microprocessor selection logic, the appropriate input signal is passed to NAND-gate IC2 - the remaining OR-gates being inhibited by the action of the associated pull-up resistors. With two of its inputs held high, IC2 is enabled and the selected oscillator input is passed out to the frequency counter on AD3.

Board AC1 - 50 MHz xtal oscillator

Circuit diagram : Chap. 7, Fig. 20

162. This board contains a low noise 50 MHz crystal oscillator which is phase-locked by AC6 to a 10 MHz t.c.x.o. The phaselock loop has a very narrow bandwidth to reject any noise or spurious sidebands on the t.c.x.o. and this is achieved by dividing down the two phaselocking signals on AC6. Oscillations are maintained during standby operation in order to provide the processor clock signal.

163. TR1, TR2 form the varactor controlled crystal oscillator whose +11.5 V power supply is provided by regulator IC1. Normally, IC1 is supplied by +15 V from AC6. When the +15 V line drops to 0 V under standby operation, TR12 switches on and the +14.5 V line from AR2 supplies the power. D5 then becomes reverse biased and prevents power being fed back to AC6. The error signal from AC6 supplies the control voltage for varactor diodes D1 to D4. Oscillator frequency is set by L3 and peak gain at 50 MHz is set by L2. Emitter followers TR7 and TR8 at this point supply local oscillator inputs for the mixers on boards AC2 and AA10 respectively. Three isolating amplifiers follow : TR4, TR5 feed to AB4 while emitter follower TR9 feeds via TR10 to AA4 as well as via TR11 to the sampling gate on AC6 supplying the oscillator control voltage.

Board AC6 - Phase detector

Circuit diagram : Chap. 7, Fig. 20

164. TTL drivers TR3, TR4 connect the 50 MHz input from AC1 to divider IC9 whose 10 MHz and 5 MHz outputs at this point are taken to AD2, AD4 and AC4, AE1 respectively. The 10 MHz from IC9 is further divided by 60 by IC7 and IC8 and the result integrated by IC1. A sampling gate follows consisting of f.e.t. switch TR2 and voltage follower IC2a. TR2 switching is controlled from AD4, either by an internal 10 MHz t.c.x.o. or an external 1,2,5 or 10 MHz reference. This input is fed to ICs 5 and 6 which perform division by 120 and the result is used to clock monostable IC4. 300 ns negative pulses from the pulse generator switch on TR1 which in turn switches on TR2 to store the instantaneous output from IC1 in sample and hold capacitor C4. Sampling gate output is taken via amplifier and loop filter IC2b to the varactor diodes on AC1 so controlling the frequency of the v.c.x.o. In order to provide an out of lock indication, the signal from IC2a is fed to the out of lock detector formed by IC3. For an out of lock condition, the input to pin 3 of comparator IC3a exceeds the reference voltage set by potential divider R9, R10 causing voltage follower IC3b output to go high. This sets the REF UNLOCKED FLAG which causes an appropriate warning to be displayed on the screen.

Board AD4 - 10 MHz calibrator

Circuit diagram : Chap. 7, Fig. 39

Functions

165. This board performs the functions summarized below :-

(1) Provides the master 10 MHz reference to AC6 for the 50 MHz phase locked loop.

(2) Accepts 10 MHz (50 MHz/5) back from AC6 and derives from this :-

(a) A square wave of fundamental level -10 dBm which feeds the STD 10 MHz OUTPUT socket.

(b) A -10 dBm sinusoid.

(3) In instruments without the standard tracking generator, when the SWITCH CONTROL logic input is active, the -10 dBm sinusoid is fed to the attenuator calibration input. When SWITCH CONTROL is inactive and the instrument is in the input mode, the sinusoid and any harmonics are attenuated sufficiently to ensure that none of them has a level at the first attenuator pad greater than -150 dBm.

(4) Is able to accept a voltage from the back panel potentiometer and use this to adjust the 10 MHz reference to compensate for long-term drift.

(5) Detects the presence of an external standard input of >50 mV p-p and substitutes this for the internal 10 MHz standard.

(6) On detecting the external standard, sets the EXT STD flag.

Standard selection

166. The internal standard is provided by temperature compensated crystal oscillator (TCXO) X1. Adjustment in the range ±50 Hz is provided by varactors D1,8,9 and potentiometer R2 via low-pass filter R3, R4 and C1. To compensate for long-term drift this adjustment can be over-ridden by a back panel potentiometer which gives the same range and is normally isolated by a ganged switch. Oscillator output provides one of the two inputs to dual line receiver IC1. When required, an external standard of 1,2,5 or 10 MHz provides a second input to IC1 and this is applied to pin 12. These signals are converted to t.t.l. by IC1 and the external standard passed on to the peak-peak detector formed by C8, D2, D3, C9, R14 and one Schmitt NAND of IC2. If the upper level of the external standard output from IC1 exceeds about 2.6 V the external standard is selected in preference to the internal one. In this case, the peak-peak detector takes IC2 pin 11 low and this is applied to IC1 pin 5 to inhibit output from the internal standard as well as being used to set the EXTERNAL STANDARD FLAG low. The selected standard is fed from IC2 pin 6 to AC6.

Calibrators

167. TR1, TR2 produce a square wave with fundamental level -10 dBm when fed with a sine wave derived from AC6. TR2 when on, forms a current source with current defined by R21, R22 and the -15 V rail, but is turned off when its emitter voltage is raised by the input signal via follower TR1. C11, R16 minimize risetime to ensure adequate harmonics up to 400 MHz.

168. TR3, TR4 operate in a similar way. L2, C14, L3 are part of a filter which renders the output from this pair approximately sinusoidal. D4, D5, D6, driven by IC3 via R29, R30, R31 form the output switch for the -10 dBm sinusoid. When SWITCH CONTROL is low, D4 and D6 are biased on and D5 off, thus passing the signal with only a small insertion loss. When the instrument is in input mode, the bias is reversed and the signal is attenuated by at least 100 dB.

MICROPROCESSOR AND CONTROL

169. Inputs from the variable control on AZ2 and the keyboard AF1 are applied to latches on AF2. Any change in this data due to movement of the control or to a key being pressed is detected on this board and results in a processor interrupt on AD3 (see Fig. 8). The processor responds by latching the amended data onto the quiet data bus during a read cycle. Similarly, interrupts occur due to movement of the variable controls on the two AZ1 boards but not until the direction of movement has first been resolved on AF2. Other processor interrupts are caused by an input attenuator overload, and end of sweep, as well as for controlling the transfer of serial housekeeping data between the r.f. and display units. Servicing of all interrupts is organized by a Real Time Executive residing in the main program held in EPROM.

170. Data transfer between the microprocessor and the memory, status register and frequency counter is by means of the µP data bus. The memory bank consists of 56 K of EPROM holding the main program, 4 K of EAROM to store the current instrument settings when the instrument is switched off and 4 K of RAM for scratch pad operations. The 8-bit status register holds the r.f. unit address in 3 bits which enables up to 8 r.f. units to be connected to one display unit. Two bits convey instrument temperature information. A further two bits indicate when an external standard is connected and when the internal one is uncalibrated. The final bit indicates when the optional tracking generator is fitted. The frequency counter on AD3 is used to monitor the h.f. master, l.f. master and interpolation oscillators during frequency setting operations. Data transfer for switching, control and flag reads is via a 2-way buffer between the µP data bus and the quiet data bus. The buffer prevents processor activity from spilling over onto the quiet bus to prevent possible analogue interference.

171. Housekeeping data is conveyed between r.f. and display units by the 20 mA current loop on AR1. This board also feeds serial display data accompanied by synchronizing pulses for serial to parallel conversion to the display unit. The associated board AR2 contains the instrument temperature sensor controlling the cooling fan as well as the audio amplifier used for monitoring purposes. Power is supplied from the display unit to the regulators and line cleaners on this board as well as to AA11.

Board AA11 - Line cleaner

Circuit diagram : Chap. 7, Fig. 12

172. This board contains the thermistor which adjusts fan speed to maintain the instrument at a constant temperature, regulators IC1 and IC3 for the ±10 V lines and line cleaners based on 4 sections of IC2.

Line cleaners

173. The purpose of the line cleaners is to remove any low frequency a.c. component occurring on the d.c. supply lines to the oscillators. All the line cleaners operate and are configured similarly to the +14.5 V one here described. The principle of operation is that any detected change in current on the supply line causes a greater or lesser amount of current to be drawn from the supply line in compensation. Approximately 10 mA of current is constantly drawn through D5 and R8 by TR1 and any change in the supply current causes the standing current to be correspondingly increased or reduced. R8

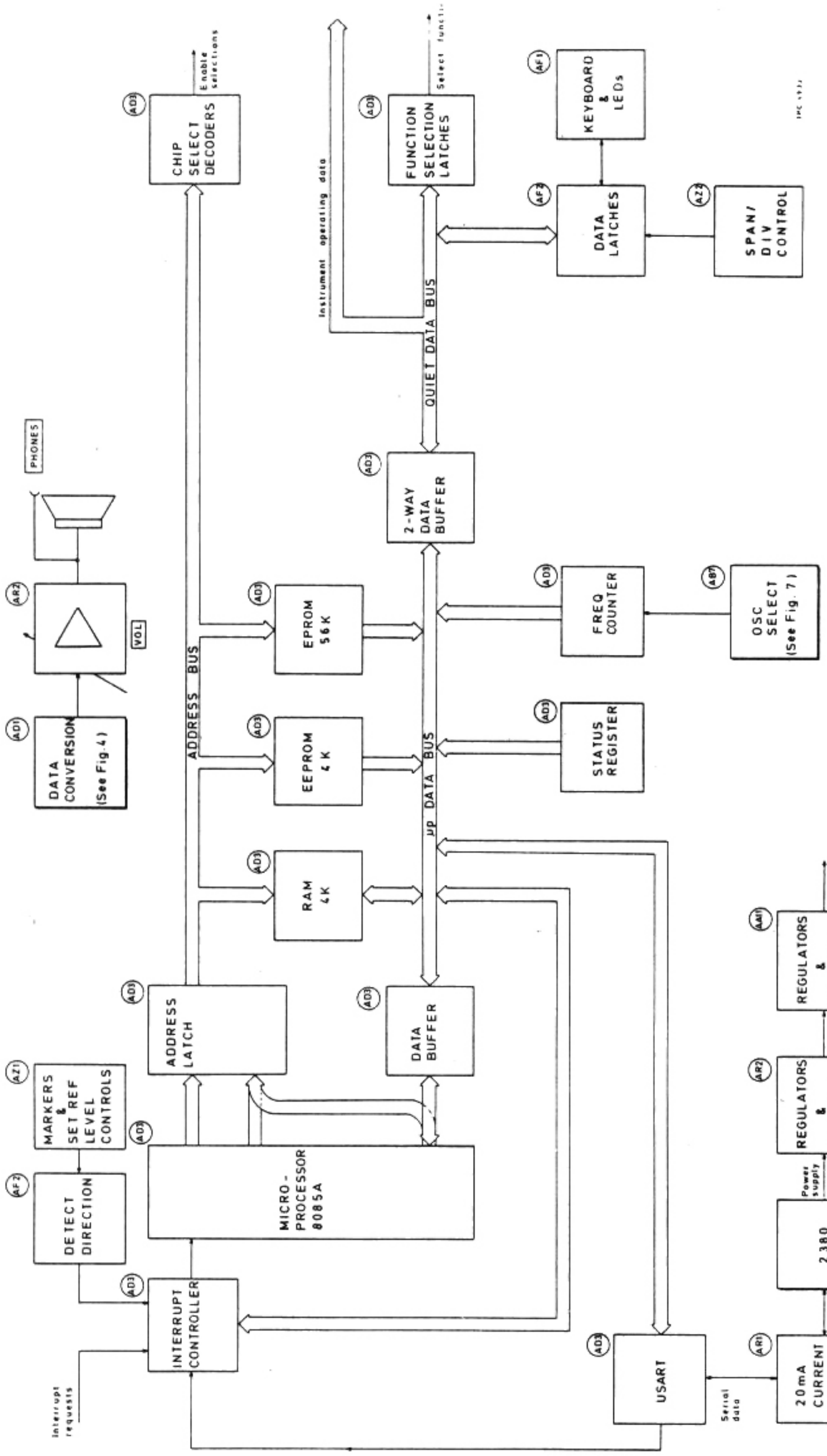


Fig. 8 Microprocessor & control block diagram showing main functions of boards

forms a potential divider with R7 and R4 to maintain the charge on C4 which provides the reference for IC2a. IC2a is a differential amplifier which controls the conduction of TR1. Due to the time constant of C4 and R5, only long-term changes of current through R8 e.g. due to temperature changes affect the stored reference causing IC2a to restore TR1 conduction to the correct value. At switch on, D2 enables C4 to quickly attain the reference level. Zener diodes D3 and D5 perform standoff functions while D4 provides protection against a TR1 base-emitter reverse bias. In operation, an increase, for example, of voltage on the supply line is detected by R3 and R31. This causes the inverting input of IC2a to go more positive increasing p.n.p. TR1 conduction to bleed away the extra current so restoring the original level.

Board AD3 - Microprocessor

Circuit diagram : Chap. 7, Fig. 35-38

174. The microprocessor and associated circuits are described in the order in which they appear in the circuit diagram.

Frequency counter

175. The frequency counter on this board is used as part of the frequency setting process to measure the settings of the h.f. master v.c.o. on AA5, the interpolation v.c.o. on AB2 and the l.f. master v.c.o. on AB3. The required oscillator output selected on AB7 is fed into the t.t.l. driver TR1,2 and used to clock 4-bit counter/latch IC16. To provide the gating period for this counter, a 10 MHz input derived from the 50 MHz crystal oscillator on AC1 is divided down to 2 MHz by IC8a then fed to the counter 1 section of IC30. The counter section is programmed to produce gating periods of 7.8125 ms for the two master oscillators and 31.25 ms for the interpolation oscillator. The gating periods determine the measuring resolutions of 8.192 kHz for AA5, 128 Hz for AB3 and 32 Hz for AB2. Dividing AB2 output by 32 on AB6 sets the system accuracy to 1 Hz.

176. IC30 output provides the data input for retimer IC31a which, when clocked, opens IC49a to IC16 which then commences counting the clock input on pin 8. The counter m.s.b. output cascades into the 16-bit counter formed by IC30 section 2. At the end of the gating period, gate IC49a is closed and the latest count is held latched out to buffer IC17. When ready, the processor reads the 16 m.s.b. of the frequency from IC30 using CS10, and the 4 l.s.b. from buffer IC17 using CS20.

Clock signals

177. The 10 MHz input is also divided by IC8b and the resulting 5 MHz directly supplies the internal operating frequency for microprocessor IC32 as well as providing the clock input for a number of counters.

CLK TIK signal

178. The 2 MHz is counted by a ÷20,000 section of IC30 to produce the 10 ms CLK TIK interrupts. This function is required by a suite of software referred to as the executive. One of the routines within the executive is capable, by means of CLK TIK, of delaying the execution of a task for any multiple of 10 ms. Other routines organize the tasks into two queues of high and low priority. When all high priority tasks have been executed the executive will continue with any low priority tasks that may be queued. At

any point throughout this procedure, high or low priority tasks may be transferred from the delay queue to the end of the respective priority queue to await execution.

BAUD RATE CLOCK signal

179. The 5 MHz clock signal is successively divided by 2 by IC9a and IC10a then divided by 8 by IC10b and the resulting 156.2 kHz provides the BAUD RATE CLOCK for the USART IC11.

Non-linear sweep generator

180. This provides compensation for the non-linearity of the l.f. master, h.f. master and interpolation voltage controlled oscillators' frequency/voltage characteristics. The generator consists of 3 counter sections of IC30. The first section varies the correction gradient, the second provides an adjustment for the different sweep speeds while the third stores the number of clock periods to the next gradient change. This correction process is heavily dependent on software in association with INT 6.5. On the occurrence of this interrupt, signalling a breakpoint, the gradient is changed in Section one and the number of clock periods in Section three is adjusted in accordance with the stored voltage/frequency characteristic. Output from the second section is taken via t.t.l. driver TR3 to form the variable SWEEP CLOCK signal. This is fed to the D-A converter on AB1 so supplying a compensating non-linear sweep to the oscillators.

Display presentation/frequency mask counter

181. Counter Section 5 of IC30 is preprogrammed to interrupt the processor via INT 7.5 on any one or more of the 503 ordinates on the forward scan of the display. The counter enables accurate marker and negative start frequency adjustments to be made. For the latter purpose, the digital techniques used allow the generation of pseudo negative sweep frequencies. This facility is used for starting and stopping the sweeps when the instrument's frequency range is exceeded as well as for monitoring certain marker functions. It also allows a symmetrical display of the zero frequency point.

Sweep latches

182. Bus data from 8-bit latch IC29 provides a number of control signals. One output controls the sine wave calibration switch on AD4 while another, on the SERIAL DATA OUTPUT ENABLE line, enables the tri-state buffers on AR1. A third output supplies the LOW POWER STANDBY signal to power supply interface AR2, while also providing write protection for the EAROMs. A fourth opens gate IC48a to the AD2 SWEEP TRIG signal which is asserted low on the occurrence of a trigger pulse. Besides causing an RST 5.5 interrupt it enables a further, 4-bit, latch IC28. One output from this latch, DISPLAY INHIBIT, is used to reset the PISOs supplying the display data on AD2. Two further outputs provide counter start signals for IC30.

Microprocessor

183. Central processor IC32 is an 8-bit Intel 8085A which uses a multiplexed data bus to accommodate the 16-bit address. This is split between the 8-bit address bus and the 8-bit data bus. Output lines A8 to A15 carry the high order memory or input/output (I/O) address. Input/output lines AD0 to AD7 carry the low order memory or I/O address during the first clock cycle, and then carry data during the second and third machine state clock cycles. ALE (address latch enable) is used to differentiate between data and address; when it is taken high the contents of the data bus are treated as part of the address and latched out from IC34. IO/M is used to differentiate between an I/O and a memory address; when it is taken low the on-board memory is addressed. WR (write) and RD (read) asserted low enable the memory or I/O device selected by the address bus to be written into or read out from respectively. They also indicate that the data bus is available for the data transfer operation. X1 has a 5 MHz input which is divided internally by 2 to give the internal operating frequency.

184. The 8085A has 5 interrupt inputs : in ascending priority these are INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP (unused). Interrupt request line INTR is connected to the master interrupt controller IC13. When an interrupt occurs on the RST lines the start address of the service routine is pointed to by the vector stored at the location which is 8 times the RST value, e.g. for RST 7.5 the vector is stored at 3C hexadecimal (60 decimal). For an interrupt on the INTR input, the processor asserts INTA (interrupt acknowledge) low to the interrupt controller as well as to enable buffer IC35, in order to obtain the service routine address on the data bus.

Interrupt controllers

185. The master IC13 and the slave IC12 each manage up to 8 interrupt requests on lines IR0 to IR7. Interrupts are then asserted on the INT lines; to the master from the slave, to the processor from the master. At initialization, IC12 and IC13 are enabled by chip select lines CS02 and CS00 respectively and, in conjunction with command select line A0, WR (write) is asserted low to allow the initialization commands to be written in on the data bus. Amongst its other functions the command configures the interrupt priority levels so that IR0 has the highest, and IR7 has the lowest, priority. At a later stage, RD (read) may be asserted low to read the status and then WR asserted to change the priorities or to mask off an interrupt request line.

186. When slave IC12 receives an edge-triggered interrupt request on one of its IR lines, it sends an interrupt request to the IR7 input of the master Programmable Interrupt Controller (PIC). Unless engaged with a higher priority interrupt, IC13 passes on the interrupt request to the INTA input of the processor. At this, IC32 completes its current instruction then acknowledges the interrupt by sending a low INT pulse. This sets buffer IC35 for data input and is applied to both PICs. On receipt, the master PIC addresses the slave using the CAS0-2 lines while sending a call instruction back to the processor. When it is received, the processor sends two further INTA pulses which enable the slave to release its preprogrammed address onto the data bus in the order low byte, high byte. The address contains a pointer to the area in memory holding the routine to service the interrupt.

Communication interface

187. IC11 is a USART (universal synchronous/asynchronous receiver/transmitter) operating at 9600 baud and performing asynchronous data control between r.f. and display units. It accepts data from the processor in parallel format and converts it into a serial stream for transmission to the display unit. Simultaneously, it can receive data from the display unit and convert it into parallel data for the processor. It is interrupt driven and signals to the processor whenever it can accept a new character for transmission or whenever it has received a character from the processor. The processor can read the status of the USART at any time.

Operation

188. At initialization, processor IC32 addresses IC11 by taking chip select line CS04 low then sets the control/data (C/D) line high and the write (WR) line low to send a set of control words on the data bus. These define the operating format. Subsequently, a high RESET pulse can force the USART into an idle state to enable a new set of control words to be written in.

189. Serial data is clocked in and out of IC11 at the 9600 Baud rate derived from the 156.25 kHz input to pin 9. Serial input data is assembled in a receive buffer within the IC and, when the character is complete, RXRDY pin 14 takes the IR1 line high to master interrupt controller IC12 to request a processor interrupt. If, however, the assembled character is a Break instruction, it is BD pin 16 instead which requests the interrupt on the lower priority IR2 line. When ready to read the character, the processor addresses the USART using the CS04 line, then takes C/D and RD (read) low and accepts the data on the data bus.

190. When able to accept a character from the processor for onward transmission to the display unit, the USART takes TXRDY pin 15 high to request an interrupt on the highest priority (IR0) line to IC13. When ready with a character, the processor places the data on the bus, addresses the USART on the CS04 line, then takes the C/D and WR lines low. The character is accepted by a transmit buffer within the IC and then serially clocked out on the TX line to the display unit.

Memory banks

191. The operating program is contained in EPROMs (ultra-violet erasable programmable read only memory) IC39 to IC42 which provide a total of 56 K-bytes of memory. These are enabled by IC38 which decodes A14 and A15 of the address bus and is itself disabled by the IO/M line going high.

192. IC20 and IC21 each contain 2 K-bytes of RAM (random access memory) used for scratch-pad read/write operations. When the instrument is switched off the contents of these memories are lost. In the same bank are EAROMs (electrically alterable PROMs) IC22 and IC23 each of which also holds 2 K bytes of memory. These store the current instrument settings which are then remembered when the instrument is switched on again. The entire memory bank is enabled by IC18 which decodes A11 to A13 of the address bus. The decoder is enabled when IO/M is low and A14, A15 are high. To prevent corruption of the memory contents, write enable for the EAROMs is gated by IC46d under the control of monostable IC24a. When a write operation is completed, either RDY output going low causes a processor interrupt.

Data direction control

193. The direction of data flow between the microprocessor data bus and the quiet data bus is controlled by two-way buffer IC14. This is enabled only when the A5 and IO/M lines are both high. Data direction is determined by the logic state of the RD line; for a read operation this line is taken low.

Chip select decoding

194. IC36 is the master decoder providing the low enable signals for the chip select decoders. When enabled by the IO/M line being high and address lines A6 and A7 being low it decodes the A3 to A5 lines to produce 7 outputs. Two of these enable IC19a and b which decode address lines A1 and A2. The remaining decoders ICs 2,3,7,15 and 37 decode lines A0 to A2, and since their chip select outputs involve read/write operations they are additionally enabled by the RD + WR line.

Board AF1 - Front panel keyboard

Circuit diagram : Chap. 7. Fig. 47

195. The front panel circuit is mainly a static encoder for the 46 push-buttons which are arranged at the nodes of the 8 x 8 matrix. The code used to represent each button is derived from its node address; columns are numbered 0 to 7 and rows are numbered 8 to F hexadecimal. The code used to represent each button is derived from its node address, as an example the LOG button is coded C2H. Columns feed directly to decoder IC3 while rows feed to decoder IC4 via the 9 elements of ICs 1 and 2. With no buttons pressed, all the comparators' inverting inputs are held low by the elements of R2 connected to ground, while the non-inverting inputs are held slightly high by the potential divider formed by R3, R4. Consequently, the inputs to row decoder IC4 are held high as are all the inputs to column decoder IC3 due to the action of pull-up resistors R1. When a button is pressed, it shorts together a row and column of the matrix. This forms a potential divider from the respective elements of R1 and R2 causing the appropriate input lines to be taken low to the decoders. These are 8 to 3 line decoders with IC3 and IC4 supplying the l.s.b's and m.s.b's of the button address respectively. Due to IC3 pin 5 being tied to ground, any input going low causes pin 14 also to go low and this feature is used to generate KEY PRESSED to AF2 for key debounce purposes. The PRESET button does not form part of the matrix but instead is connected to cross-coupled gate bistable, IC5.

196. The l.e.d's installed in many of the push-buttons have their anodes connected to the +5 supply and their cathodes separately driven via selection logic from AF2.

Board AF2 - Front panel logic

Circuit diagrams : Chap. 7, Figs. 48 & 49

Sweep speed control

197. When the SPAN DIV control is turned, it alternately makes and breaks with contacts on shaft encoder board AZ2. When it makes, it connects the ground on tag 1 AF2 to one of the 3 lines to IC7 pulling it low; When it breaks, all lines are taken high by pull-up resistors R1 to R3. Pin 5 of the 8 to 3 line decoder IC7 is tied to ground to enable the IC to detect when all the inputs

are high. This occurs with the break condition which signals a SPAN DIV change, and pin 15 is taken low to initiate a processor interrupt. To prevent interrupts due to multiple contact closures the output from pin 15 is first of all taken to the debounce circuit formed by ICs 9 and 15.

198. The negative-going edge of the break signal to pin 1, IC9a triggers the monostable which produces a 500 µs negative-going pulse from pin 4. Bistable IC15a is clocked by the trailing edge of the pulse and its output pin 5 follows the IC7 low output. This sets IC15b pin 6 low as well as clocking IC9b pin 9. The latter action resets the IC to enable it to respond to the rising edge occurring at the end of the break signal when the new SPAN DIV setting is selected. When this occurs at pin 10 of IC9b, the monostable produces a 2 ms negative pulse. The rising edge at the end of the pulse clocks IC15b which takes pin 6 high so producing the required single rising edge on the HZ/DIV line to cause an interrupt.

199. As a result of the interrupt request, the processor takes chip select line CS47 low to read the data from buffer IC6. By comparison with the previous shaft position data the processor determines the direction of rotation of the SPAN DIV control and takes the appropriate action.

MOVE and REF LEVEL controls

200. The direction detectors for the MOVE and REF LEVEL variable controls both operate in a similar manner and each receives quadrature inputs from a shaft encoding board AZ1. The detectors produce pulses on one of two output lines depending upon the direction in which the shaft is turning.

201. The following explanation is for the MARKER direction detector but the principle applies to both detectors. The output pulse trains from the encoder arrive at IC14b: let them be X to pin 4 and Y to pin 5. Y is used as the reference phase and is also connected to IC14a pins 1 and 2. When an edge occurs due to movement of the control, a delay is caused by R6 and C6 so that pins 1 and 2 are momentarily logically opposite. The trailing edge of the resulting narrow pulse triggers monostable IC13a whose output on pin 13 enables IC11c and IC12b with a window pulse of about 2 µs duration. If X leads Y, then IC14 pin 6 will always be low during the window period, and negative-going pulses will appear at output pin 6 of IC12. Conversely, if X lags Y, IC14 pin 6 will always be high during the window period, and negative-going pulses will appear at output pin 8 of IC11. The pulses from IC11c and IC12b will have the same duration as the window pulse but at twice the frequency of X and Y. The output of IC11c is used as MARKER DOWN (IR6), and that of IC12b as MARKER UP (IR5), when they are sent to the interrupt controller. An example of operation is shown in Fig. 9.

Keypad

202. When a push-button on front panel keyboard AF1 is pressed, the inputs to AF2 consist of a negative-going signal on the KEY PRESSED line and the push-button identity on lines KD0 to KD6. The former signal is taken to the keypad interrupt debounce circuit while the latter is applied to latch IC1. The debounce circuit comprises dual multivibrator monostable IC10 and dual bistable IC8 and operates in a similar way to the HZ/DIV debounce circuit described under Sweep speed control. Here however, the delay introduced when the key is depressed (make) is 5 ms and when released (break) is 20 ms. When KEY ON goes high to cause an interrupt, it also clocks IC1 which latches in the key identity. In response to the interrupt, the processor takes CS43 low to enable the IC1 tristate outputs to be placed on the data bus. After

reading the identity of the key being pressed, the processor will also take one of the chip select lines CS42 to CS46 high to clock out the l.e.d. illuminating data if appropriate. KEY OFF also causes an interrupt; its main purpose is for use with the INTMD IDENT key when the processor inserts a 3 dB pad for the period during which the key is held depressed.

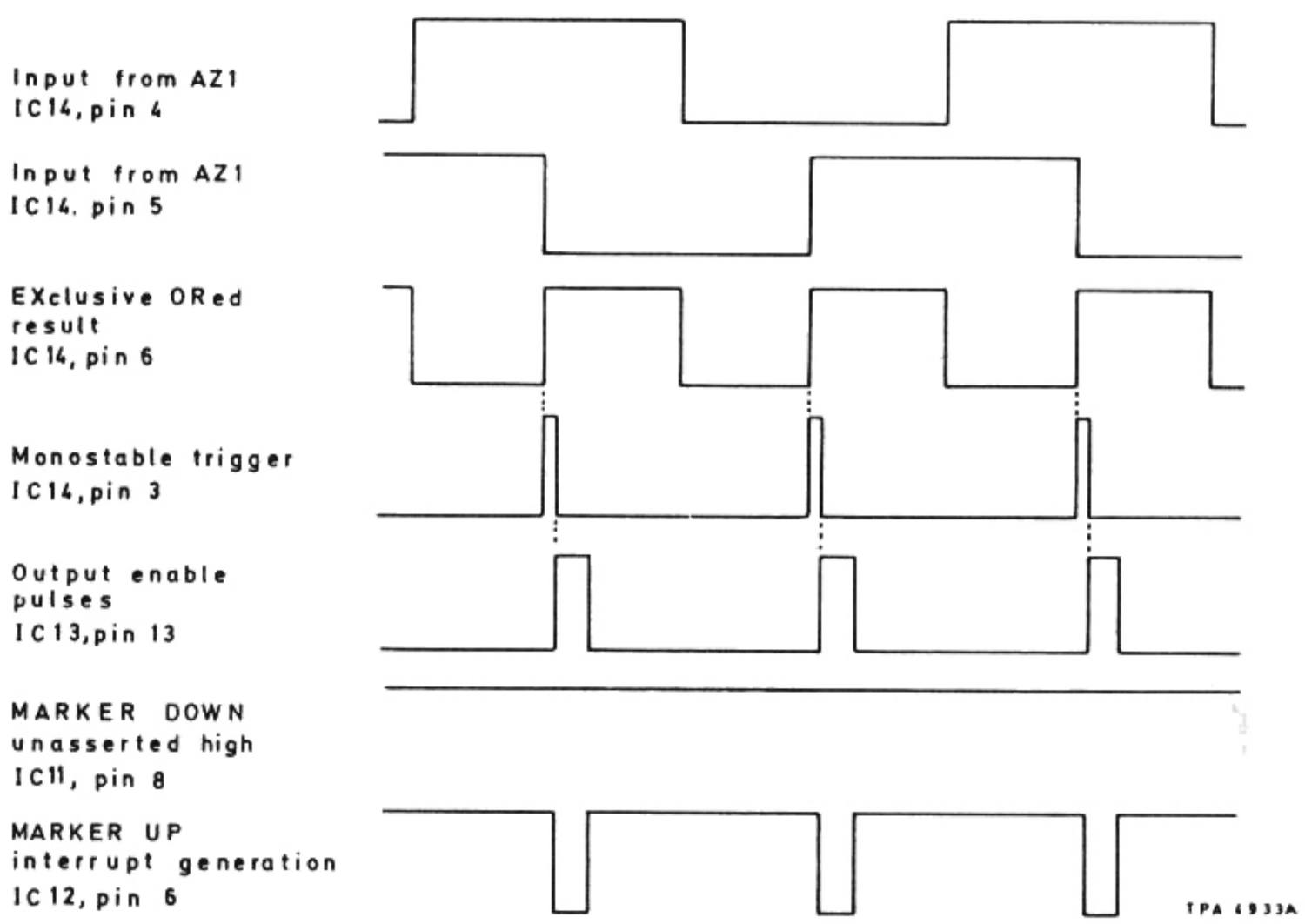


Fig. 9 MARKER direction detector operation. Example shows up movement - AF2

Board AR1 - Signal interface

Circuit diagram : Chap. 7, Fig. 51

Unit address

203. The three UNIT ADDRESS lines from input socket SKS carry the r.f. unit address. At the display unit these lines are earthed, setting the address of the first, top, r.f. unit to zero. The address is fed out from PLA to the

status buffer on AD3 as well as to the unit address incrementer IC1. This is a full adder which adds 1 from the high logic level on pin 6 to the address passed out from SKT to the next lower unit. By this means, each subsequent unit, up to a further 7, is identified by an incremented address.

Data transfer

204. Serial data from the USART on the TX line is used to control the operation of switch TR1. In the absence of data the transistor is held switched on by pull-up resistor R6 and current, limited by R4, is fed to the input of opto-coupler IC5. The data modulates the 20 mA TRANSMIT CURRENT LOOP to the RS232 interface in the display unit. Data from the display unit similarly modulates the RECEIVE CURRENT LOOP and the serial data on the RX line from opto-coupler IC4 is fed at t.t.l. levels to processor board AD3. The lowest r.f. unit links SKT 7 and 8 and SKT 9 and 10 together to complete the loop.

Display data

205. Display data from the PISOs on AD2 on the SERIAL DATA line and synchronizing pulses on the SERIAL DATA SYNC line are fed through tristates IC2a and IC2b to the display unit when enabled by DATA OUTPUT ENABLE from AD3. The 5 MHz line, when enabled, supplies the master clock signal which synchronizes the display to the data.

External standard

206. If an external standard is connected to the rear panel EXT STD socket, calibrator board AD4 sets the EXT STD line low to AR1. Providing the r.f. unit is the active one, DATA OUTPUT ENABLE causes tristate IC2d to gate out the low to AND-gate IC3a. IC3a output flags EXT STD low either to the display unit or to SKT 19 of an intervening r.f. unit which then passes the signal on. The EXT STD flag is negated by IC3a, if the unit is not the active one, or is the active one and no external standard is connected. This is achieved by the pull-up resistors on AR1 on each r.f. unit plus SKT 19 being held high on the lowest powered r.f unit.

Board AR2 - Power supply interface

Circuit diagram : Chap. 7, Fig. 52

207. The power supply interface in each r.f. unit has its supply lines so configured that power from the display unit can be used to supply no more than two r.f. units. For example, the +20 V line is connected from the display unit to input sockets SKP31 and SKP13. SKP31 provides power for the 2382 containing the interface while SKP13 passes on the power to output socket SKR31. SKR31 supplies power to a second r.f. unit, but since output socket SKR13 has no connection (unlike the input sockets to the first interface which are linked by the display unit) power cannot be passed on.

208. The -14.5 V power supply from the display unit is linked back by the interface so that the removal of an r.f. unit causes an automatic display unit power supply shutdown. This prevents an otherwise unloaded 2380 from causing overvoltage conditions at the time of reconnection to an r.f. unit.

Line cleaner

209. The purpose of the line cleaner IC4b, TR1 is to remove any low frequency a.c. component occurring on the +5 V d.c. supply line. The principle of operation is that any detected change in current on the supply line causes an equal amount of current to be drawn from or fed to the line in compensation. Current is constantly drawn from the supply and sunk by R14 and any change in the supply causes the standing current to change accordingly. Resistors R12 and R13 form a potential divider whose junction maintains the charge on C12 which provides the reference for IC4b. IC4b is a differential amplifier which controls the conduction of TR1. Due to the large time constant of C12 and R11, only long term changes of current through R11, e.g. due to temperature changes, affect the stored reference causing C12 to restore TR1 conduction to the correct value. At switch-on, D7 enables C12 to quickly attain the reference level. D8 provides protection against a TR1 base-emitter reverse bias. In operation an increase, for example, of voltage on the supply line is detected by R10 causing the inverted output of IC4b to go more negative. This increases the conduction of p.n.p. TR1 which bleeds away the extra current so restoring the supply to its original level.

Voltage regulators

210. The board contains three voltage regulators, these supply +15 V, -15 V and -5.5 V from the +20 V, -20 V and -8.5 V lines respectively from the display unit. The regulators are similarly configured. Each has a low-pass filter at the input, diodes to protect against reverse transients and a means of output voltage setting by a preset resistor. The latter forms part of a potential divider used by the regulator to sense output voltage variations.

Frequency standard adjustment

211. The rear panel SET INT STD potentiometer (with combined on/off switch) is connected between +15 V supplied by AR2, and ground. When the internal standard is adjusted, potentiometer output adjusts a varactor diode on AD4 which controls the 10 MHz TCXO. The switch is ganged with another which connects to ground to assert a low to the processor on AD3 to signal internal standard adjustment. When the switch is open, a pull-up resistor on AR1 takes the line high.

Audio amplifier

212. Audio from log. amp. interface board AD2 is controlled by the rear panel VOL potentiometer connected to the AR2 amplifier IC4a. This provides a gain of approximately 6 and the output is fed to the rear panel PHONES jack or to the nearby loudspeaker. When, during frequency sweeps, AUDIO MUTE is asserted high from AD2, TR2 is switched on to disable the audio input to the amplifier.

Temperature sensor and fan speed controller

213. The instrument temperature sensing thermistor on AA11 is connected to the +15.5 V rail and forms a potential divider with R18 which is connected to the -15.5 V rail. The divider mid-point is connected to the base of TR3 as well as providing the input to comparators IC5a and IC5b. At 20°C the resistance of the thermistor is equal to that of R18 and the zero potential holds TR3 off while the current for the cooling fan is supplied via D10. If the temperature rises, the thermistor resistance decreases so that the divider mid-point goes positive. This forward biases TR3 which switches on, reverse biasing D10 and supplying an increased current to the fan to increase its speed. If the temperature, and hence the sensed voltage, rises sufficiently, IC5b output goes low to the processor via the HOT line on AR1. The processor then displays a warning message to the user. If the temperature continues to rise, IC5a output goes low on the CUT OUT line to the processor and r.f. unit. The upper display unit disconnects the power supply to the lower unit. Diode D11 prevents the mid-point voltage from falling below -0.4 V in order to protect the inverting inputs to the comparators.

Low power operation

214. The display unit can supply power to two r.f. units, one of which is on standby. To switch the unit to standby, the processor takes the LOW POWER STANDBY line low which switches on TR7 and TR6. This causes 1.2 V from TR5 to be applied to the VADJ inputs of regulators IC1 and IC2. Since the negative regulators maintain VOUT at 1.2 V lower than VADJ, the -15 V and -5.5 V outputs both change to 0 V. In addition, switching of these supplies respectively disables the +15 V and +70 V regulators on AB1. With the -15 V supply switched off, TR4 in turn switches on which applies 0 V to VADJ of IC3 causing the output to drop from +15 V to approximately +1.2 V. The +5 V regulator continues operation which together with the +14.5 V from the display unit supplying the 50 MHz oscillator on AC1, ensures that processor clock operation is maintained during standby.

Board AZ1 - Optical encoder

Circuit diagram : Chap. 7, Fig. 53

215. This is one of two similar boards which form part of the variable REF LEVEL and MOVE controls. The board function is to indicate the direction of movement of the shaft of the control to board AF2. Power is supplied from AF2 on contacts 1 and 3 to two l.e.d's. These are optically coupled via a pierced disk mounted on the shaft to photo-detectors connected to contacts 4 and 5. By this means, as the shaft is rotated, quadrature pulses are generated for subsequent decoding on board AF2 to determine the direction and rate of movement of the control.

Board AZ2 - Span switch

Circuit diagram : Chap. 7, Fig. 54

216. This board forms part of the SPAN/DIV variable control. Its function is to indicate the direction of movement of the shaft of the control to AF2. As the shaft is turned, it alternately makes and breaks with contacts 3,4 and 5. When it makes, it applies a low from contact 1 to the connected output contact. When it breaks, a high is applied on the line by a pull-up resistor on AF2. The sequence and frequency at which the low pulses occur enable board AF2 to determine the direction and rate of movement of the control.

TRACKING GENERATOR (OPTIONAL)

217. A 5 MHz input from board AC6 is divided by 25 in AE1 and the resulting 200 kHz is used to switch a sampling gate in order to phase lock the 47.4 MHz crystal oscillator to the frequency standard (see Fig. 10). Oscillator output is fed via an amplifier controlled by the a.g.c. line from the AE6. The input is mixed on AE3 with 550 MHz from AA9 - applied via isolating amplifier board AE2 - and the resulting 502.6 MHz is selected by band-pass filter AE3. The signal is next mixed on AE5 with a 498.6 to 906.6 MHz input from the synthesizer applied via isolating amplifier board AE4. The following low-pass filter selects the difference frequency in the range 100 Hz to 400 MHz and this is fed to the 21 dB amplifier on AE6.

218. Selection logic from AB1 operates the switches on AE6 and AE7 to provide either a tracking generator output to the TRACKING GENERATOR socket or a calibrated output for the signal path. Levelling detectors follow which provide a constant output irrespective of frequency to sample and hold gates. These are operated by a pulse generator and logic from AB1 so as to select the required signal for gain control of the input amplifier on AC1. The tracking generator output level may be adjusted by the REF LEVEL variable control when TRACK GEN is selected.

Board AE1 - 47.4 MHz xtal oscillator

Circuit diagram : Chap. 7, Fig. 41

219. The 47.4 MHz v.c.o. is a Colpitts oscillator TR1 which uses a third overtone crystal XL1 in its series resonant mode. Fine tuning is set by L1 and controlled by varactor diode D1. Oscillator output from TR2 is buffered by TR3 and applied to a sampling gate which is used to phaselock the oscillator to the frequency standard. The 5 MHz standard from AC6 is divided by 25 by IC1 and the resulting 200 kHz is fed to the pulse generator. This consists of TR4 driving a step recovery diode comb generator via an impedance matching transformer T1. Diode D6 output is shaped by L3, L4 and D7 into two antiphase pulses which are used to switch the sampling gate formed by D2 to D5. Buffer TR3 prevents the 200 kHz from the pulse generator getting into the oscillator circuit. Error signal output is fed through amplifier IC2 and loop filter C22, R36 to the cathode of varactor diode D1.

220. Oscillator output from TR2 is fed to amplifier TR5 whose gain is controlled from AE6. As the voltage on the GAIN CONTROL line is adjusted, the effective value of TR5 emitter resistance is changed by the variable resistance of the pin diodes D9 to D11. To provide shaping of the characteristic each diode is progressively switched in as the voltage is increased. Output to mixer board AE3a at 47.4 MHz in the range -1 to -19 dBm is used to keep the tracking generator output constant.

Board AE2 - Buffer

Circuit diagram : Chap. 7, Fig. 42

221. This board contains a 20 dB attenuator and an isolating amplifier. TR1 and TR2 amplify the 550 MHz input from the second l.o. by 10 dB as well as providing 60 dB of isolation. Output at -8 dBm is fed to mixer board AE3a.

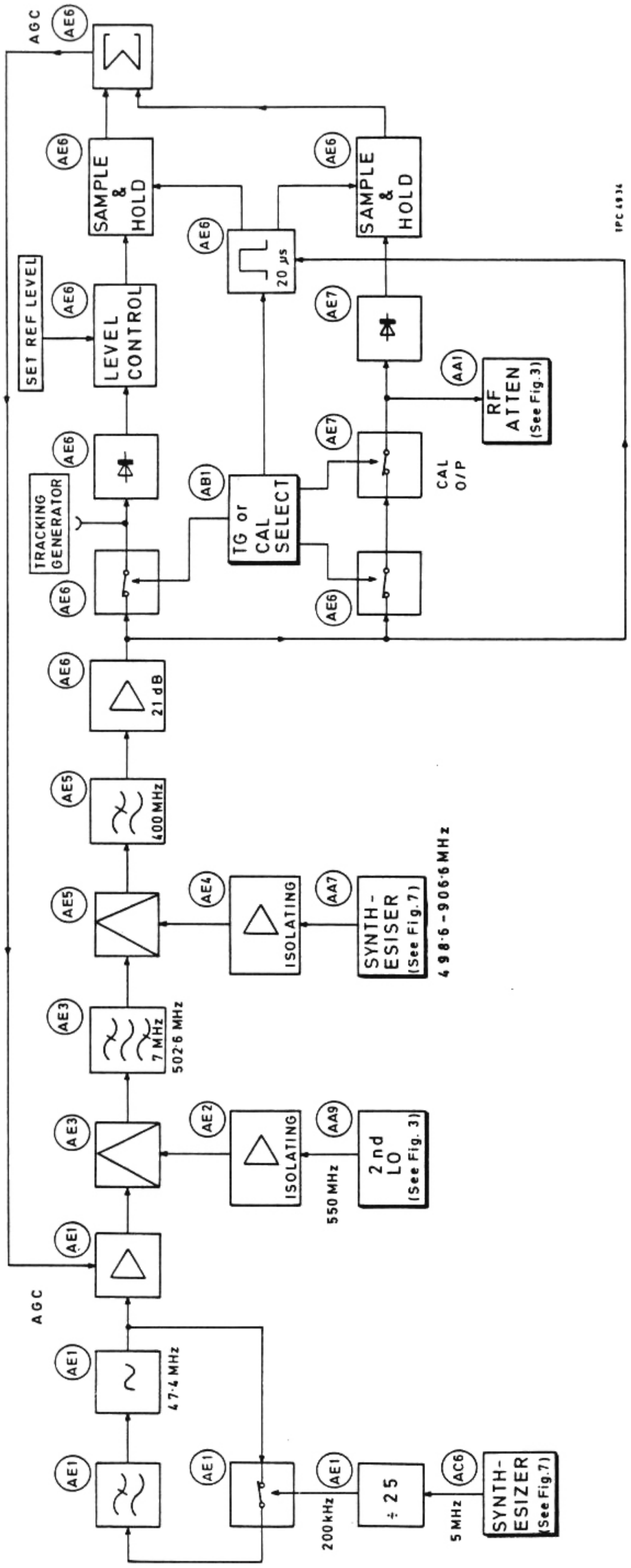


Fig. 10 Tracking generator block diagram showing main functions of boards

Unit AE3 - Bandpass filter &
Board AE3a - Narrow band mix/buff

Circuit diagram : Chap. 7, Fig. 42

222. The 47.4 MHz input from the gain-controlled amplifier on AE1 is connected via matching network L4, C8 to one of the gates of f.e.t. mixer TR3. A second board input, at 550 MHz, is from AE2 and this is fed in to the high level buffer formed by TR1 and TR2. The buffer and the isolating amplifier on AE2 provide a total tracking generator isolation of 120 dB. Buffer output at approximately 10 V p-p is passed via matching network L3, C5 to the second gate of mixer TR3. After the mixing process, the difference frequency of 502.6 MHz is selected by the bandpass filter AE3 and connected to the output mixer on AE4.

Board AE4 - TG buffer

Circuit diagram : Chap. 6, Fig. 43

223. This board contains the amplifier formed by TR1 and TR2 which amplifies the 498.6 to 906.6 MHz input from the slave v.c.o. by 10 dB as well as providing 60 dB of isolation. Output at 0 dBm is fed to mixer board AE5a.

Unit AE5 - Output low level filter &
Board AE5a - Wideband mix/buff

Circuit diagram : Chap. 7, Fig. 43

224. The 502.6 MHz input from the band-pass filter AE3 is connected via matching network C10, C11 to buffer amplifier TR7. This provides one of the inputs to the mixer XM1. A second board input, at 0 dBm in the range 498.6 - 906.6 MHz, is from AE4 and this is fed in to the isolating amplifier formed by TR1 and TR2. Total tracking generator isolation of this amplifier and the one on AE4 is 120 dBm. TR4 is biased via TR3 and provides the high level drive for the following class 2 double balanced mixer XM1. Total gain of TR1 to TR4 is 17 dB. The difference frequency from the mixer in the range 100 Hz to 400 MHz is selected by the low-pass filter on AE5 for passing out to the 21 dB amplifier on AE6.

Board AE6 - Amp/leveller

Circuit diagrams : Chap. 7, Figs. 44 & 45

Amplifier

225. The 21 dB amplifier consists of three d.c. coupled stages TR1, TR2 and TR3. Zener diodes D31 to D33 are level shifters used to set the operating point for each stage. Feedback for stabilizing purposes is fed through IC1 to the emitter of TR1. When LF CUT is unasserted low on the SET LF RESPONSE line, TR4 switches on to add the value of C2 to that of C1 to extend amplifier response down to 100 Hz. When TR4 is switched off on wide sweeps, amplifier response is reduced to 10 kHz in order to minimize unwanted low frequencies. HF response is peaked by C8.

Tracking generator

Output switch

226. When the tracking generator output is selected, SET TG OFF and SELECT CAL are both unasserted high. This causes a low from NAND-gate IC12c to be applied to the inverting input of IC5a and the non-inverting input of IC5b. The comparator outputs reverse bias D1 and D3 and forward bias D5 to D8. The forward biased pin diode bridge allows the amplifier output to be fed via a 2 dB pad to the TG levelling detector. When, instead the calibrator output is selected, D5 to D8 are reverse biased so blocking the signal path, while grounding diodes D1 and D3 are forward biased providing a total isolation of 60 dB. The addition of the 2 dB pad to the 2 dB of the switch insertion loss provides equality with the 4 dB insertion loss of the calibrator signal path.

Levelling detector

227. The signal from the output switch is detected by D10 and charges reservoir capacitor C28 negatively. Diode offset voltage compensation is provided by D11 in the feedback path of unity gain amplifier IC6a. For optimum detector efficiency, d.c. bias is supplied from integrating capacitor C33 and fed via R40 to the detector diode D10 and via R42 to compensating diode D11. Bias is in the form of a constant current due to the high values of R40 and R42. Variation of the bias alters the charging rate of C28 and modifies the detector time constant. For frequencies down to 1 kHz, bias derived from +5 V across C33 is at the maximum of 2.3 µA, below 1 kHz bias decreases in direct ratio with decreasing frequency (e.g. at 100 Hz bias is 0.23 µA). Below 1 kHz therefore, the detector ripple is maintained constant due to the increasing detector time constant. To provide temperature compensation, diodes D10 and D11, which are a matched pair, are mounted close together. D9 balances the circuit to minimize distortion due to detector action.

Level control

228. Tracking generator output level is controlled by the voltage on the TG LEVEL CONTROL line fed to comparator IC6b which has a gain of 21. The voltage is adjusted by the front panel REF LEVEL variable control when TRACK GEN is selected. When the voltage on the control line is 10 V output at the TRACKING GENERATOR socket is maximum, and when it is 0 V the output is minimum. Range limits are -10 dBm and -20 dBm with overrange, and are preset by R50 and R55 respectively. Comparator output feeds to a sample and hold circuit formed by f.e.t. switch IC2a and hold capacitor C54. R47 in conjunction with sampling gate and hold capacitor C54 determine the loop bandwidth of the tracking generator AGC loop. Loop bandwidth decreases with decreasing signal frequency below 50 kHz and ensures overall loop stability. TR10 changes the levelling loop time constant for sweeps above 3 kHz. For frequencies above 50 kHz, the 20 µs sampling period causes the switch to be continuously closed. Voltage follower IC3a feeds the sampled signal to summing amplifier IC3c and out via IC3d to control the gain-controlled amplifier on board AE1. D26 and D27 ensure that IC3d output is always negative.

Calibrator

Output switch

229. When the calibrator output is selected, the low on the SELECT CAL line is applied to the inverting input of IC5c and the non-inverting input of IC5d. The comparators forward bias the pin diodes D17 to D20 and enable the amplifier output to pass to a second similar diode switch on board AE7. Total isolation of the two switches is 120 dB. Here, the signal is detected in the same manner as for the tracking generator signal before being passed back to IC4b on AE6.

Output

230. Calibrator signal output level is preset by R60 which supplies the reference for comparator IC4b. This supplies a gain of 21 before the signal is fed to the sample and hold circuit formed by IC2c, C55 and R70. For frequencies below 50 kHz, f.e.t. switch IC2c is closed for a 20 µs sampling period to charge hold capacitor C55. For higher frequencies, the switch is continuously closed. R70 restricts overall loop bandwidth. Voltage follower IC3b feeds the signal to summing amplifier IC3c to control the gain-controlled amplifier on board AE1. Calibrator output level is -10 dBm.

Frequency conscious switch

231. The 21 dB amplifier output is a.c. coupled to squarer TR8 and TR7 which produces an inverted t.t.l. compatible square wave that takes two paths, one of them to the frequency conscious switch. The low-pass filter at the switch input ensures that the circuit only passes frequencies below 2 MHz. Reservoir capacitor C47 is charged negatively through detector D21, and is connected to the inverting input of comparator IC9a. Below cut-off, the C47 stored voltage is more negative than the reference and the comparator output sits high. This reverse biases D23 so that the +5 V rail supplies a high logic level to pin 4 of Schmitt NAND IC12b, enabling normal operation. Above cut-off, the voltage on C47 is less negative than the reference and IC9a output goes low forward biasing D22 and D23 so that a low logic level is applied to the NAND gate. When this happens, or when LF CUT is asserted, IC12b pin 6 is taken high which causes IC13a to hold TR6 switched off and forces IC13d output low. R102 provides positive feedback around comparator IC9a and introduces a degree of hysteresis to the switching action.

Detector bias voltage generation

232. The square wave from TR7 is given fast transitions by Schmitt NAND-gate IC12d and fed as the clock signal to the retriggerable monostable IC10a. When triggered on the falling edge, IC10a generates a 1 ms positive pulse which is gated by IC13a to the switch TR6. For a frequency of 1 kHz and above, the monostable output is continuously high and this is inverted by the NOR-gate so holding TR6 switched off. This applies +5 V via voltage follower IC4a to reservoir capacitor C33 which supplies the bias control for the tracking generator and calibrator detectors. Below 1 kHz, the bias voltage decreases with frequency, e.g. for a frequency of 100 Hz, IC10a switches TR6 on for 9 ms and off for 1 ms and the mean level on C33, dependent on the mark/space ratio, reduces to 0.5 V. For wide sweep widths when LF CUT is asserted, or for signals above 2 MHz to the frequency conscious switch, the output from IC12b is held high to IC13a. This gates off the monostable output and keeps TR6 switched off to maintain the detector bias voltage at +5 V.

Sampling pulse generation

233. By sampling the detector output once every cycle, detector ripple which becomes significant below 10 kHz can be effectively removed. The optimum point at which to sample the input signal is in phase with the positive peak. To select this point, the positive half of the squared waveform from IC12d is phase shifted by 90° and used to trigger the monostable producing the sampling pulse (see waveform diagram, Fig. 11). When the logic level from IC11b is low, it is summed via R77 with TR9 high output level via R78 and applied to the inverting input of integrator IC9d. Since this source voltage is below that of the reference to the non-inverting input of the integrator, a positive ramp is generated for the duration of the IC12d low state. The ramp output is inverted by IC9c which has unity gain for positive inputs as D12 is then forward biased. The resulting low output holds TR9 switched off. When IC12d output goes high, both R77 and R78 are returned to a high level of +5 V and the source voltage to the integrator inverting input exceeds the reference. Component values determine that the ramp now falls at twice the rise rate. When the ramp voltage falls below zero, the inverting amplifier output goes high, D12 becomes reverse biased and the gain is increased to 23. This switches TR9 on and the collector voltage falls to a value where the integrator source voltage equals the reference voltage, so that integrator output remains at a constant level. Negative feedback from TR9 collector

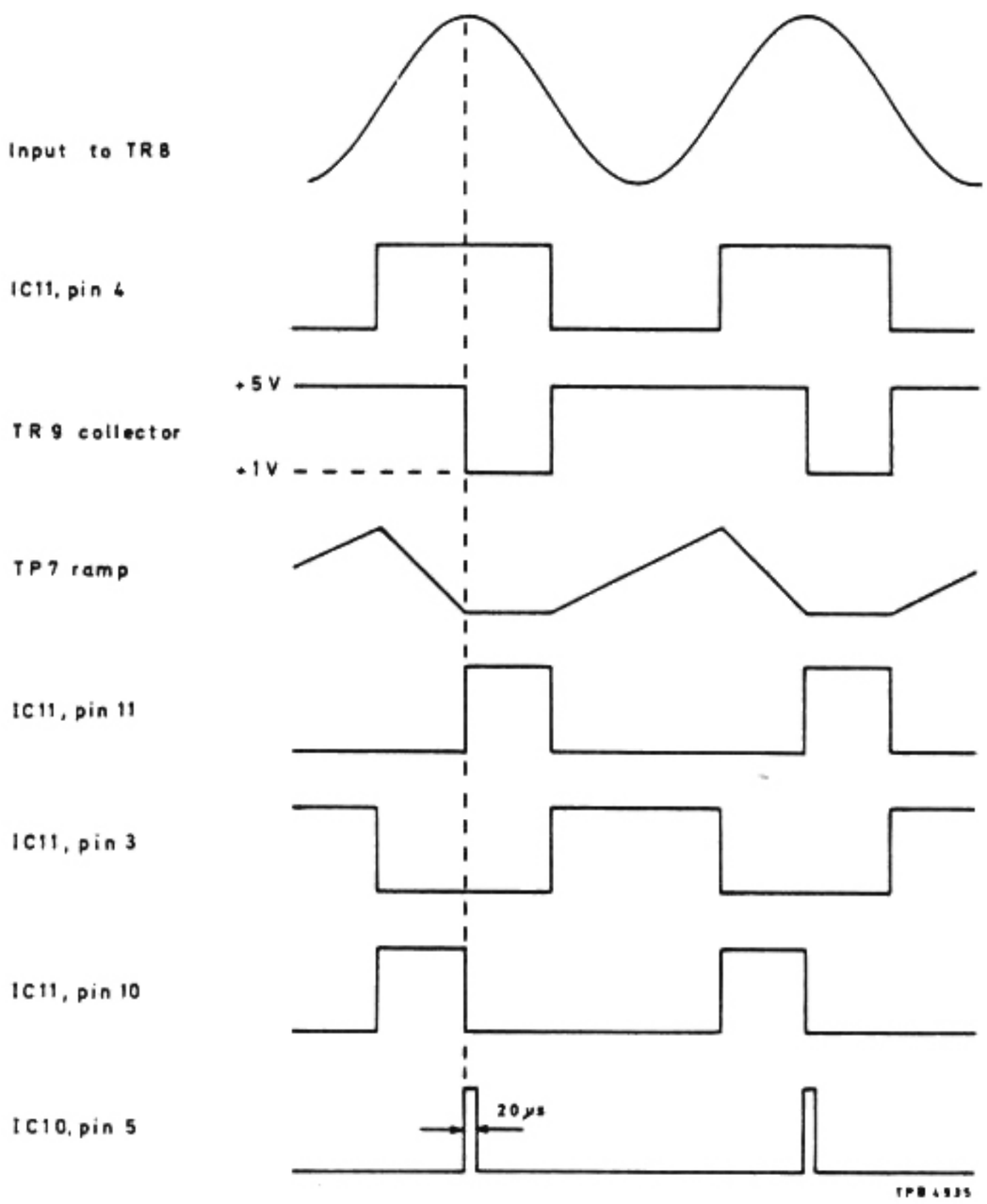


Fig. 11 Sampling gate pulse generation waveforms - AE6.

maintains this state until the sequence restarts. Switching TR9 on causes a low logic level to be applied to IC11d which, via IC11c causes a falling edge to clock monostable IC10b. A 20 µs pulse is generated by IC10b which occurs at the positive peak of the input signal as required. Providing that pin 13 of NOR-gate IC13d is low, the inverted pulse is passed out as the switching pulse to the drivers controlling the sampling f.e.t. switches forming IC2.

Output switching

234. The selection of the tracking generator output or the calibrator output on the GAIN CONTROL line is determined by processor logic on the SET TG OFF and SELECT CAL lines. The logic controls the drivers forming IC7 which operate the four f.e.t. switches forming IC2. ICs 13b and 13c gate these signals with the output from IC13d. For frequencies below 50 kHz, when LF CUT is not asserted, and either the calibrator or tracking generator output is required, the 20 µs negative pulses from the 90^0 phase shifter are gated through IC13d to operate the sampling switches IC2a or IC2c. For frequencies above 50 kHz the pulses are no longer discrete and the selected sampling gate switch is held closed. The selected switch is also held closed when LF CUT is asserted or the input to the frequency conscious switch exceeds 2 MHz. When neither output is required, sampling switches IC2a and IC2c are held open while grounding switches IC2b and IC2c are held closed. Switch selection logic is shown in Table 10.

TABLE 10 FET SWITCH SELECTION LOGIC - AE6

SET TG OFF (L)	SELECT CAL (L)	IC2 Pins 13	5	6	12
L	L	L	H	⎍	L
L	H	L	H	L	H
H	L	L	H	⎍	L
H	H	⎍	L	L	H

Board AE7 - Switch

Circuit diagrams : Chap. 7, Figs. 44 & 45

Output switch

235. When SELECT CAL is asserted low to the inverting input of comparator IC1b and to the non-inverting input of IC1a, the comparator outputs reverse bias D1 and D3 and forward bias D5 to D8. The forward biased pin diode bridge allows the signal from the similar switch on board AE6 to be fed through this switch to the input attenuator on AA1 as well as to the calibrator signal detector. Insertion loss for each switch is 2 dB. If, instead, the tracking generator output is selected, D5 to D8 are reverse biased so blocking the signal path while grounding diodes D1 to D3 are forward biased providing, with the AE6 switch, a total isolation of 120 dB.

Detector

236. The signal from the switch is detected by D10 and charges reservoir capacitor C10 negatively. Diode offset voltage compensation is provided by D12 in the feedback path of unity gain amplifier IC2. For optimum detector efficiency, d.c. bias is supplied from AE6 via R15 to the detector diode D10 and via R16 to compensating diode D12. Bias is in the form of a constant current due to the high values of R15 and R16. Variation of the bias alters the charging rate of C10 and modifies the detector time constant. For frequencies down to 1 kHz, bias is at the maximum of 2.3 µA and decreases below 1 kHz in direct ratio with decreasing frequency. Below 1 kHz therefore, the detected ripple is maintained constant due to the increasing detector time constant. To provide temperature compensation, diodes D10 and D12, which are a matched pair, are mounted close together. D9 balances the circuit to minimize distortion due to detector action. The detected signal is fed out to the level control circuit on AE6.

Chapter 5-0

MAINTENANCE

CONTENTS

Para.
1 Introduction
3 Safety precautions
8 Recommended test equipment
9 Access to trays and boards
9 Removal of outer covers
10 Access to trays
12 Access to boards
14 Removal of boards
15 Removal of front panel

Table
Page
1 Recommended test equipment 3

Fig.
1 Location of trays and boards 6

INTRODUCTION

1. This chapter provides servicing support information for the three chapters which follow:

5-1: PERFORMANCE TESTING - procedures for verifying that the equipment complies with the Performance Data in Chap. 1.

5-2: ADJUSTMENT AND CALIBRATION - tests and adjustments for restoring the equipment to peak performance.

5-3: FAULT DIAGNOSIS - procedures for localizing faults at least to sub-assembly level (normally a printed circuit board), together with information on repair and replacement.

2. In case of difficulties which cannot be resolved with the aid of this manual, please contact our Service Division at the address at the rear of the manual or your nearest Marconi Instruments representative. Always quote the type number and serial number found on the instrument data plate.

SAFETY PRECAUTIONS

3. Although this equipment has been designed and constructed in accordance with international safety standards, it is important that the advice given under NOTES AND CAUTIONS at the front of this manual should be observed in all

maintenance procedures to ensure safe working practices. In addition to these general precautions, special handling techniques are required for certain items, as below.

Chip components

4. Numerous chip capacitors and resistors are fitted in this instrument. These have silver palladium end cap terminations. When soldering these devices the following precautions should be observed.

(i) Use solder containing 3% silver, and a temperature controlled 45 W soldering iron set to 315°C (600°F). The use of a high wattage soldering iron will minimize the time taken to solder the device.

(ii) When soldering chip components to printed circuit boards a long fillet of solder should be laid on the track leading up to each end cap termination. This reduces the otherwise adverse inductive effects at high frequencies.

5. Static sensitive components. The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Take care also when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMS.

6. Bulkhead connectors and gaskets. To ensure that no r.f. leakage occurs all bulkhead connectors and lid sealing gaskets must be securely fitted. It is essential that the unit lids are correctly relocated in their slotted recesses after removal.

7. Transistor and diode checking. Transistors may be checked by measuring the electrode voltages and/or by measuring the resistance between electrodes by means of a multimeter. So that the meter voltage does not damage the transistors or diodes use the lowest voltage and the maximum source resistance available, e.g. the Ω range on the AVO 8 or the SEI Selectest Super 50.

RECOMMENDED TEST EQUIPMENT

8. The test equipment recommended for use in Chaps. 5-1, 5-2 and 5-3 is shown in Table 1. Alternative equipment may be used provided it complies with the stated minimum specification.

TABLE 1 RECOMMENDED TEST EQUIPMENT

Description	Minimum specification	Example	Use[1]
Generator	Frequency range: 5 Hz to 1 MHz Output range: -40 dBm to +10 dBm with auxiliary TTL output.	Hewlett-Packard 3325	PF
Generator (high-frequency)	Frequency range: 1 MHz to 500 MHz Output range: -40 dBm to +10 dBm	Marconi 2018A or 2019A	PAF
Oscillator	Centre frequency: 100 MHz Output level: 0 dBm Phase noise: <-90 dBc/Hz at 1 kHz Short term stability: 1 part in 10^9	HCD Research 185R	P
Variable d.c. power supply	Range: -5 V to + 12 V d.c.	Marconi 2158	F
RF amplifier	Frequency range: 1 MHz to 500 MHz Gain: 40 dB	Marconi 2177	P
Power meter	Frequency range: d.c. to 50 MHz Accuracy: ±0.01 dB	Wandel & Goltermann EPM1	PF
Power meter (high frequency)	Frequency range: 30 kHz to 500 MHz Accuracy: ±0.02 dB	Marconi 6960 & 6912 sensor	PA
Counter	Frequency range: 10 Hz to 500 MHz	Marconi 2432A	PAF
Digital multimeter	Functions: d.c. volts, resistance	Solartron 7150	AF
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235	PAF
Spectrum analyzer	Frequency range: 100 Hz to 1 GHz (with tracking generator facility)	Marconi 2370 & 2373 extender	PAF

[1] P = Performance testing A = Adjustment and calibration F = Fault location

TABLE 1 RECOMMENDED TEST EQUIPMENT (continued)

Description	Minimum specification	Example	Use
Active probe	Frequency range: 100 kHz to 1 GHz	Marconi 2388	AF
Step attenuator	60 dB in 10 dB steps	Hewlett-Packard 8495A	PF
Attenuator pads (qty. 2)	10 dB, 50 Ω, type N connectors	Marconi 6534/3	P
Power splitter	Frequency range: d.c. to 500 MHz Impedance: 50 Ω	Weinschel 1870A	P
Combiner	Frequency: 100 MHz Impedance: 50Ω	Mini-Circuits ZFSC-2-1	P
Low-pass filter	Cut-off frequency: 100 MHz Attenuation at 200 MHz: >50 dB	Telonic TCP 10048A	P
VSWR bridge	Frequency range: 10 MHz to 1 GHz	Wiltron 62N50	PAF
Termination (qty. 2)	Impedance: 50 Ω Type N connector	Weinschel 1404	P
Mismatch	470 Ω in series between type N connectors	-	P
Coaxial adapters	Type SMC female to BNC female, 50 Ω Type SMC female to N female, 50 Ω	Radiall R191123 Radiall R191147	A A
Coaxial lead	1.5 m long Impedance: 50 Ω	RG214	P

ACCESS TO TRAYS AND BOARDS

Removal of outer covers

9. To remove the top and bottom outer covers, unscrew the two retaining screws situated on the rear panel, slide each cover slightly to the rear, then lift off.

Access to trays

10. With the tracking generator fitted there are three trays. From top to bottom these are:-

IF unit	- AC0, AD0
RF units	- AA0, AB0
Tracking generator	- AE0

Of these, the centre tray is fixed in position while the tracking generator and r.f. tray are both hinged at the rear and may be opened out. This is only necessary for access to the r.f. tray or to the AC0 side of the i.f. tray or to front panel board AF2. The trays, opened out in the optional servicing position, together with their boards, are shown in Fig. 1.

11. To open out the trays proceed as follows:-

(1) Remove the knurled screw at each side of the r.f. tray.

(2) Carefully open out the tray. The tray may be locked at a right angle by inserting the previously removed screws in the holes provided next to the hinge screws.

(3) Remove the slotted head screw at each side of the tracking generator (TG) tray, slide the tray rearward in its slots and disconnect all four semi-rigid pipes.

(4) Repeat (2) above.

Access to boards

12. Most boards are protected and screened by metal lids. For access to these boards, lift off the lids after removing all retaining screws. When replacing a lid, ensure that the gasket is correctly fitted. The positions of the boards within their trays are shown in Fig. 1.

13. For identification of individual components on a board see the board layout diagrams opposite the circuit diagrams in Chap. 7.

Removal of boards

14. The boards may be removed from within the tray after unscrewing the retaining male-female hexagonal pillars and cross head screws. Take care to disconnect all flying leads, ribbon connectors and board-to-board couplers. Slide the latter from their slots after depressing their tops.

	PART No.
RF TRAY AA1	44990-423W
1a	44828-450Y
2	44990-434B
2a	44828-451N
3	44990-441H
3a	44828-452L
4	44828-453J
5	44828-454F
6	44828-455G
7	44828-456V
8	44828-457S
9	44838-458W
10	44828-459D
11	44828-460S
RF TRAY AB1	44828-462D
2	44828-463T
3	44828-464P
4	44828-465X
5	44828-466M
6	44828-467C
7	44828-468R
8	44828-469B
IF TRAY AC1	44828-472B
2	44828-473K
3	44828-474A
4	44828-475Z
5	44828-476X
6	44828-477E
IF TRAY AD1	44828-479Y
2	44828-480E
3	44828-481U
4	44828-482Y
TRACKING GEN TRAY AE1	44828-485J
2	44828-486F
3	44990-442E
3a	44828-487G
4	44828-488V
5	44990-435K
5a	44828-489S
6	44828-490G
7	44828-491V
FRONT & REAR PANELS AF1	44828-494D
2	44828-495T
AR1	44828-496P
2	44828-497X
AZ1	44828-523J
2	44828-498M

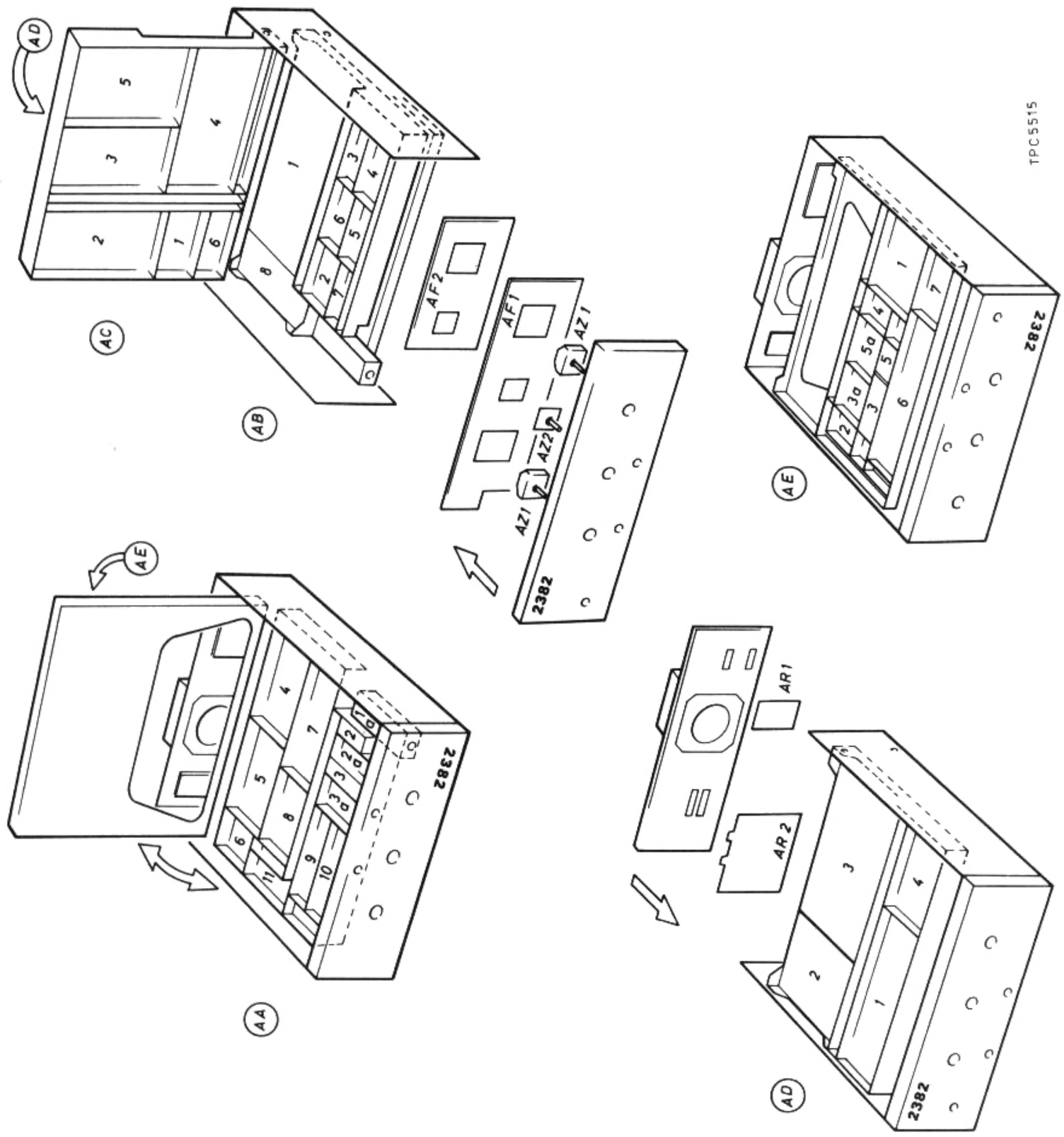


Fig. 1 Location of trays and boards, with the top and bottom trays shown opened out in the optional position

Removal of front panel

15. The front panel assembly may be removed as a unit as follows:-

(1) Stand the instrument on its rear feet and hinge down the TG tray (see 'Access to trays' above).

(2) Remove the front handle trim strips after removing the two cross headed screws. This will reveal two screws for each handle. Remove the screws and handles.

(3) Disconnect the ribbon cable from above the marker move encoder. Disconnect the two remaining cables.

(4) Release the front panel by removing the hexagonal nut (clamping the attenuator to the rear of the panel) adjacent to the probe socket.

Chapter 5-1

PERFORMANCE TESTING

CONTENTS

Para.
1 Introduction
2 Test precautions
3 Test procedures
3 Frequency span, /DIV and LOG
4 External standard input
5 Reference frequency, /DIV
6 Frequency count
7 Resolution, 1 Hz
8 Resolution bandwidths
9 Residual f.m.
10 Drift
11 Displayed noise sidebands
12 Overload protection
13 Display fidelity, dB/DIV and VOLTS/DIV
14 Amplitude accuracy
15 Frequency response
16 Input reflection coefficient
17 Local oscillator leakage
18 Harmonic distortion
19 Non-harmonic distortion
20 Third order intermodulation
21 Residual responses
22 Input noise sensitivity
23 Tracking generator cross-coupling
24 External trigger source
25 FM demod display accuracy
26 Tracking generator frequency accuracy
27 Tracking generator frequency response
28 Tracking generator amplitude setting
29 Tracking generator distortion
30 Tracking generator return loss
31 Standard 10 MHz output frequency
32 Standard 10 MHz output amplitude
33 47.4 MHz output
34 Demodulated output

Table Page
1 Display accuracy at 500 kHz/div 6
2 Display accuracy at 10 kHz/div 7
3 Display accuracy at 500 Hz/div 7

CONTENTS (continued)

Fig.	Test set-ups	Page
1	Frequency span	4
2	External standard input	8
3	Reference frequency	9
4	Frequency count	11
5	Resolution, 1 Hz	12
6	Resolution bandwidths	13
7	Residual f.m.	14
8	Drift	15
9	Displayed noise sidebands	16
10	Overload protection	17
11	Display fidelity	19
12	Amplitude accuracy	20
13	Frequency response	22
14	Input reflection coefficient	24
15	Local oscillator leakage	25
16	Harmonic distortion	26
17	Non-harmonic distortion	28
18	Third order intermodulation	29
19	Residual responses	30
20	Input noise sensitivity	31
21	Tracking generator cross-coupling	32
22	External trigger source	34
23	FM demod display accuracy	35
24	Tracking generator frequency accuracy	36
25	Tracking generator frequency response	37
26	Tracking generator amplitude	38
27	Tracking generator distortion	39
28	Tracking generator return loss	40
29	Standard 10 MHz output frequency	41
30	Standard 10 MHz output amplitude	42
31	47.4 MHz output	43
32	Demodulated output	45

INTRODUCTION

1. The test procedures in this chapter enable you to verify that the electrical performance of the Spectrum Analyzer, together with its Display Unit, complies with the Performance Data given in Chap. 1 (in the Operating Manual). The test equipment recommended for this purpose is listed in Chap 5-0. All tests may be performed with the covers in place and are intended to be carried out in the order given. For convenience, the test equipment and specification for each test are summarized before the test procedure.

TEST PRECAUTIONS

2. To ensure minimum errors and uncertainties when making measurements, it is important to observe the following precautions:-

(1) Always use recently calibrated test equipment, with any correction figures taken into account, so as to establish a known or traceable limit of performance uncertainty. This uncertainty must be allowed for in determining the accuracy of measurements.

(2) A common external frequency standard, with an accuracy within ±1 part in 10^6, should be used for the analyzer and for the test generator and other frequency controlled test equipment.

(3) Use the shortest possible connecting leads; ideally the analyzer should be directly coupled to the test equipment.

(4) Allow a warm-up time of half an hour before commencing tests.

(5) Before each test select the 'preset' and 'calibrated' operating conditions of the analyzer by pressing the PRESET and CAL keys. Every subsequent 10 minutes the CAL key must be pressed again to maintain calibration.

-TEST PROCEDURES-

FREQUENCY SPAN, /DIV and LOG

3. This tests the display accuracy in the /DIV mode. If it is correct the less stringent display accuracy in LOG mode can be assumed to be correct also.

SPECIFICATION	
Frequency span, /DIV:	±1% of full span ±1% separation
LOG:	±5N% where N = number of decades selected

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output range: -40 dBm to +10 dBm	Marconi 2019A

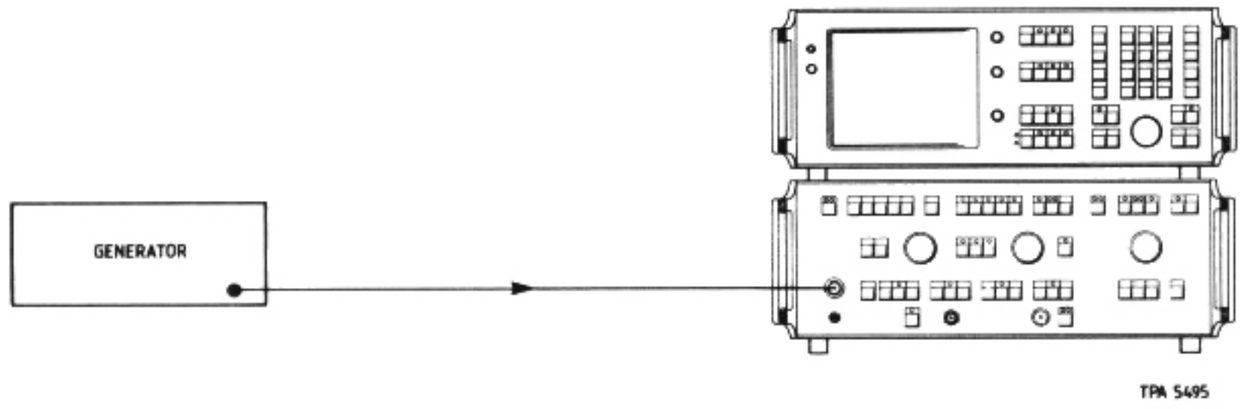


Fig. 1 Frequency span test set-up

Procedure

(1) Connect the generator output to the analyzer INPUT.

(2) On the generator select:

Carrier frequency ..... 9.5 MHz
Output level ..... -10 dBm
Incremental frequency..... 3.5 MHz

On the analyzer select:

PRESET and CAL
HORIZ POSN ..... left hand reference
REF LEVEL ..... 0 dB
SPAN/DIV ..... 500 kHz
REF FREQ ..... 9.5 MHz
PEAK FIND

(3) The marker annotation (Mkr1) shows the frequency of the response, which should be 9.5 MHz ±50 kHz.

(4) Increment the generator frequency by 3.5 MHz, to give a frequency of 13.0 MHz, and press PEAK FIND on the analyzer. The response should move to a position at 70% of full span, as shown on line 1 of Table 1, and the Mkr frequency should read 13.0 MHz ±85 kHz, the limit being shown on the bottom line under the 70% column.

(5) On the analyzer select:

REF FREQ ..... 14.5 MHz (as in line 2 of the table)
INC FREQ ..... 5 MHz

Increment the signal generator frequency by a further 3.5 MHz, press PEAK FIND and check that the 16.5 MHz response is at 40% of full span and within 70 kHz.

(6) Step through each successive line of Table 1 by incrementing the analyzer reference frequency by 5 MHz and the generator by 3.5 MHz and check the response for correct position and frequency.

(7) On the generator select:

Carrier frequency ..... 8.1 MHz

On the analyzer select:

SPAN/DIV ..... 10 kHz
SWEEP TIME ..... 50 ms/div
RESPONSE BANDWIDTH ..... 1 kHz
REF FREQ ..... 8.1 MHz

(8) Step through each line of Table 2 by incrementing the generator frequency and analyzer reference frequencies to the values shown and check the response for correct position and frequency.

(9) On the generator select:

Carrier frequency ..... 7.5 MHz

On the analyzer select:

SPAN/DIV ..... 500 Hz
SWEEP TIME ..... 2 s/div
RESPONSE BANDWIDTH ..... 30 Hz
REF FREQ ..... 7.5 MHz

(10) Step through each line of Table 3 by incrementing the generator and analyzer reference frequencies and check the response for correct position and frequency.

TABLE 1 DISPLAY ACCURACY at 500 kHz/div (AUTO mode)

2382 REF FREQ MHz	GENERATOR FREQUENCY (MHz) AS POSITION OF FULL SPAN									
	0	10	20	30	40	50	60	70	80	90
9.5	9.5							13.0		
14.5					16.5					
19.5		20.0							23.5	
24.5						27.0				
29.5			30.5							34.0
34.5							37.5			
39.5				41.0						
44.5	44.5							48.0		
49.5					51.5					
54.5		55.0							58.5	
59.9						62.0				
64.5			65.5							69.0
69.5							72.5			
74.5				76.0						
79.5	79.5							83.0		
84.5					86.5					
89.5		90.0							93.5	
94.5						97.0				
99.5			100.5							104.0
104.5							107.5			
109.5				111.0						
114.5	114.5							118.0		
119.5					121.5					
124.5		125.0							128.5	
129.5						132.0				
134.5			135.5							129.0
139.5							142.5			
144.5				146.0						
149.5	149.5							153.0		
154.5					156.5					
159.5		160.0							163.5	
164.5						167.0				
169.5			170.5							174.0
174.5							177.5			
179.5				181.0						
184.5	184.5							188.0		
189.5					191.5					
194.5		195.0							198.5	
199.5						202.0				
204.5			205.5							209.0
209.5							212.5			
214.5				216.0						
219.5	219.5							223.0		
224.5					226.5					
229.5		230.0							233.5	
234.5						237.0				
239.5			240.5							244.0
244.5							247.5			
249.5				251.0						
254.5	254.5							258.0		
259.5					261.5					
264.5		265.0							268.5	
269.5						272.0				
274.5			275.5							279.0
279.5							282.5			
284.5				286.0						
289.5	279.5							293.0		
294.5					296.5					
299.5		300.0							303.5	
304.5						307.0				
369.5			310.5							314.0
319.5				321.0						
324.5	324.5							328.0		
329.5					331.5					
334.5		335.0							338.5	
339.5						342.0				
344.5			345.5							349.0
349.5							352.5			
354.5				356.0						
359.5	359.5							363.0		
364.5					366.5					
369.5		370.0							373.5	
374.5						377.0				
379.5			380.5							384.0
384.5							387.5			
389.5				391.0						
394.5	394.5							398.0		
399.5	399.5									
Limits +/-	50kHz	55kHz	60kHz	65kHz	70kHz	75kHz	80kHz	85kHz	90kHz	95kHz

TABLE 2 DISPLAY ACCURACY at 10 kHz/div (manual mode)

	GENERATOR FREQUENCY (MHz) As Position of FULL SPAN									
2382 REF FREQ (MHz)	0	10	20	30	40	50	60	70	80	90
8.1	8.1	8.11								
8.6	8.6		8.62							
9.1	9.1			9.13						
9.6	9.6				9.64					
10.1	10.1					10.15				
10.6	10.6						10.66			
11.1	11.1							11.17		
11.6	11.6								11.68	
12.1	12.1	12.11								12.19
12.6	12.6		12.62							
13.1	13.1			13.13						
Limits +/-	1kHz	1.1kHz	1.2kHz	1.3kHz	1.4kHz	1.5kHz	1.6kHz	1.7kHz	1.8kHz	1.9kHz

TABLE 3 DISPLAY ACCURACY at 500 Hz/div (manual mode)

	GENERATOR FREQUENCY (MHz) As position of FULL SPAN									
2382 REF FREQ	0	10	20	30	40	50	60	70	80	90
7.50	7.50	7.5010								
7.51	7.51		7.5155							
7.52	7.52			7.5220						
7.53	7.53				7.5325					
7.54	7.54					7.5430				
7.55	7.55						7.5535			
7.56	7.56							7.5640		
7.57	7.57								7.5745	
7.58	7.58									7.5850
7.59	7.59	7.5910								
7.60	7.60		7.6015							
Limits +/-	50Hz	55Hz	60Hz	65Hz	70Hz	75Hz	80Hz	85Hz	90Hz	95Hz

EXTERNAL STANDARD INPUT

4. This tests the ability of the analyzer to lock to an external standard.

SPECIFICATION	
Ext. standard input:	The system will lock to an external standard signal of 1, 2, 5 or 10 MHz at a level between -15 and +15 dBm. The frequency must be within ±1 part in 10^6 for the system to lock.

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level: -40 dBm to +10 dBm	Marconi 2019A
Power meter	Frequency range: 30 kHz to 500 MHz Accuracy: ±0.02 dBm	Marconi 6960 & 6912 sensor
RF power splitter	Frequency range: d.c. to 500 MHz Impedance: 50 Ω	Weinschel 1870A
RF amplifier	Frequency range: 1 MHz to 500 MHz Gain: 40 dB	Marconi 2177

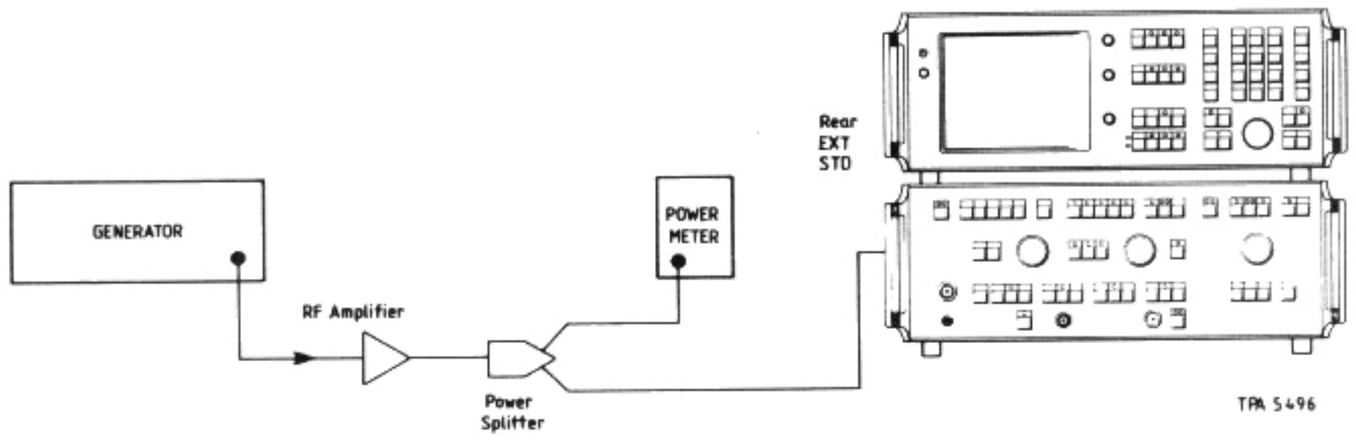


Fig. 2 External standard input test set-up

Procedure

(1) Connect the power meter sensor and the EXT STD input on the rear of the analyzer to the respective outputs of the power splitter.

(2) Set the generator frequency to precisely 1 MHz at an output level of -60 dBm. Connect the generator via the r.f. amplifier to the input of the power splitter. Adjust the generator level until the power meter reads +15 dBm.

External standard locking is indicated by the **ext std** annotation on the screen; if lock is not acheived the annotation remains flashing.

(3) Check that the external standard locks for each of the values below:-

EXT STD INPUT	
Freq (MHz)	Level (dBm)
1.0	-15
10.0	+15
10.0	-15
10.000010	0
10.999990	0

REFERENCE FREQUENCY, /DIV

5.

SPECIFICATION	
Accuracy:	±[(freq. std. error x ref. freq./10 MHz) +2% of selected sweep span + oscillator drift] Hz

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output range : -40 dBm to +10 dBm	Marconi 2019A

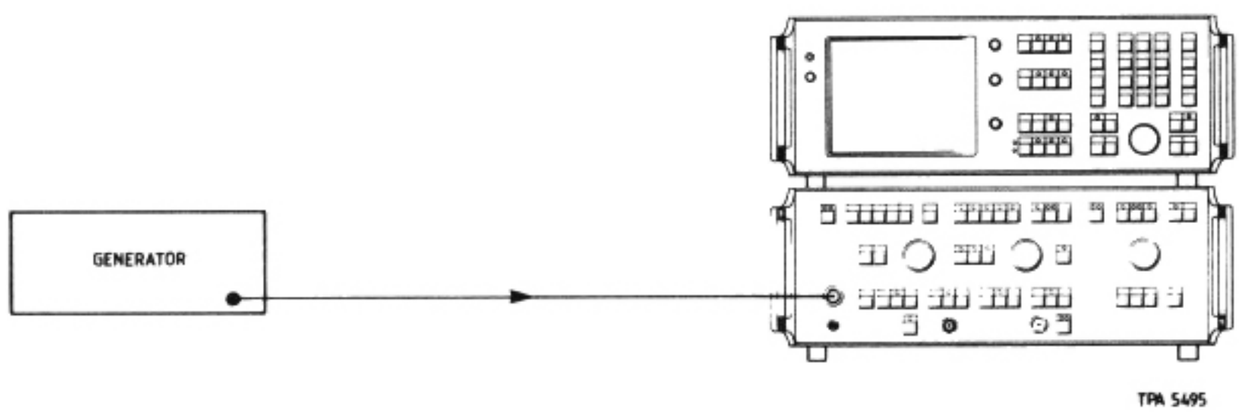


Fig. 3 Reference frequency test set-up

Procedure

(1) Connect the generator output to the analyzer INPUT.

(2) On the generator select 200 MHz at -10 dBm.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 200 MHz
REF LEVEL ..... 0 dBm

(3) Set SPAN/DIV, SWEEP TIME and RESOLUTION BANDWIDTH as in line 1 of the table below and trigger a single sweep on the analyzer.
Then press PEAK FIND and note that the response frequency shown by the Mkr1 annotation is 200 MHz ±8.05 MHz.

(4) Repeat step (3) for each set of values in the table and check that the frequency is within the limits shown.

SPAN/DIV	RESOLUTION BANDWIDTH	SWEEP TIME/DIV	LIMITS (±)
40 MHz	100 kHz	50 ms	8.05 MHz
20 MHz	100 kHz	20 ms	4.05 MHz
10 MHz	100 kHz	10 ms	2.05 MHz
5 MHz	100 kHz	10 ms	1.05 MHz
2 MHz	100 kHz	10 ms	0.45 MHz
1 MHz	100 kHz	10 ms	0.25 MHz
0.5 MHz	100 kHz	10 ms	0.15 MHz
200 kHz	30 kHz	10 ms	40.05 kHz
100 kHz	10 kHz	10 ms	20.5 kHz
50 kHz	10 kHz	10 ms	10.5 kHz
20 kHz	3 kHz	10 ms	4.5 kHz
10 kHz	1 kHz	5 ms	2.5 kHz
5 kHz	1 kHz	2 ms	1.5 kHz
2 kHz	300 Hz	100 ms	410 Hz
1 kHz	100 Hz	500 ms	210 Hz
500 Hz	100 Hz	500 ms	110 Hz
200 Hz	30 Hz	2.0 s	50 Hz
100 Hz	10 Hz	1.0 s	30 Hz
50 Hz	10 Hz	2.0 s	20 Hz

FREQUENCY COUNT

6.

SPECIFICATION
Frequency count: Resolution of screen readout ±10 kHz on spans >200 kHz/div, ±1 Hz on spans <200 Hz/div and ±100 Hz on all other spans, with the marker at least 20 dB out of noise and 3 dB bandwidth >0.2% of span

TEST EQUIPMENT
- none required -

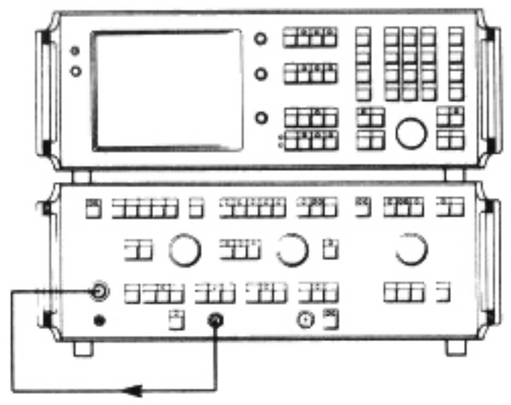


Fig. 4 Frequency count test set-up

Procedure

(1) Connect the STD 10 MHz OUTPUT to the INPUT.

Select:

PRESET and CAL
REF LEVEL ..... 0 dBm
SPAN/DIV ..... 40 MHz

(2) Move Mkr1 so that it is positioned on the 10 MHz peak at least 20 dB out of the noise.

Select:

FREQ COUNT
MKR1 SETS REF FREQ
SPAN/DIV ..... 10 kHz

Ensure that the response is within ±1 division from the reference frequency origin.

(3) Move Mkr1 onto the response at least 20 dB out of the noise.

Select:

MKR1 SETS REF FREQ
SPAN/DIV ..... 100 MHz

The response should be within ±1 div of the reference frequency origin.

(4) Repeat with SPAN/DIV 10 Hz. Mkr1 should read 10 MHz ±1 Hz.

RESOLUTION 1 Hz

7.

SPECIFICATION
As for frequency count except resolution of 1 Hz for all spans

TEST EQUIPMENT - none required -

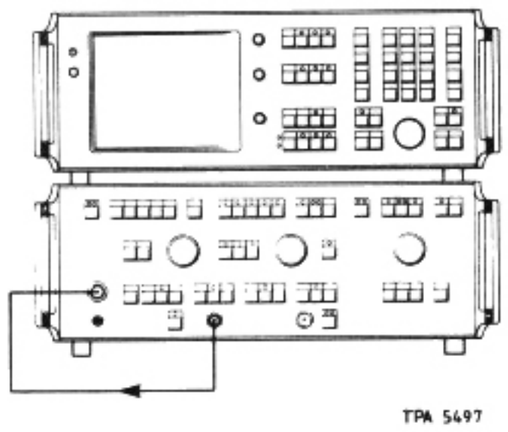


Fig. 5 Resolution 1 Hz test set-up

Procedure

(1) Connect the STD 10 MHz OUTPUT to the INPUT.

Select:

PRESET and CAL
REF FREQ ..... 15 MHz
REF LEVEL ..... 0 dBm
SPAN/DIV ..... 2 MHz

(2) Move marker Mkr1 onto the 10 MHz response and 20 dB out of the noise. Select RES 1 Hz (2nd FUNCT:FREQ COUNT) and allow time for the reading to be taken. Centre the 10 MHz response using MKR1 SETS REF FREQ and deselect RES 1 Hz. Set SPAN/DIV to 10 Hz and check that the **Ref** frequency annotation reads 10 MHz ±1 Hz.

RESOLUTION BANDWIDTHS

8.

SPECIFICATION
3 dB bandwidth: ±20% of nominal value (+0% -30% for 1 MHz filter) Shape factor : <11:1 (<5:1 for 1 MHz filter)

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz	Marconi 2019A

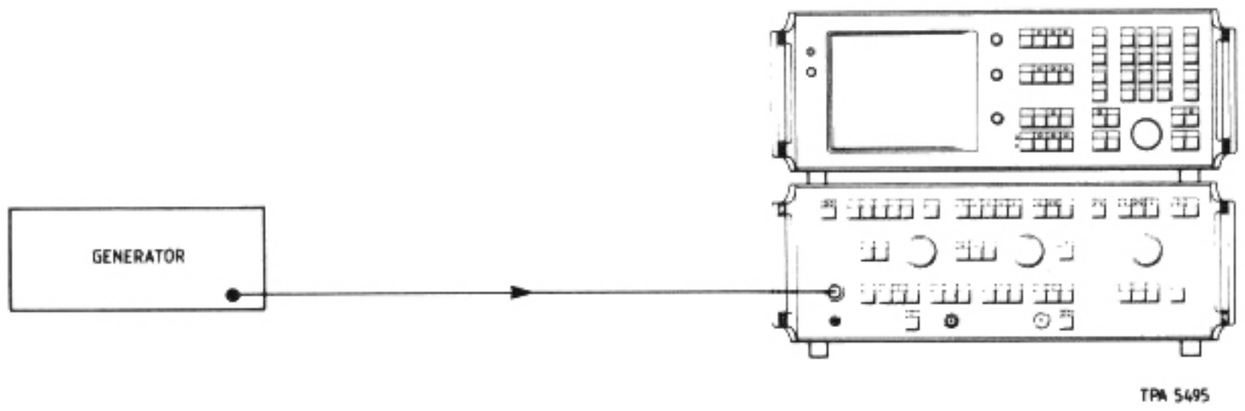


Fig. 6 Resolution bandwidths test set-up

Procedure

(1) Connect the generator OUTPUT to the analyzer INPUT.

On the generator select:

Carrier frequency ..... 10 MHz
Output level ..... 0 dBm

On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
REF LEVEL ..... +2 dBm
dB/DIVISION ..... 0.5 dB
RESOLUTION BANDWIDTH ..... 1 MHz
SPAN/DIV ..... 100 kHz
PEAK FIND
MKR1 SETS REF LEVEL

(2) Move Mkr1 to the lower 3 dB point and Mkr2 to the upper 3 dB point. The ΔF annotation will give the 3 dB bandwidth which should be equal to 1 MHz within the limits +0 and -300 kHz as shown in the table.

RESOLUTION BANDWIDTH	A 3 dB SPAN/DIV	B 60 dB SPAN/DIV	3 dB BANDWIDTH LIMITS	SHAPE FACTOR
1 MHz	100 kHz	500 kHz	+0-300 kHz	< 5:1
300 kHz	50 kHz	500 kHz	±60 kHz	<11:1
100 kHz	20 kHz	200 kHz	±20 kHz	<11:1
30 kHz	5 kHz	50 kHz	±6 kHz	<11:1
10 kHz	2 kHz	20 kHz	±2 kHz	<11:1
3 kHz	500 Hz	5 kHz	±600 Hz	<11:1
1 kHz	200 Hz	2 kHz	±200 Hz	<11:1
300 Hz	50 Hz	600 Hz	±60 Hz	<11:1
100 Hz	20 Hz	200 Hz	±20 Hz	<11:1
30 Hz	10 Hz	50 Hz	±6 Hz	<11:1
10 Hz	10 Hz	10 Hz	±2 Hz	<11:1
3 Hz	10 Hz	10 Hz	±1 Hz	<11:1

(3) Repeat (2) for each subsequent value of FILTER BANDWIDTH and 3 dB SPAN/DIV (Column A) in the table and check that the 3 dB bandwidth is correct to within the limits shown.

(4) Change dB/DIVISION to 10 dB and measure the 60 dB bandwidth for each value of RESOLUTION BANDWIDTH and 60 dB SPAN/DIV (Column B) in the table. For each measurement calculate the shape factor $\left(=\frac{\text{60 dB bandwidth}}{\text{3 dB bandwidth}}\right)$ and check that it is within the limits shown.

RESIDUAL FM

9.

SPECIFICATION	
Residual f.m.:	<1.5 Hz peak-to-peak during a 10 second period for spans <20 kHz, resolution bandwidths <30 kHz and video bandwidths <43 Hz

TEST EQUIPMENT		
Description	Minimum specification	Example
Crystal oscillator	Output level: 0 dBm Output frequency: 100 MHz Phase noise: <-90 dBm at 100 Hz offset	HCD185R

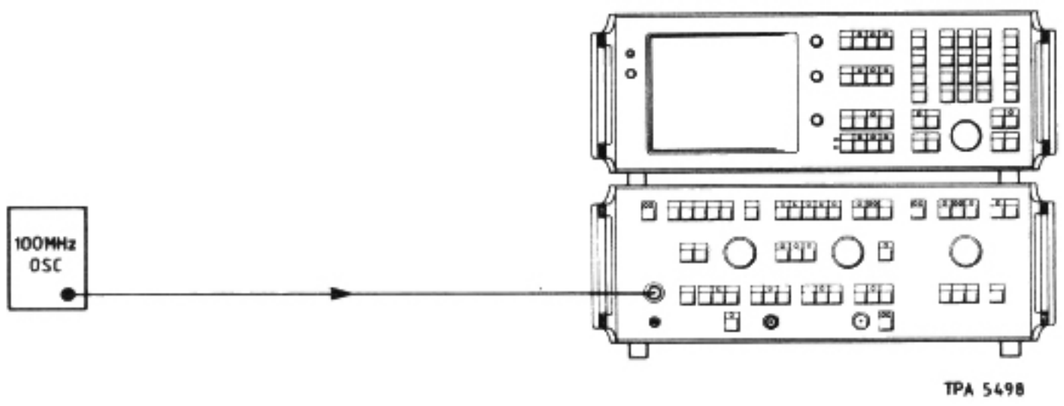


Fig. 7 Residual f.m. test set-up

Procedure

(1) Connect the crystal oscillator to the analyzer INPUT.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
SPAN/DIV ..... 10 kHz

(2) Adjust the REF LEVEL until the response is in the top 2 dB of the screen.

Select:

FM DEMOD (2ND FUNCT:ZERO SPAN)
SWEEP TIME ..... 2 s/DIV
RESOLUTION BANDWIDTH ..... 30 Hz

The displayed variation at any point should be less than 1.5 Hz.

DRIFT

10.

SPECIFICATION	
Drift: After a 1 hour warm-up	<10 Hz/min at 10 Hz/div. increasing to <20 Hz/min at 2 kHz/div. <500 Hz/min at 5 kHz/div. increasing to <1 kHz/min at 200 kHz/div. <100 kHz/min at 40 MHz/div.

TEST EQUIPMENT		
Description	Minimum specification	Example
Counter	Frequency range: 10 Hz to 500 MHz	Marconi 2432A

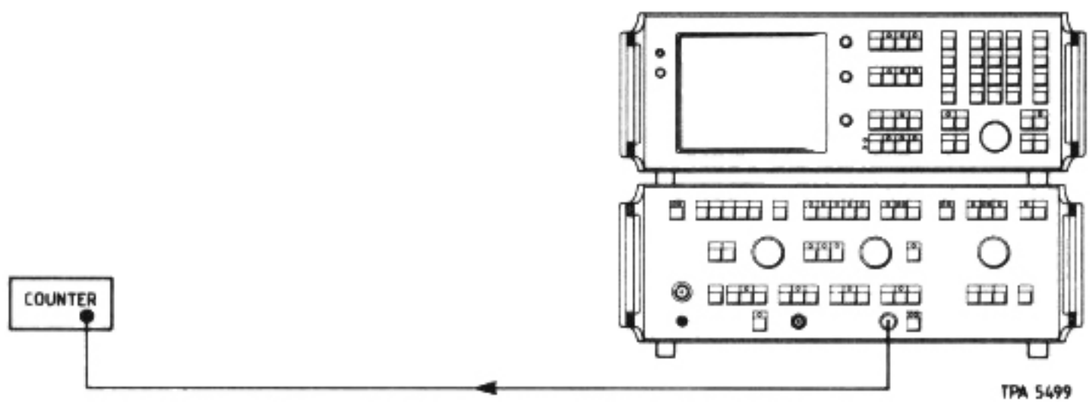


Fig. 8 Drift test set-up

Procedure

(1) Allow the analyzer to warm up for at least 1 hour. Connect the TRACKING GENERATOR output to the counter input.

(2) On the analyzer select:

PRESET and CAL
REF FREQ ..... 95 MHz
SPAN/DIV ..... 500 kHz
METER
TRACK GEN

Note the counter reading, wait 1 minute and note the reading again. The drift should be <50 kHz.

(3) Repeat for SPAN/DIV 5 kHz and check that the drift is <500 Hz.

(4) Repeat again for SPAN/DIV 500 Hz and check that the drift is <10 Hz.

DISPLAYED NOISE SIDEBANDS

11.

SPECIFICATION		
Displayed noise sidebands:	Displacement from carrier	Displayed noise to 1 Hz bandwidth
	100 Hz	<-90 dBc
	300 Hz	<-95 dBc
	20 kHz	<-100 dBc

TEST EQUIPMENT		
Description	Minimum specification	Example
100 MHz oscillator	Phase noise at 100 Hz : <-100 dBc/Hz at 1 kHz: <-110 dBc/Hz Output frequency : 100 MHz Output level : 0 dBm	HCD185R

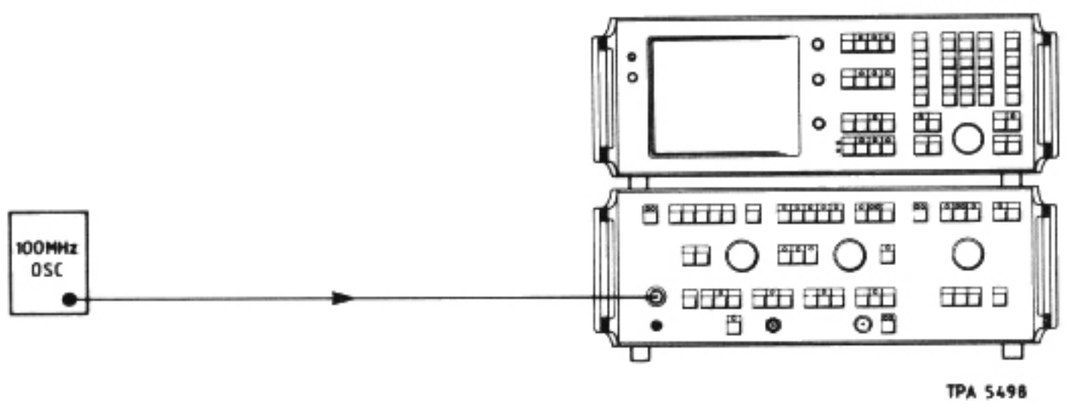


Fig. 9 Displayed noise sidebands test set-up

Procedure

(1) Connect the 100 MHz crystal oscillator to the analyzer INPUT.

(2) On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
REF LEVEL ..... 0 dBm
SPAN/DIV ..... 10 Hz
INC FREQ ..... 100 Hz
REF FREQ ↑

(3) Position marker at reference frequency origin.

Select NOISE 1 Hz (2nd FUNCT:FULL SPAN)

The marker should read the equivalent of at least -90 dBc.

(4) Press REF FREQ ↑ twice

The marker should read the equivalent of -95 dBc.

(5) Select REF FREQ ..... 100.02 MHz

The marker should read the equivalent of -100 dBc.

OVERLOAD PROTECTION

12.

SPECIFICATION
Overload protected to +47 dBm

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level: -40 dBm to +10 dBm	Marconi 2019A
RF amplifier	Gain of +40 dB	Marconi 2177

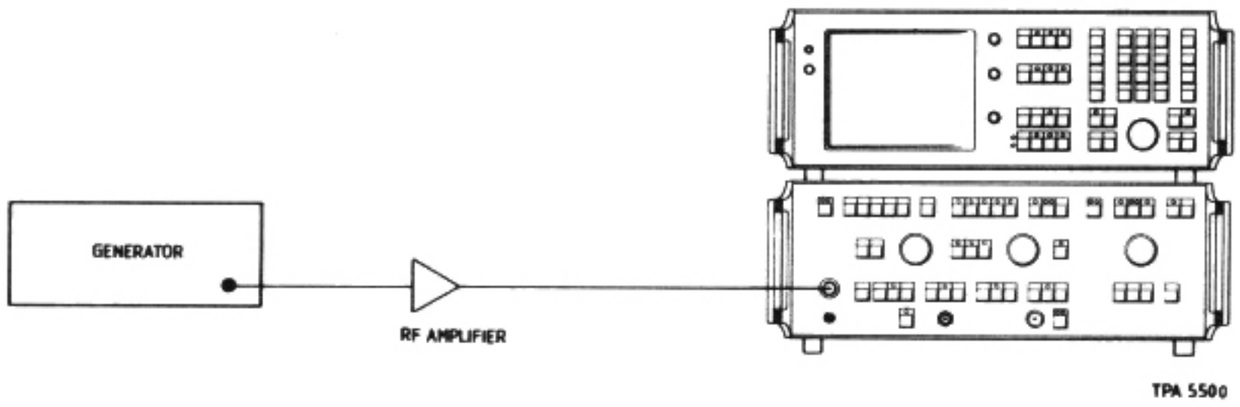


Fig. 10 Overload protection test set-up

Procedure

(1) Connect the r.f. amplifier to the analyzer INPUT.

(2) On the generator select:

Carrier frequency ..... 400 MHz
Output level ..... 30 dBm

(3) Connect the generator output to the r.f. amplifier input. Increase the generator level to -20 dBm. The analyzer should not register an overload.

(4) Increase the generator output to -10 dBm and check that the **Overload** annotation is displayed.

(5) Remove the input to the analyzer and press INTMD IDENT to remove the annotation and reset the overload protection.

DISPLAY FIDELITY, DB/DIV AND VOLTS/DIV

13.

SPECIFICATION
dB/DIV: departure from true logarithmic relationship less than 0.3 dB anywhere over the top 80 dB of display
VOLTS/DIV: linearity better than ±2% of full-scale

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A
Power meter	Frequency range: 30 kHz to 500 MHz Accuracy : ±0.02 dBm	Marconi 6960 & 6912 sensor
RF amplifier	Gain: 40 dB	Marconi 2177
RF attenuator	10 dB steps	HP 8495A
Power splitter	50 Ω, d.c. to 500 MHz	Weinschel 1870A

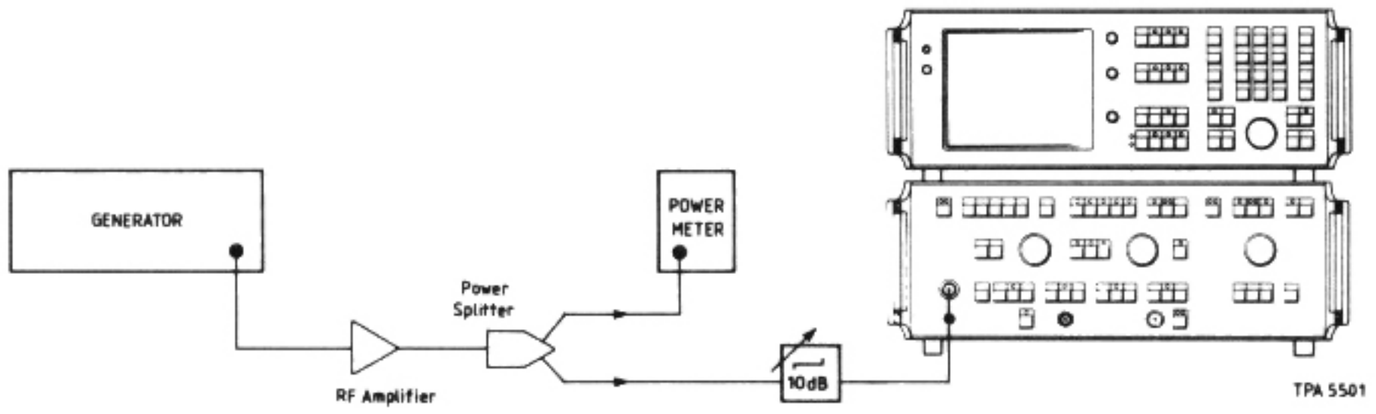


Fig. 11 Display fidelity test set-up

Procedure

(1) On the generator select a frequency of 10 MHz and an output level of -40 dB. Connect the generator via the amplifier to the power splitter. Connect the analyzer INPUT via the 10 dB step attenuator to the other port of the power splitter.

(2) On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
REF LEVEL ..... +10 dBm
SPAN/DIV ..... 100 kHz

(3) On the generator select a frequency of 10 MHz and adjust the output level to give +10 dBm on the screen. Note the power meter reading. Decrease the output level of the generator by 5 dB, checking correct reduction by use of the power meter. Use MKR1 and PEAK FIND to obtain the level of the response. All readings should be within 0.3 dB of the input level. Reduce the level in 5 dB steps to an input level of -10 dBm.

(4) Increase the output level of the generator to the original power meter reading. Introduce 20 dB of external attenuation. Repeat as above to an input level of -30 dBm.

(5) Increase the reference level of the generator to the initial power meter reading and introduce a further 20 dB of input attenuation. Repeat as previously to an input level of -50 dB.

(6) Adjust the generator output level to the initial power meter reading and introduce a further 20 dB of input attenuation. Repeat as above at a reference level on the screen of -70 dB.

AMPLITUDE ACCURACY

14.

SPECIFICATION	
dB/DIVISION accuracy:	±1 dB at any frequency, i.f. gain setting, r.f. attenuation setting, and filter bandwidth provided that the coupled control settings are not over-ridden

TEST EQUIPMENT		
Description	Minimum specification	Example
Generators	Frequency range : 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm Frequency range : 100 Hz to 1 MHz Output level : -40 dBm to +20 dBm	Marconi 2019A HP 3325
Power meter	Frequency range : d.c. to 50 MHz Accuracy : ±0.01 dB Frequency range : 30 kHz to 500 MHz Accuracy : ±0.02 dB	W & G EPM1 Marconi 6960 & 6912 sensor
Power splitter	50 Ω, d.c. to 500 MHz	Weinschel 1870A
RF attenuator	10 dB steps	HP 8495A

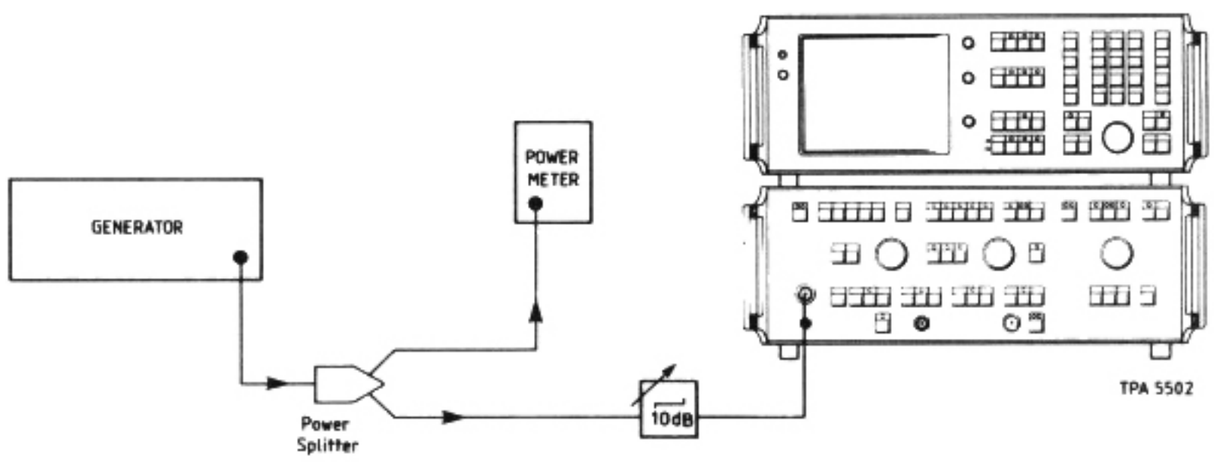


Fig. 12 Amplitude accuracy test set-up

Procedure

(1) Connect the STD 10 MHz OUTPUT to the INPUT.

(2) On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
REF LEVEL ..... -8 dBm
SPAN/DIV ..... 10 Hz
dB/DIVISION ..... 0.5 dB
B VIEW
VERTICAL A B SELECT ..... B
dB/DIVISION ..... 0.5 dB
RESOLUTION BANDWIDTH ..... 1 kHz
B SAVE

(3) Select each of the filters in turn and measure their amplitudes relative to the 1 kHz filter by use of MARKERS AB SELECT and PEAK FIND. Note each of the relative amplitudes. From these figures calculate the filter that has the greatest value relative to the 1 kHz filter and the one which has the least value relative to the 1 kHz filter.

(4) Connect the generator to the power splitter input. Connect the power meter to the output port and the attenuator onto the other output port of the power splitter. Attach the attenuator output onto the analyzer INPUT.

(5) On the generator select a carrier frequency of 100 Hz, levelled to 0 dBm.

(6) On the external attenuator select 20 dB attenuation.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 Hz
REF LEVEL ..... +10 dBm
SPAN/DIV ..... 10 Hz

(7) Select the greatest filter and measure the response level using MKR1 and PEAK FIND. Repeat using the least filter. Both readings should be 20 dB ±1 dB.

(8) For each of the generator frequencies and the analyzer reference frequencies below, level the generator to 0 dBm using the power meter and measure the response level using the calculated filters.

GENERATOR and ANALYZER FREQUENCIES				
(Hz)	(kHz)	(MHz)	(MHz)	(MHz)
100	2	2	145.01	310.01
200	6	6	160.01	325.01
600	20	10.01	175.01	340.01
	60	25.01	190.01	255.01
	200	40.01	205.01	370.01
	600	55.01	220.01	385.01
		70.01	235.01	400.00
		85.01	250.01	
		100.01	295.01	
		115.01	280.01	
		130.01	295.01	

(9) Repeat the procedure for the reference levels and external attenuator settings below.

ANALYZER REFERENCE LEVEL (dBm)	EXTERNAL ATTENUATOR (dB)	MARKER READING ±1 dB (dB)
+10	20	-20
0	20	-20
-10	30	-30
-20	30	-30
-30	40	-40
-40	40	-40

FREQUENCY RESPONSE

15.

SPECIFICATION	
Frequency response:	±0.4 dB for r.f. attenuation of >10 dB ±0.05 dB for r.f. attenuation of 0 dB

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 100 Hz to 1 MHz Output level : -40 dBm to +20 dBm	HP 3325
	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A
Power splitter	50 Ω	Weinschel 1870A
Power meter	Frequency range: d.c. to 50 MHz	W & G EPM1
Power meter	Frequency range: 30 kHz to 500 MHz Accuracy : ±0.02 dB	Marconi 6960 & 6912 sensor

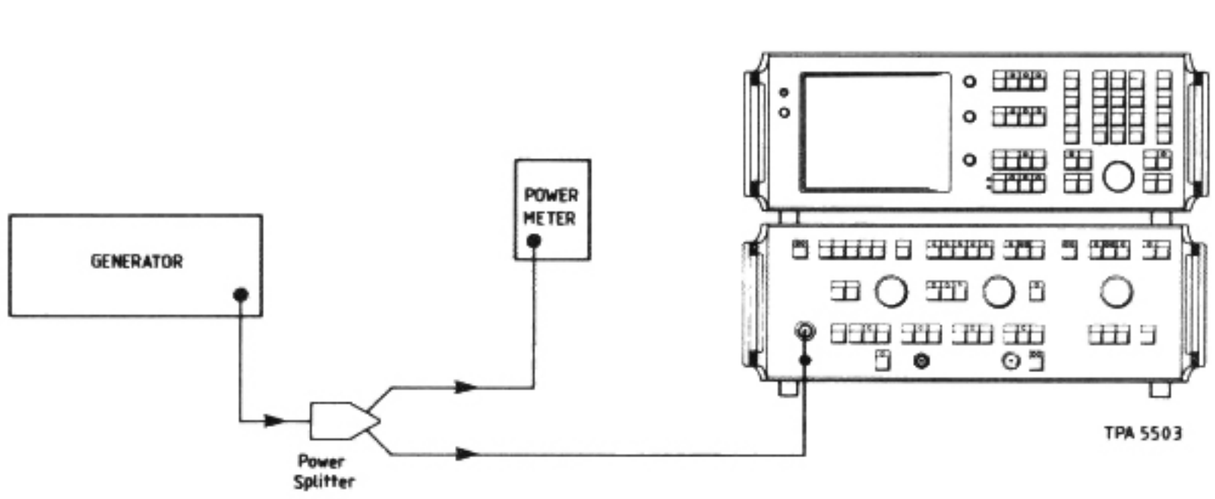


Fig. 13 Frequency response test set-up

Procedure

(1) Connect the generator as required to the power splitter input, and the power meter and analyzer to the power splitter outputs.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
REF LEVEL ..... -8 dBm
dB/DIVISION ..... 0.5 dB
RF ATTEN ..... 0 dB
SPAN/DIV ..... 1 kHz

(2) On the generator select 10 MHz and adjust the output level until the response on the analyzer is -10 dBm. Note the power meter reading.

(3) For each of the generator and analyzer frequencies below adjust the output so as to read the value for the 10 MHz level.

(4) On the power meter use MKR1 and PEAK FIND to obtain the level at each frequency. This should be -10 dBm ±0.5 dB.

(5) Repeat for 20 dB of input attenuation. The levels should be -10 dBm ±0.4 dB.

GENERATOR and ANALYZER FREQUENCIES				
(Hz)	(kHz)	(MHz)	(MHz)	(MHz)
100	2	2	130.01	280.01
200	6	6	145.01	295.01
600	20	10.01	160.01	310.01
	60	25.01	185.01	325.01
	200	40.01	190.01	340.01
	600	55.01	205.01	355.01
		70.01	220.01	370.01
		85.01	235.01	385.01
		100.01	250.01	400.0
		115.01	265.01	

INPUT REFLECTION COEFFICIENT

16.

SPECIFICATION	
Reflection coefficient:	<0.10 (20 dB return loss) for 10 dB attenuation settings <0.18 (15 dB return loss) for 0 dB attenuation settings

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range : 100 Hz to 1 GHz with tracking generator	Marconi 2370 & 2373 extender
Return loss bridge	Frequency range : 10 MHz to 1 GHz Impedance : 50 Ω	Wiltron 62N50

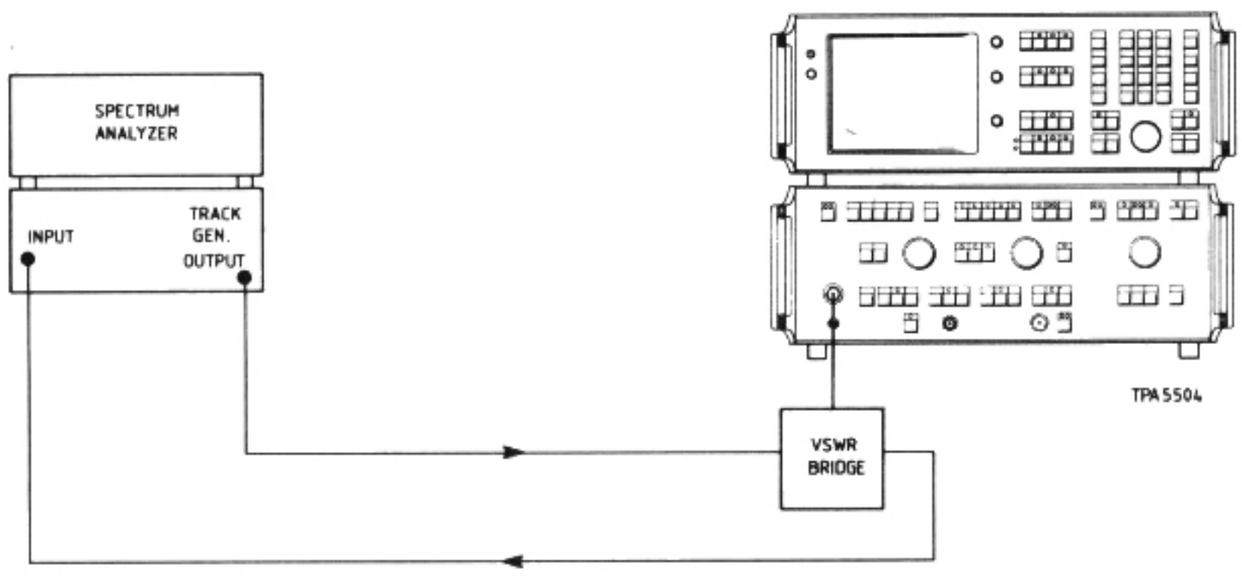


Fig. 14 Input reflection coefficient test set-up

Procedure

(1) Connect the test analyzer tracking generator output to the v.s.w.r. bridge input and the v.s.w.r. bridge output to the 2373 analyzer INPUT.

(2) On the test analyzer select:

Reference frequency ..... 200 MHz
Horizontal scale ..... 50 MHz/div
Reference level ..... 0 dB
Vertical scale ..... 10 dB/DIV

With the bridge test port open-circuited, save the level displayed on the test analyzer as a reference.

(3) Connect the v.s.w.r. bridge to the 2382 INPUT.

On the 2382 analyzer select:

REF FREQ ..... 0 MHz
ZERO SPAN
RF ATTEN ..... 0 dB

The maximum level on the test analyzer up to 400 MHz should be 15 dB below the reference level stored.

(4) Repeat for 10 dB r.f. attenuation on the 2382. The reflected response should be 20 dB below the reference level.

LOCAL OSCILLATOR LEAKAGE

17.

SPECIFICATION
Leakage: Typically <-95 dBm at any frequency and any attenuator setting

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range: 100 Hz to 1 GHz	Marconi 2370 & 2373 extender

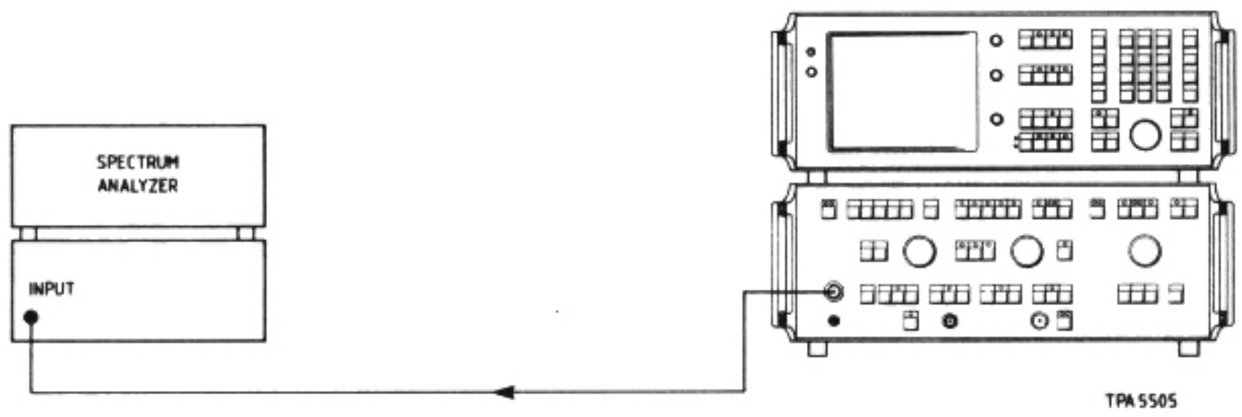


Fig. 15 Local oscillator leakage test set-up

Procedure

(1) Connect the 2382 analyzer INPUT to the test analyzer extender r.f. input.

On the 2382 select:

PRESET and CAL
REF FREQ ..... 0 MHz
RF ATTEN ..... 0 dB
ZERO SPAN

(2) Tune the 2373 to 502.6 MHz and check that any signal at this frequency is below -95 dBm.

HARMONIC DISTORTION

18.

SPECIFICATION	
Harmonic distortion:	With a sinusoidal signal at -42 dBm at the input mixer any internally generated harmonic distortion products will be >80 dB down on the fundamental

TEST EQUIPMENT		
Description	Minimum specification	Example
100 MHz crystal oscillator	Harmonics : >30 dB down on fundamental	HCD185R
100 MHz low-pass filter	Attenuation : >50 dB at 200 MHz. Cut-off frequency: 100 MHz	Telonic TCP100 48B

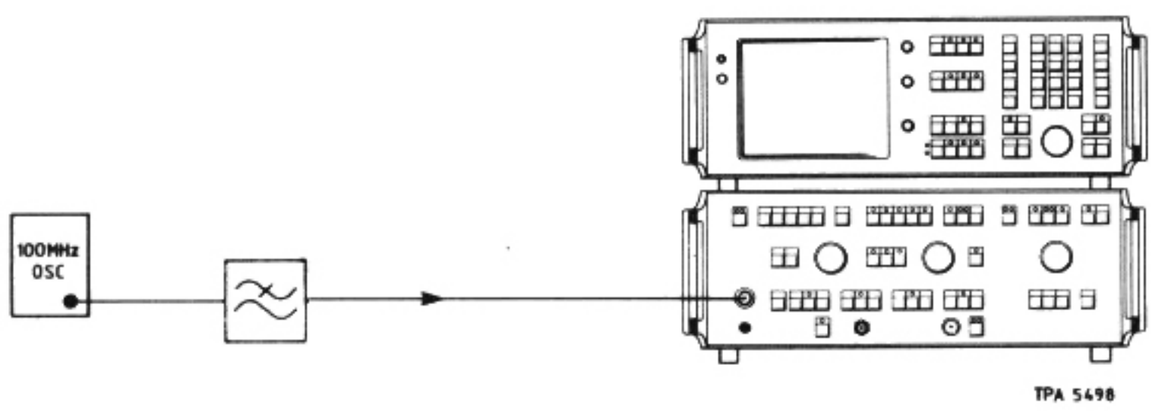


Fig. 16 Harmonic distortion test set-up

Procedure

(1) Connect the 100 MHz oscillator via the low-pass filter to the analyzer INPUT.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
REF LEVEL ..... -10 dB
SPAN/DIV ..... 200 Hz
RF ATTEN ..... 40 dB

(2) Adjust the oscillator output until it is at the top of the screen. Pressing INTMD IDENT should display ´**input level of -10 dB gives mixer level of -42 dBm.**´

Select:

PEAK FIND
MKR1 SETS REF FREQ
MKR1 SETS INC FREQ
REF FREQ ↑
SPAN/DIV ..... 10 Hz
RESOLUTION BANDWIDTH ..... 3 Hz
SWEEP MODE:SINGLE ARM
PEAK FIND

The marker reading should be at least 80 dB below the carrier (i.e. at least -90 dBm).

(3) Select:

REF FREQ ↑
SWEEP MODE:SINGLE ARM
MKR1 and PEAK FIND

The marker reading should again be at least -90 dBm.

(4) Select:

REF FREQ ↑
SWEEP MODE:SINGLE ARM
MKR1 and PEAK FIND

The marker reading again should be at least -90 dBm.

NON-HARMONIC DISTORTION

19.

SPECIFICATION	
Non-harmonic distortion:	With a sinusoidal signal at -42 dBm at the input mixer any internally generated non-harmonic distortion products will be >75 dB down on signal

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A

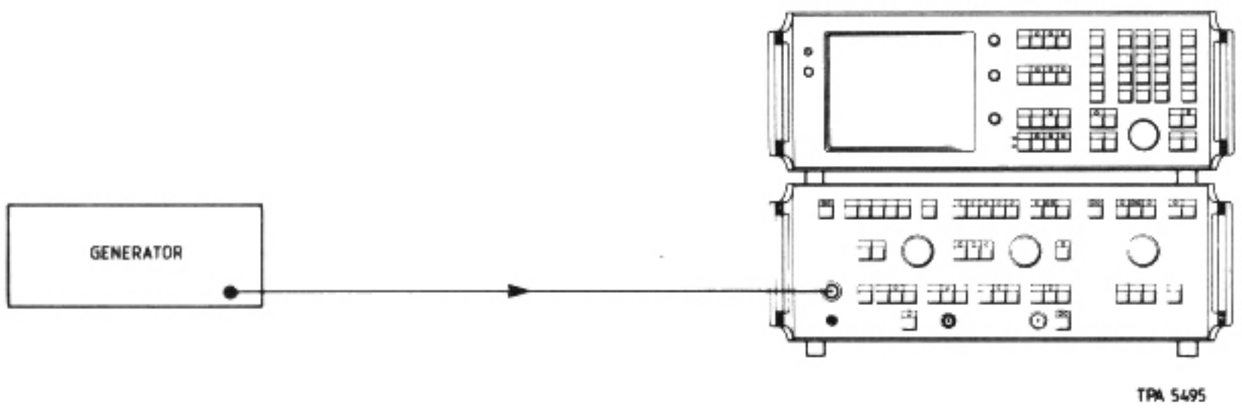


Fig. 17 Non-harmonic distortion test set-up

Procedure

(1) Connect the generator to the analyzer INPUT.

On the generator select:

Carrier frequency ..... 260 MHz
Reference level ..... -10 dBm

(2) On the analyzer select:

PRESET and CAL
REF FREQ ..... 8.7 MHz
REF LEVEL ..... -10 dB
SPAN/DIV ..... 10 Hz
RF ATTEN ..... 40 dB

(3) Adjust the generator so that the response is at -10 dBm on the screen. INTMD IDENT should display **´input level of -10 dBm gives mixer level of -42 dBm´**.

(4) Select RESOLUTION BANDWIDTH 3 Hz and use PEAK FIND to measure the response. The response should be at least -85 dBm.

Repeat for generator frequencies and analyzer reference frequencies below.

GENERATOR FREQUENCY (MHz)	REFERENCE FREQUENCY (MHz)
300.0	48.7
350.0	98.7
400.0	147.7
9.919	104.719
109.919	104.719
356.919	104.719

THIRD ORDER INTERMODULATION

20.

SPECIFICATION
Third order intermodulation: -95 dBc for on-screen signals using 3 Hz filter at -42 dBm at the input mixer

TEST EQUIPMENT		
Description	Minimum specification	Example
100 MHz crystal oscillator	Output level : 0 dBm Phase noise at 1 kHz: <-100 dBc	HCD 185R
Generator	Generator frequency : 1 MHz to 500 MHz Output range : 40 dBm to +10 dBm	Marconi 2019A
Combiner	Frequency : 100 MHz Impedance : 50 Ω	Mini-Circuits ZFSC-2-1

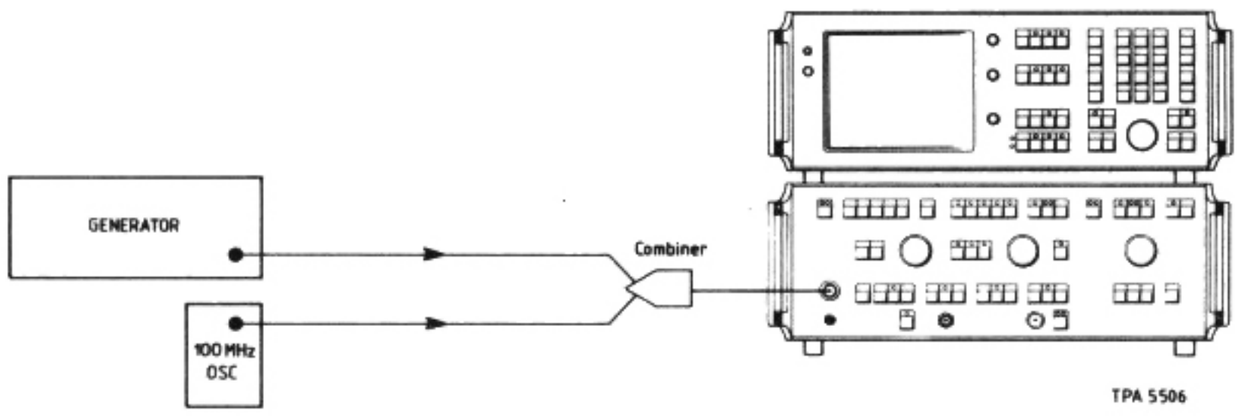


Fig. 18 Third order intermodulation test set-up

Procedure

(1) Connect the crystal oscillator and the generator to the combiner input. Connect the combiner output to the analyzer INPUT. Set the generator to 99.9995 MHz at -10 dBm.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
REF LEVEL ..... -10 dBm
SPAN/DIV ..... 500 Hz

(2) Adjust both peaks so that they are at the top of the screen. Position Mkr1 on the generator´s peak and Mkr2 on the other displayed peak.

Select:

MKR1 SETS INC FREQ
MKR1 SETS REF FREQ
SPAN/DIV ..... 10 Hz
RESOLUTION BANDWIDTH ..... 3 Hz
RF ATTEN ..... -40 dBm

(3) Pressing INTMD IDENT should display ´**input level of -10 dBm gives a mixer level of -42 dBm**´.

Select:

REF FREQ ↑
REF LEVEL ..... -20 dBm
SPAN/DIV ..... 10 Hz
SWEEP MODE:SINGLE ARM

Using Mkr1 the maximum response should be <-75 dBm.

RESIDUAL RESPONSES

21.

SPECIFICATION
Residual responses: <-120 dBm at 0 dB r.f. attenuation

TEST EQUIPMENT		
Description	Minimum specification	Example
50 Ω termination	Impedance: 50 Ω	Weinschel 1404

Fig. 19 Residual responses test set-up

Procedure

(1) Terminate the analyzer INPUT with the 50 Ω load.

Select:

PRESET and CAL
REF FREQ ..... 5 MHz
REF LEVEL ..... -80 dB
SPAN/DIV ..... 100 Hz
RESOLUTION BANDWIDTH ..... 10 Hz
RF ATTEN ..... 0 dB
PEAK FIND
SWEEP MODE:SINGLE ARM

The response should be <-120 dBm.

(2) Repeat for the reference frequencies below:

REFERENCE FREQUENCIES (MHz)	
10.0	40
15.0	50
20.0	100
30.0	200
35.0	250
	300

INPUT NOISE SENSITIVITY

22.

SPECIFICATION
Sensitivity: <-135 dBm for reference frequencies greater than 150 kHz

TEST EQUIPMENT		
Description	Minimum specification	Example
Type N termination	Impedance: 50 Ω	Weinschel 1404

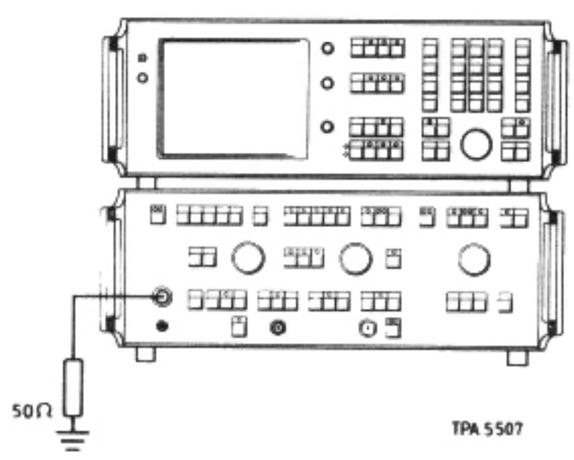


Fig. 20 Input noise sensitivity test set-up

Procedure

(1) Terminate the INPUT with a 50 Ω load.

Select:

PRESET and CAL
REF FREQ ..... 151 kHz
REF LEVEL ..... -50 dBm
SPAN/DIV ..... 10 Hz
RF ATTEN ..... 0 dB
RESOLUTION BANDWIDTH ... 3 Hz
SWEEP MODE SINGLE ARM
PEAK FIND

The response should be <-135 dBm.

(2) Repeat using REF FREQ 200.01 MHz.

TRACKING GENERATOR CROSS-COUPLING

23.

SPECIFICATION	
Cross-coupling:	With the tracking generator switched on and both the input and the tracking generator output terminated in 50 Ω, the displayed noise level in a 3 Hz bandwidth is not >-125 dBm from 150 kHz to 400 MHz

TEST EQUIPMENT		
Description	Minimum specification	Example
2 x Type N terminations	Impedance: 50 Ω	Weinschel 1404

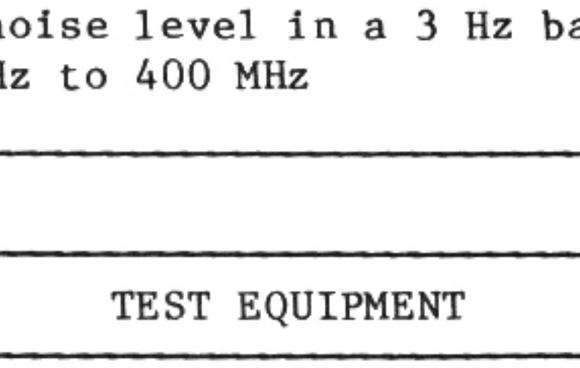


Fig. 21 Tracking generator cross-coupling test set-up

Procedure

(1) Terminate the INPUT and TRACKING GENERATOR output with 50 Ω.

Select:

PRESET and CAL
REF FREQ ..... 0.15 MHz
REF LEVEL ..... -60 dBm
SPAN/DIV ..... 10 Hz
RF ATTEN ..... 0 dB
RESOLUTION BANDWIDTH ... 3 Hz
TRACK GEN
SWEEP MODE:SINGLE ARM
PEAK FIND

The response should be at least -125 dBm.

(2) Repeat for the frequencies below

REFERENCE FREQUENCIES (MHz)
1.03
3.03
10.03
30.03
100.03
200.03
300.03
399.99

EXTERNAL TRIGGER SOURCE

24.

SPECIFICATION	
External trigger source:	Sweep is triggered by external signals from the rear panel EXT TRIG BNC connector over the range 50 mV p-p to 100 V p-p from 10 Hz to 300 kHz

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 100 Hz to 1 MHz Output level : -40 dBm to +20 dBm	HP3325

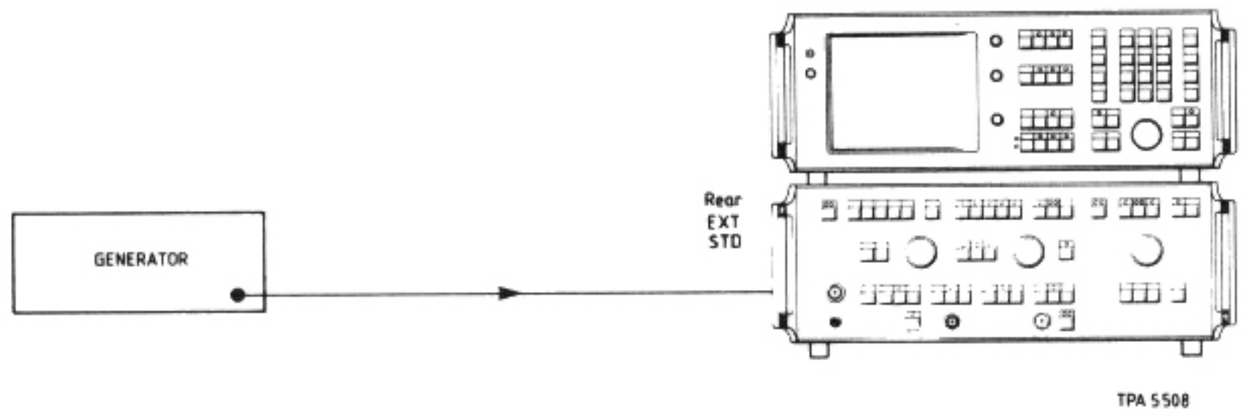


Fig. 22 External trigger source test set-up

Procedure

(1) On the analyzer select:

TRIGGER SOURCE EXT
AUTO TRIGGER ..... off
SWEEP MODE SINGLE ARM

(2) Connect the signal source to the EXT TRIG input on the rear of the 2382 and check that the yellow sweep light (in the SINGLE ARM key) is extinguished for each of the inputs below:

10 Hz at 50 mV p-p
10 Hz at 5 V p-p
300 kHz at 50 mV p-p
300 kHz at 5 V p-p

Note ...

Reselect SINGLE ARM to re-arm the sweep before applying each input.

FM DEMOD DISPLAY ACCURACY

25.

SPECIFICATION	
Accuracy:	Deviation accuracy at zero deviation rate is ±20% ±1 kHz. Bandwidth depends upon selected filter

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A

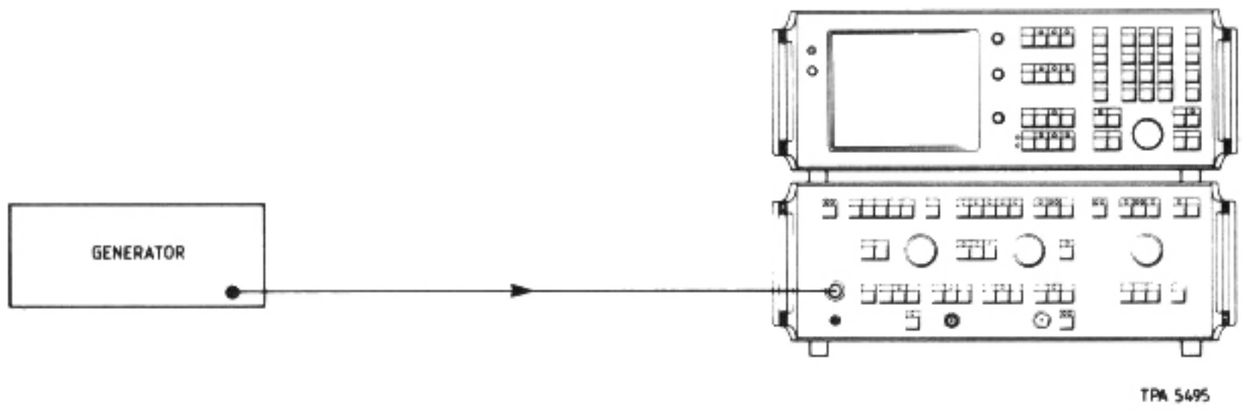


Fig. 23 FM demod display accuracy test set-up

Procedure

(1) Connect the generator output to the analyzer INPUT.

On the generator select:

Frequency ..... 100 MHz
Output level ..... 0 dBm

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
REF LEVEL ..... 0 dB
SPAN/DIV ..... 100 kHz

(2) Adjust the generator level until the response is within the top 2 dB of screen. On the analyzer select:

FM DEMOD (2ND FUNCT:ZERO SPAN)
SPAN/DIV ..... 1 kHz

Note the reading, increase the generator frequency by 1 kHz and check that the reading on the analyzer is the original value +1 kHz ±120 Hz.

TRACKING GENERATOR FREQUENCY ACCURACY

26.

SPECIFICATION
Accuracy: ±1 Hz referred to the tuned frequency

TEST EQUIPMENT		
Description	Minimum specification	Example
Counter	Frequency range: 10 Hz to 500 MHz	Marconi 2432A

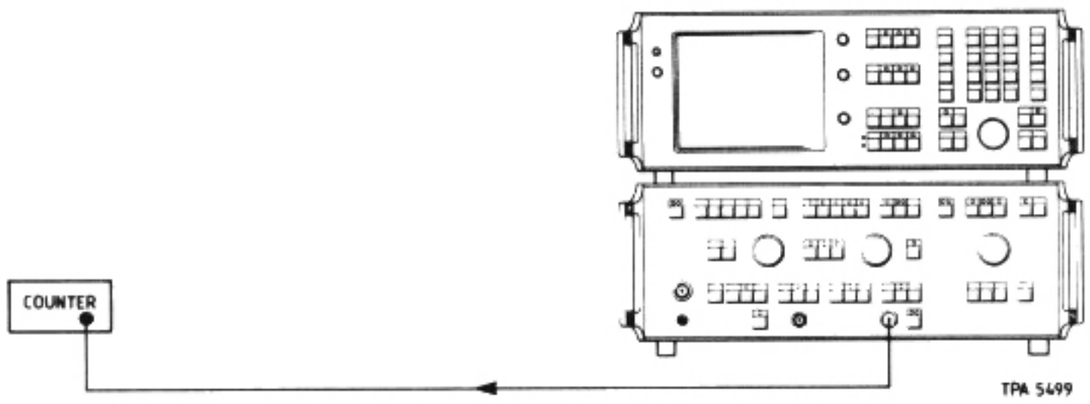


Fig. 24 Tracking generator frequency accuracy test set-up

Procedure

(1) Connect the TRACKING GENERATOR output to the counter input.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 100 MHz
ZERO SPAN

The counter should read 100 MHz ±1 Hz.

TRACKING GENERATOR FREQUENCY RESPONSE

27.

SPECIFICATION
Amplitude accuracy: ±0.5 dB at -10 dBm at 10 MHz
Frequency response: ±0.35 dB at -10 dBm

TEST EQUIPMENT		
Description	Minimum specification	Example
Power meter	Frequency : 30 kHz to 500 MHz Accuracy : ±0.02 dB	Marconi 6960 & 6912 sensor
Power meter	Frequency range: d.c. to 50 MHz Accuracy : ±0.01 dB	W & G EPM1

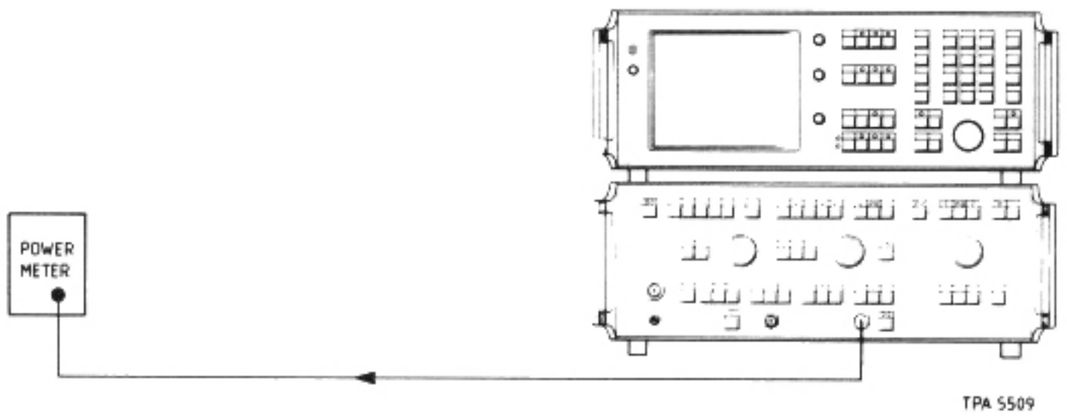


Fig. 25 Tracking generator frequency response test set-up

Procedure

(1) Connect the TRACKING GENERATOR output to the input of the appropriate power meter.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
ZERO SPAN

The power meter reading should be -10 dBm ±0.5 dB.

(2) Select:

REF FREQ ..... 200 Hz

The power meter should read the level at 10 MHz ±0.35 dB.

(3) Repeat for all of the frequencies below. Each reading should be within ±0.35 dB of the level at 10 MHz.

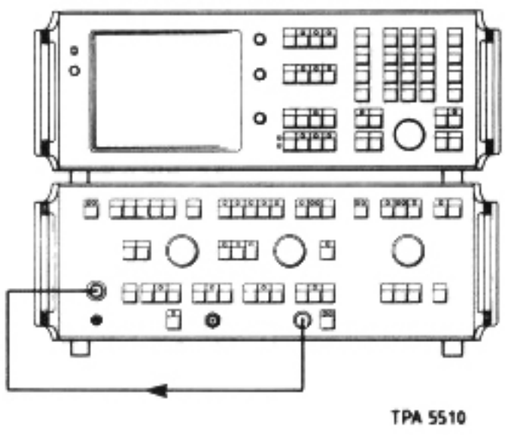
REFERENCE FREQUENCY			
(kHz)	(MHz)	(MHz)	(MHz)
0.5	2.0	130.0	280.0
2.0	5.0	145.0	295.0
5.0	10.0	160.0	310.0
20.0	25.0	175.0	325.0
50.0	40.0	190.0	340.0
200.0	55.0	205.0	355.0
500.0	70.0	220.0	370.0
	85.0	235.0	385.0
	100.0	250.0	400.0
	115.0	265.0	

TRACKING GENERATOR AMPLITUDE SETTING

28.

SPECIFICATION
Amplitude: -9.7 dBm to -20 dBm in 0.1 dB steps

TEST EQUIPMENT
- None required -



TPA 5510

Fig. 26 Tracking generator amplitude test set-up

Procedure

(1) Connect the TRACKING GENERATOR output to the INPUT.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
SPAN/DIV ..... 10 kHz
TRACK GEN
SET TG (2ND FUNCT:REF LEVEL) .... -9.7 dBm
PEAK FIND

The marker should read -9.7 dBm ±0.5 dB and the annotation at the top of the screen should read -9.7 dBm.

(2) Select a tracking generator level of -20.3 dBm. The marker should read -20.3 dBm ±0.5 dB and the associated annotation should read -20.3 dBm.

TRACKING GENERATOR DISTORTION

29.

SPECIFICATION
Harmonics : all >30 dB down on the fundamental signal Non-harmonic signals: all >30 dB down on the fundamental signal Residual signals : all <-70 dBm with the tracking generator off

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range: 100 Hz to 1 GHz	Marconi 2370 & 2373 extender

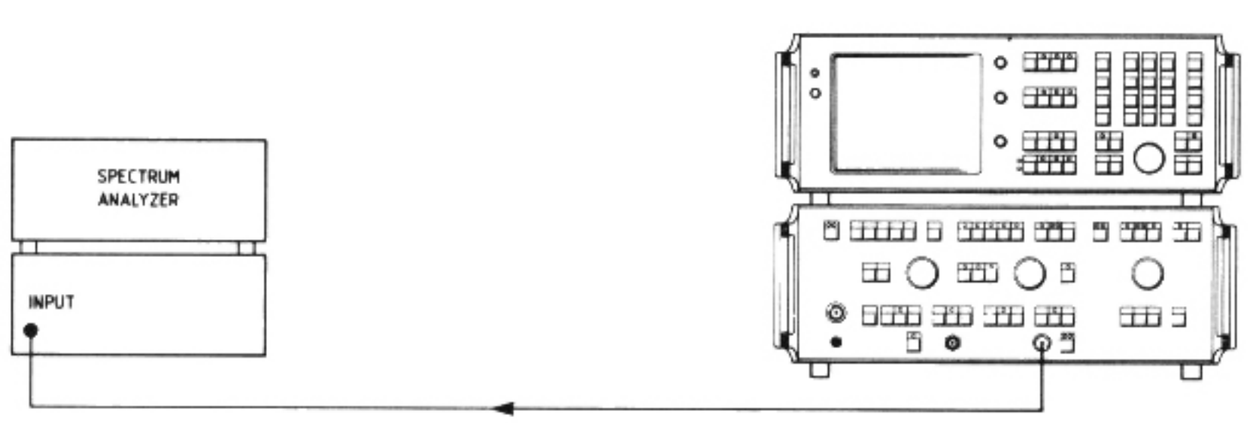


Fig. 27 Tracking generator distortion test set-up

Procedure

(1) Connect the TRACKING GENERATOR output to the test analyzer input.

On the test analyzer select:

Reference frequency ..... 200 MHz
Horizontal scale ..... 500 MHz/DIV
Top of screen ..... 0 dBm
Vertical scale ..... 10 dB/DIV

On the 2382 select:

PRESET and CAL
FULL SPAN
TRACK GEN

All harmonics and spurious signals should be >30 dB down on the fundamental.

Deselect TRACK GEN. Any residual signals should be <-70 dBm.

TRACKING GENERATOR RETURN LOSS

30.

SPECIFICATION
Return loss: 20 dB

TEST EQUIPMENT		
Description	Minimum specification	Example
Attenuators Mismatch Cable	N-type 10 dB attenuators (Qty. 2) 470 Ω resistor with N-type connectors 1.5 m of N-type 50 Ω cable	Marconi 6534/3 - RG214

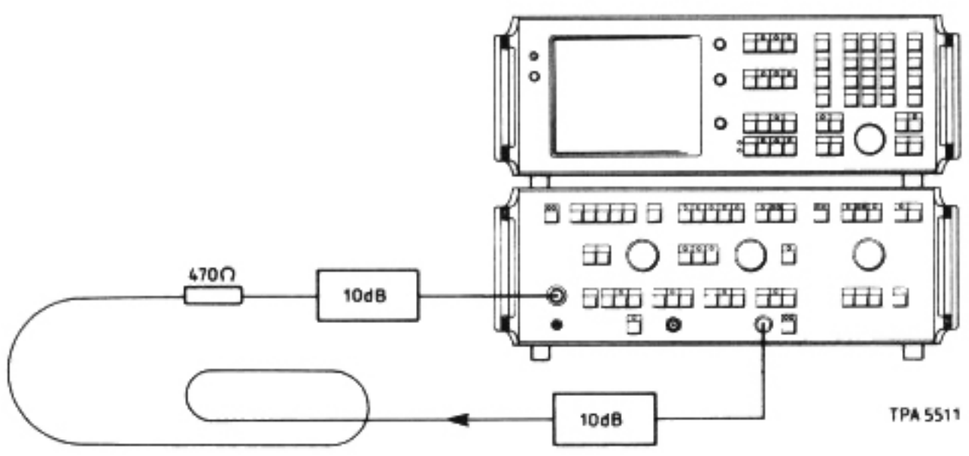


Fig. 28 Tracking generator return loss test set-up

Procedure

(1) Select:

PRESET and CAL
REF LEVEL ..... -42.5 dBm
SWEEP TIME ..... 500 ms/div
TRACK GEN

(2) Select NORM once, then attach the assembly as shown and reselect NORM.

Select:

REF LEVEL ..... 2.5 dBm
SWEEP MODE SINGLE ARM

The maximum amplitude of the displayed signal should be 1 dB.

STANDARD 10 MHz OUTPUT FREQUENCY

31.

SPECIFICATION
Frequency: 10 MHz ± standard frequency error

TEST EQUIPMENT		
Description	Minimum specification	Example
Counter	Frequency range: 100 Hz to 500 MHz	Marconi 2432A

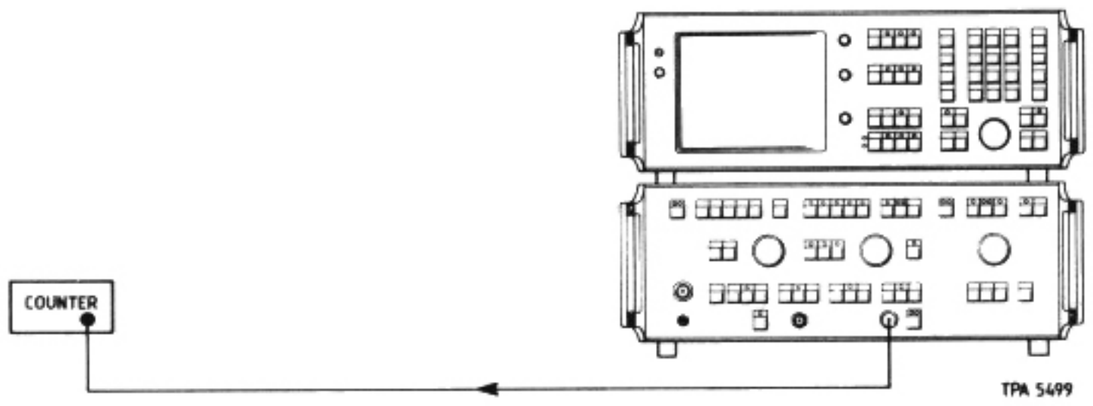


Fig. 29 Standard 10 MHz output frequency test set-up

Procedure

(1) Connect the STD 10 MHZ OUTPUT to the counter input. Remove any standard input connected to the analyzer EXT STD socket.

The counter should read 10 MHz ±20 Hz.

STANDARD 10 MHz OUTPUT AMPLITUDE

32.

SPECIFICATION
Amplitude: -10 dBm ±0.3 dB

TEST EQUIPMENT		
Description	Minimum specification	Example
Power meter	Frequency range: 30 kHz to 500 MHz Accuracy : ±0.02 dB	Marconi 6960 & 6912 Sensor
Generator	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A

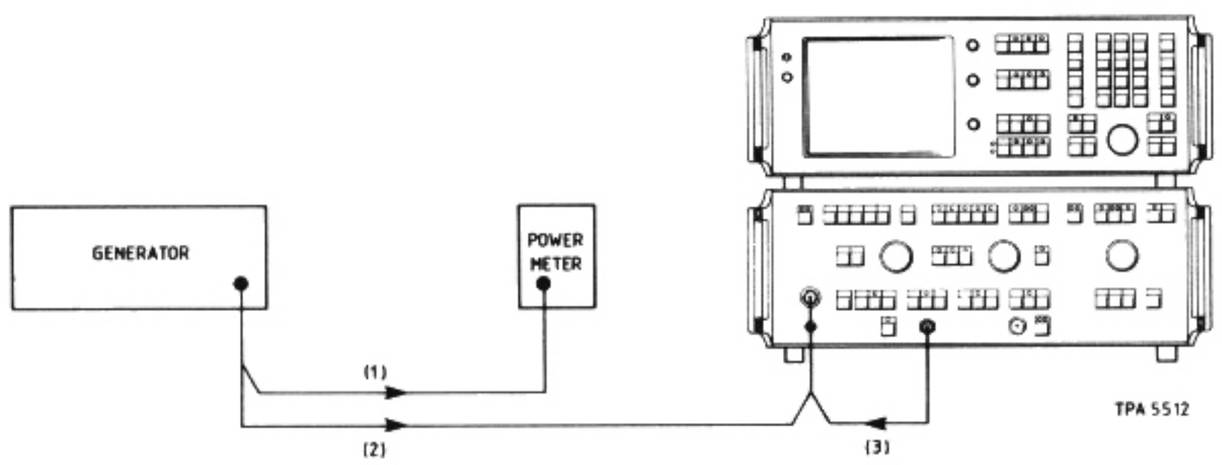


Fig. 30 Standard 10 MHz output amplitude test set-up

Procedure

(1) Connect the generator output to the power meter input.

On the generator select:

Carrier frequency ..... 10 MHz
Output level ..... -10 dBm

Adjust the reference level until the power meter reads -10 dB.

(2) Connect the generator output to the analyzer INPUT.

On the analyzer select:

PRESET and CAL
REF FREQ ..... 10 MHz
REF LEVEL ..... -8 dBm
SPAN/DIV ..... 10 kHz
dB/DIVISION ..... 0.5 dB
A SAVE

(3) Connect the STD 10 MHz OUTPUT to the INPUT.

On the analyzer select:

B VIEW
VERTICAL A B SELECT ..... B
dB/DIVISION ..... 0.5 dB

Using the markers the level of the 10 MHz standard should be within ±0.3 dB of the stored generator level.

47.4 MHz OUTPUT

33.

SPECIFICATION	
Centre frequency:	47.4 MHz
Bandwidth :	typically 3 MHz
Amplitude :	nominally 3 dB greater than r.f. input signal for 0 dB r.f. attenuation

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range: 100 Hz to 1 GHz	Marconi 2370 & 2373 extender

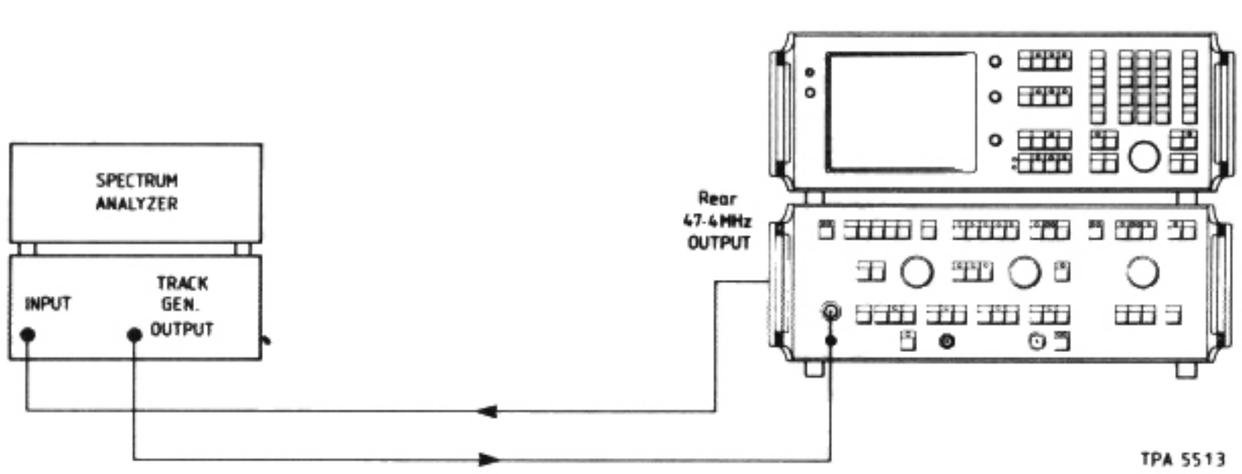


Fig. 31 47.4 MHz output test set-up

Procedure

(1) Connect the test analyzer tracking generator output to the 2382 INPUT. Connect the 47.4 MHz OUTPUT at the rear of the 2382 to the analyzer input.

(2) On the test analyzer select:

Reference frequency	47.4 MHz
Top of screen	+5 dB
Horizontal scale	1 MHz/div
Vertical scale	1 dB/DIV

(3) On the 2382 select:

REF FREQ	47.4 MHz
RF ATTEN	0 dB
SPAN/DIV	0

The response displayed on the test analyzer should be centred on 47.4 MHz with a bandwidth of nominally 3 MHz. The peak level should be nominally 3 dB greater than the test analyzer tracking generator output level.

DEMODULATED OUTPUT

34.

SPECIFICATION
Dependent on vertical scale range, modulation depth and volume control setting. Signal level corresponding to a signal at the top of the screen is nominally:

10 to 0.5	dB/div.	6.5 V
Linear 1	V/div.	1.5 V
2	V/div.	2.0 V
5	V/div.	3.5 V

TEST EQUIPMENT		
Description	Minimum specification	Example
Generator	Frequency range: 1 MHz to 500 MHz Output level : -40 dBm to +10 dBm	Marconi 2019A
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

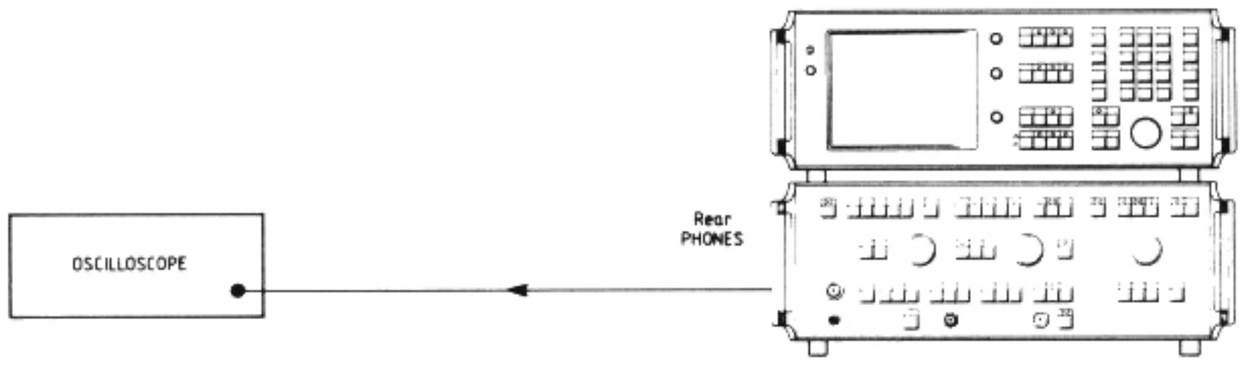


Fig. 32 Demodulated output test set-up

Procedure

(1) Lock the analyzer and the generator to an external standard. Connect the PHONES output to the oscilloscope.

On the generator select:

Carrier frequency ..... 100 MHz
AM depth 30%
Modulation frequency ..... 1 kHz
Modulation ..... Off
Reference level ..... 10 dBm

On the analyzer select:

REF FREQ ..... 100 MHz
SPAN/DIV ..... 20 kHz
VOLTS/DIV ..... 100 mV full-scale
RESOLUTION BANDWIDTH ..... 10 kHz
VOL control ..... fully clockwise

Adjust the r.f. level of the generator until the response is at 50 mV. Then switch the modulation on.

On the analyzer select:

ZERO SPAN
AUDIO (2ND FUNCT METER)
SWEEP TIME ..... 1 ms/div

The demodulated signal will be displayed on the oscilloscope. Check that its amplitude is approximately 2 V peak-to-peak.

Chapter 5-2

ADJUSTMENT AND CALIBRATION

CONTENTS

Para.
1 Introduction

- Procedures -
4 AA2 - Input low-pass filter
6 AA2a - Input filter and mixer
9 AA3 - 502.6 MHz i.f. filter
11 AA3a - 2nd mixer
13 AA4 - Sampling gate
15 AA5 - Master u.h.f. VCO
17 AA7 - Slave u.h.f. VCO
19 AA8 - Master/slave phase detector
21 AA9 - 2nd local oscillator VCO
23 AB1 - D-A converter
25 AB2 - Interpolation oscillator
27 AB3 - Master h.f. VCO
29 AB4 - Sampling gate
31 AB5 - Slave h.f. VCO
33 AC1 - 50 MHz crystal oscillator
35 AC2 - 47.4 MHz i.f. amplifier
37 AC3 - 2.6 MHz LC filter
39 AC4 - 100 kHz i.f. crystal filter
41 AC5 - 2.6 MHz crystal filters
43 AD1 - Log amplifier
45 AD4 - 10 MHz calibrator
47 AE1 - 47.4 MHz crystal oscillator
49 AE3 - 502.6 MHz band-pass filter
51 AE5 - 400 MHz low-pass filter
53 AE6 - Amp/leveller
55 AE7 - Cal switch
56 AR2 - Power supply interface

Table Page
1 Board calibration order 2
2 AD1 attenuator switlch adjustment 23

Fig.
1 AD1 snotchet adjustment 22

INTRODUCTION

1. This chapter describes adjustments which will restore the analyzer to its peak operating condition. Test equipment recommended for this purpose is listed in Chap. 5-0 and summarized for each test board procedure. Before carrying out any adjustment procedures refer to Chap. 5-0 for safety considerations and access instructions.

2. Adjustable procedures are described for each board and are listed in board alph-anumeric order. When it is known that readjustment is needed on just one or two boards it is normally sufficient to confine activities to those boards alone. If extensive re-adjustment or re-calibration is needed, the complete set of procedures should be carried out, in the order shown in Table 1.

3. Adjustment and factory selected components are indicated on the circuit diagrams and their location is shown on the layout diagrams opposite the circuit diagrams.

TABLE 1 BOARD CALIBRATION ORDER

SEQUENCE	BOARD	TITLE
1	AR2	Power supply interface
2	AD4	10 MHz calibrator
3	AC1	50 MHz crystal oscillator
4	AB1	D-A converter
5	AB2	Interpolation oscillator
6	AB3	Master h.f. VCO
7	AB4	Sampling gate
8	AB5	Slave h.f. VCO
9	AA5	Master u.h.f. VCO
10	AA4	Sampling gate
11	AA7	Slave u.h.f. VCO
12	AA8	Master slave phase detector
13	AA9	2nd local oscillator VCO
14	AE1	47.4 MHz crystal oscillator
15	AE3	502.6 MHz band-pass filter
16	AE5	400 MHz low-pass filter
17	AE6	Amp/leveller
18	AA2	Input low-pass filter
19	AA2a	Input filter and mixer
20	AA3	502.6 MHz i.f. filter
21	AA3a	2nd mixer
22	AC2	47.4 MHz i.f. amplifier
23	AC3	2.6 MHz LC filter
24	AC5	2.6 MHz crystal filters
25	AC4	100 kHz i.f. crystal filter
26	AD1	Log amplifier

- PROCEDURES -

AA2 - INPUT LOW-PASS FILTER

Circuit diagram: Chap. 7 Fig. 5

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum Analyzer	Frequency range: 100 Hz to 1 GHz	Marconi 2370 & 2373 extender
Active probe	Frequency range: 100 kHz to 1 GHz	Marconi 2388
Return loss bridge	Frequency range: 10 MHz to 1 GHz Impedance : 50 Ω	Wiltron 62N50

4. AA2 must be set up in situ because AA2a connects to it by a short length of wire which is not screened and thus has an unpredictable effect on the filter's termination.

Initial conditions

5. (1) Disconnect and fold out the AE tray and remove the AA2 lid (see Chap. 5-0).

(2) Select:

PRESET
REF FREQ ..... 0 MHz
ZERO SPAN
RF ATTEN ..... 0 dB

(3) Screw the test port of the return loss bridge directly onto the 2382 INPUT socket.

(4) Connect the test analyzer tracking generator output to the input port on the bridge via a length of double-screened coaxial lead.

(5) Attach the probe to AA2a TP2 via another length of double-screened coaxial lead to the input of the test analyzer. Ground the probe body to the chassis adjacent to TP2.

Setting up

6. (6) Screw C1,C2,C4 and C5 anticlockwise as far as possible or until the rotor is level with the top of the capacitor body.

(7) Screw C3 clockwise as far as possible, then back it off 1 turn.

(8) On the 2370/2373 select:

Vertical scale ..... 10 dB/div
Horizontal scale ..... 10 MHz/div
Top of screen reference ..... -10 dBm
Reference frequency ..... Centre

(9) Adjust the centre frequency by observing the 502.6 MHz signal which the 2382 should be generating. This is due to the first local oscillator from AA7 and will not change in level as the filter is tuned, but the test analyzer tracking generator should cause a notch to be visible at this frequency.

(10) Adjust C2 and C4 to tune the notch to exactly 502.6 MHz as shown by the local oscillator signal. Initially, try to adjust the trimmers by equal amounts. Note that the notch depth gets very deep as correct tune is reached, and great accuracy is not required providing the rejection is greater than 90 dB.

(11) Disconnect the test analyzer input from the probe and connect to the output port on the bridge. Set the test analyzer to 50 MHz/div and to a reference frequency of 250 MHz.

Note ...

The bridge can be calibrated by connecting a 10 dB attenuator in place of the 2382. This will generate a fairly straight line on the test analyzer screen. Adjust the reference level of the test analyzer to put this level 20 dB down from the top of the screen. Return loss can now be measured off directly in dB from the top of screen.

(12) Observe the return loss and adjust C1 and C5, again by equal amounts, to get the best return loss up to 400 MHz.

(13) Adjust C3 slightly to improve the return loss, then repeat from (12) above. As the return loss approaches 15 dB it may be necessary to offset C1 or C5 and compensate with the capacitor at the opposite end thus 'see-sawing' onto the best match.

(14) Always check the notch position after adjusting the return loss.

AA2a - INPUT FILTER & MIXER Circuit diagram: Chap. 7, Fig. 5

TEST EQUIPMENT		
Description	Minimum specification	Example
Coaxial adapter	SMC female to BNC female, 50 Ω	Radiall R191123

Initial conditions

7. (1) Ensure that no frequency response correction figures are stored in the instrument by switching off and on.

(2) Select:

PRESET
TRACK GEN
VERTICAL dB/DIV ..... 0.5 dB
REF LEVEL ..... -5 dBm

(3) Connect the AE7 tracking generator output port to the INPUT socket using the adapter and short coaxial lead. (Ensure that the drive signals from AA9 and AA7 are connected to the rear of the AE tray.)

Calibration

8. (4) Adjust C12 for optimum flatness of the tracking generator signal as displayed on the screen.

(5) Select:

PRESET
REF FREQ ..... 0 MHz
SPAN/DIV ..... 0.5 MHz
RF ATTEN ..... 0 dB
RESOLUTION BANDWIDTH.... 1 MHz

(6) Ensure that nothing is connected to the INPUT socket.

(7) If a notch is present on the displayed response go to (10).

(8) Adjust R35 to minimize the displayed response.

(9) Adjust T1 to tune a notch onto the centre graticule line.

(10) Adjust R35 to maximize the notch depth.

(11) Repeat steps (9) and (10) for the best possible notch at 0 MHz (screen centre).

AA3 - 502.6 MHz IF FILTER Circuit diagram: Chap. 7, Fig. 5

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range: 100 Hz to 100 MHz Tracking generator facility	Marconi 2370

Initial conditions

9. (1) Select:

PRESET
REF FREQ ..... 47.4 MHz
ZERO SPAN
RF ATTEN ..... 0 dB

(2) Connect the 47.4 MHz OUTPUT to the test analyzer input. Connect the test analyzer tracking generator output to the INPUT socket of the 2382.

(3) On the test analyzer select:

Referency frequency ..... 47.4 MHz
Horizontal scale ..... 5 MHz/div
Tracking generator ..... On

Setting up

10. (4) Adjust C1,C2,C3 and C4 for best shape and maximum signal on the test analyzer.

AA3a - 2ND MIXER Circuit diagram: Chap. 7, Fig. 5

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer	Frequency range: 100 Hz to 100 MHz Tracking generator facility	Marconi 2370

Initial conditions

11. (1) Set up as for AA3.

Setting up

12. (2) Adjust C8 and C21 for maximum signal on the test analyzer.

AA4 - SAMPLING GATE Circuit diagram: Chap. 7, Fig. 6

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

13. (1) Select:

PRESET
SPAN/DIV ..... 200 kHz

Setting up

14. (2) Adjust R21 for equal +ve and -ve levels on TP5 and TP6 respectively.

AA5 - MASTER VCO Circuit diagram: Chap. 7, Fig. 7

TEST EQUIPMENT		
	- None required -	

Initial conditions

15. (1) Select:

PRESET
Enter self-test mode (see Chap. 5-3, para. 10)
2nd FUNCT:MKR1 SETS INC FREQ
2nd FUNCT:MARKERS A B SELECT
MARKERS A B SELECT (to set all Ref freq D to A's to 000)

Setting up

16. (2) Adjust R35 for 523 MHz ±5 MHz.

(3) Press MARKERS A B SELECT (to set all D to A's to 255).

(4) Adjust R8 for 950 MHz ±5 MHz.

(5) Remove diagnostics by pressing 2nd FUNCT:ΔF SETS INC FREQ.

(6) Carry out a full synthesizer calibration as described in Chap. 5-3, Diagnostic routines - Mode 5(a).

AA7 - SLAVE VCO Circuit diagram: Chap. 7, Fig. 9

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

17. (1) Set the oscilloscope to X-Y mode.

(2) Set X to 10 V/cm (d.c. to left side of screen).

(3) Set Y to 2 V/cm (d.c. on centre graticule line).

(4) Select PRESET

(5) Attach a compensated oscilloscope x10 probe to the X and Y channels of the oscilloscope.

(6) Connect the X channel probe to PLP pin 4.

(7) Connect the Y channel probe to PLAN.

The oscilloscope now displays the error signal required to track AA7 to AA5 over a full sweep.

Calibration

18. (8) Adjust R30 and R8 for the flattest error voltage around 0 V on the oscilloscope display.

(9) Check that LED D2 on AA8 is not lit.

AA8 - MASTER/SLAVE PHASE DETECTOR Circuit diagram: Chap. 7, Fig. 10

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

19 (1) Connect up as in AA7 but set the oscilloscope Y channel to 100 mV/cm a.c. coupled.

(2) Connect Y channel probe to TP3.

Setting up

20. (3) Adjust R30 for 200 mV pk-pk amplitude signal at the right hand side of the oscilloscope display.

(4) Remove connection to PLAM.

(5) Rotate R28 to its end stop which leaves LED D2 lit.

(6) Reconnect connection to PLAM.

(7) Adjust R12 for centre of range where D2 is extinguished.

(8) Check for each of the 3 horizontal reference positions (LH, Centre and RH) that LED D2 does not light (this suggests break of phase lock).

(9) Change SPAN/DIV to 2 MHz and again check for correct lock.

(10) Disconnect probes.

AA9 - 2nd LOCAL OSCILLATOR VCO Circuit diagram: Chap. 7, Fig. 11

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

21. (1) Set the oscilloscope to 100 ms/cm, auto trigger.

(2) Set the oscilloscope CH1 to 0.5 V/cm vertical, d.c. coupled, 0 V on centre graticule line.

(3) Connect the probe to TP6 on AA10.

Setting up

22. (4) Adjust R6 and record the maximum and minimum d.c. voltage levels that can be obtained before lock is broken (i.e. no search signal present on the oscilloscope display).

(5) Reset R6 for mid-point.

(6) Remove the probe.

AB1 - D-A CONVERTER Circuit diagram: Chap. 7, Fig. 14

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

23. (1) Connect the d.v.m. to TP22.

Setting up

24. (2) Adjust R76 for +15 V d.c.

AB2 - INTERPOLATION OSCILLATOR Circuit diagram: Chap. 7, Fig. 8

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

25. (1) Select:

PRESET
SPAN/DIV ..... 2 kHz
Enter Self test mode (see Chap. 5-3, para. 10)
2nd FUNCT:MKR1 SETS INC FREQ
2nd FUNCT:MARKERS A B SELECT

Setting up

26. (2) Tune T1 for 32.85 MHz or minimum frequency, whichever is the greater.

(3) Press MARKERS A B SELECT to set all Ref freq D to A's to their minumum preset values.

(4) Connect the d.v.m. positive lead to PLN pin 5 and the negative lead to ground. Adjust MARKERS MOVE control until a reading of +1.5 V is obtained.

(5) Check that the frequency displayed on the screen is greater than 28 MHz.

(6) Remove diagnostics by pressing 2nd FUNCT:ΔF SETS INC FREQ.

(7) Carry out a full synthesizer calibration as described in Chap. 5-3, Diagnostic routines - Mode 5(a).

AB3 - MASTER VCO Circuit diagram: Chap. 7, Fig. 17

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

27. (1) Select:

PRESET
SPAN .....5 kHz/DIV
Enter Self-test mode (see Chap. 5-3, para. 10)
2ndFUNCT:MKR1 SETS INC FREQ
2nd FUNCT:MARKERS A B SELECT (to set all D to A's to 255)

Setting up

28. (2) Tune T1 for 34.35 MHz or minimum frequency, whichever is the greater.

(3) Press MARKERS A B SELECT to set all Ref freq D to A's to their minimum preset values.

(4) Connect the d.v.m. positive lead to PLX pin 4 and the negative lead to ground. Adjust the MARKERS MOVE control until a reading of +1.5 V is obtained.

(5) Check that the frequency displayed on the screen is greater than 26.25 MHz.

(6) Remove diagnostics by pressing 2nd FUNCT:ΔF SETS INC FREQ.

(7) Carry out a full synthesizer calibration as described in Chap. 5-3, Diagnostic routines - Mode 5(a).

AB4 - SAMPLING GATE Circuit diagram: Chap. 7, Fig. 17

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

29. (1) Select:

PRESET
SPAN/DIV ..... 500 kHz

(2) Disconnect PLY from AB3.

(3) Connect the d.v.m. to TP9.

Setting up

30. (4) Adjust R21 for zero volts on TP9.

(5) Disconnect the d.v.m.

(6) Reconnect PLY.

AB5 - SLAVE VCO Circuit diagram: Chap. 7, Fig. 18

TEST EQUIPMENT		
Description	Minimum specification	Example
Counter Digital voltmeter	Frequency range: 10 Hz to 500 MHz Function : d.c. volts	Marconi 2432A Solartron 7150

Initial conditions

31. (1) Select:

PRESET
SPAN/DIV ..... 5 kHz
Enter Self-test mode (See Chap. 5-3, para. 10)
2nd FUNCT:MKR1 SETS INC FREQ
2nd FUNCT:MARKERS A B SELECT (to set all D to A's to 255)

32. Setting up

(2) Press MARKERS A B SELECT to set all Ref freq D to A's to their minimum preset values.

(3) Connect the frequency counter to TP4.

(4) Connect the d.v.m. positive lead to PLAK and the negative lead to ground. Adjust the MARKERS MOVE control until a reading of +1.5 V is obtained.

(5) Remove PLAF and PLAE. Short PLAE pins 3 and 4 to ground.

(6) Adjust L1 for 900 kHz higher than AB3 frequency as displayed on the screen.

(7) Remove diagnostics by pressing 2nd FUNCT:ΔF SETS INC FREQ.

(8) Remove the short and reconnect PLAF and PLAE. Disconnect the d.v.m.

(9) Carry out a full synthesizer calibration as described in Chap. 5-3, Diagnostic routines - Mode 5(a).

AC1 - 50 MHz CRYSTAL OSCILLATOR Circuit diagram: Chap. 7, Fig. 20

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

33. (1) Set the oscilloscope to 0.05 µs/cm, auto trigger.

(2) Set the oscilloscope CH1 to 500 mV/cm, a.c. coupled, 0 V centre horizontal graticule line.

(3) Connect CH1 input to TP2 via the x 10 probe.

Setting up

34. (4) Adjust L2 for maximum signal level.

(5) Set CH1 to 200 mV/DIV and connect the probe to AC6 TP4.

(6) Adjust L3 for 0 V as displayed on the oscilloscope.

AC2 - 47.4 MHz IF AMPLIFIER

Circuit diagram: Chap. 7, Fig. 21

TEST EQUIPMENT		
Description	Minimum specification	Example
Spectrum analyzer Active probe	Frequency range: 100 Hz to 100 MHz Frequency range: 100 kHz to 1 GHz	Marconi 2370 Marconi 2388

Initial conditions

35. (1) Select:

PRESET
REF FREQ ..... 47.4 MHz
ZERO SPAN

(2) On the test analyzer select:

Reference frequency ..... 47.4 MHz
Horizontal scale ..... 1 MHz/div
Vertical scale ..... 1 dB/div
Tracking generator ..... On
Reference level ..... -20 dBm

(3) Set the probe to 0 dB attenuation.

(4) Connect the probe to the test analyzer input.

(5) Connect the test analyzer tracking generator output to PLA using a suitable adapter.

(6) Connect the probe tip to TP1. (Ground the probe to the filter case).

Setting up

36. (7) Screw C9, C11, C13 fully in and C15 fully out.

(8) Tune C9 for peak at 47.4 MHz on TP1.

(9) Tune C11 for a notch at 47.4 MHz on TP1.

(10) Tune C13 for a peak at 47.4 MHz on TP1.

(11) On the test analyzer change to:

Vertical scale ..... 10 dB/div
Reference level ..... 0 dBm

(12) Connect the probe to TP3.

(13) Tune C15 for a symmetrical response 20 dB down.

(14) On the test analyzer change to:

Reference frequency ..... 52.6 MHz

(15) Connect the probe to TP1.

(16) Adjust C4 for a notch at 52.6 MHz.

(17) Adjust R21 to maximize the notch at 52.6 MHz.

(18) Disconnect the probe.

AC3 - 2.6 MHz LC FILTER Circuit diagram: Chap. 7, Fig. 22

TEST EQUIPMENT		
	- None required -	

Initial conditions

37. (1) Switch the SUPPLY off and back ON. This sets the i.f. and filter tune lines to their preset values.

(2) Select:

PRESET
REF FREQ ..... 10 MHz
RESOLUTION BANDWIDTH ..... 10 kHz
ZERO SPAN
VERTICAL A B SELECT ..... A
VERTICAL dB/DIVISION ..... 1 dB
VERTICAL A B SELECT ..... B
VERTICAL dB/DIVISION ..... 1 dB
B VIEW

(3) Connect STD 10 MHz OUTPUT to INPUT.

(4) Remove power from the board by disconnecting PLH, then desolder the link between TP9 and TP10, and reconnect PLH.

(5) Link TP10 to TP3 with a shorting link.

(6) Select B SAVE (Stores level on B trace).

(7) Link TP10 to TP4 with a shorting link.

Setting up

38. (8) Adjust C12 for a peak display and equalize the level with R39.

(9) Link TP10 to TP5 with a shorting link.

(10 Adjust C22 for a peak display.

(11) Link TP10 to TP6 with a shorting link.

(12) Adjust C32 for a peak display and equalize the level with R79.

(13) Link TP10 tro TP7 with a shorting link.

(14) Adjust C42 for a peak display.

(15) Link TP10 to TP8 with a shorting link

(16) Adjust C52 for a peak display and equalize the level with R119.

(17) Disconnect PLH, remove the shorting link and resolder the original link between TP9 and TP10.

(18) Reconnect PLH.

AC4 - 100 kHz IF XTAL FILTER Circuit diagram: Chap. 7, Fig. 24

TEST EQUIPMENT		
Description	Minimum specification	Example
Frequency standard	Accuracy: 1 part in 10^6	

Initial conditions

39. (1) Switch SUPPLY off and back ON. (This sets the i.f. gain and filter tune lines to their preset value).

(2) Select:

PRESET
REF FREQ ..... 10 MHz
SPAN/DIV ..... 10 MHz
VERTICAL A B SELECT ..... A
VERTICAL dB/DIVISION ..... 0.5 dB
TRACK GEN
RESOLUTION BANDWIDTH ..... 3 Hz
REF LEVEL ..... -5 dBm

(3) Connect the external standard to EXT STD on the rear panel.

(4) Connect TRACK GEN to INPUT.

Setting up

40. (5) Set R30,R39,R59,R79 and R99 fully clockwise.

(6) Tune C23,C43,C63,C83 and C103 for maximum level.

(7) Change:

SPAN/DIV ..... 100 Hz
VERTICAL dB/DIV ..... 10 dB
RESOLUTION BANDWIDTH ..... 30 Hz

(8) Connect STD 10 MHz OUTPUT to INPUT.

(9) Desolder link between TP11 and TP12.

(10) Link TP12 and TP4 with a shorting link.

(11) Adjust R25 for symmetry.

(12) Change to:

SPAN/DIV ..... 20 Hz
VERTICAL dB/DIVISION ..... 1 dB

(13) Adjust C32 to centre the response on the dotted vertical reference line.

(14) Link TP2 to TP3 with a 100 nF capacitor.

(15) Link TP12 to TP6 with a shorting link.

(16) Change to:

SPAN/DIV ..... 100 Hz
VERTICAL dB/DIVISION ..... 10 dB

(17) Adjust R45 for skirt symmetry.

(18) Change to:

SPAN/DIV ..... 20 Hz
VERTICAL dB/DIVISION ..... 1 dB

(19) Adjust C52 to centre the response on the dotted vertical reference line.

(20) Link TP2 to TP7 with the 100 nF capacitor.

(21 Link TP12 to TP10 with a shorting link.

(22) Change to:

SPAN/DIV ..... 100 Hz
VERTICAL dB/DIVISION ..... 10 dB

(23) Adjust R65 for skirt symmetry.

(24) Change to:

SPAN/DIV ..... 20 Hz
VERTICAL dB/DIVISION ..... 1 dB

(25) Adjust C72 to centre the response on the dotted vertical reference line.

(26) Link TP2 to TP7 with the 100 nF capacitor.

(27) Link TP12 to TP10 with a shorting link.

(28) Change to:

SPAN/DIV ..... 100 Hz
VERTICAL dB/DIVISION ..... 10 dB

(29) Adjust R85 for skirt symmetry.

(30) Change to:

SPAN/DIV ..... 20 Hz
VERTICAL dB/DIVISION ..... 1 dB

(31) Adjust C92 to centre the response on the dotted vertical reference line.

(32) Link TP2 to TP9 with the 100 nF capacitor.

(33) Link TP12 to TP11 with a shorting link.

(34) Change to:

SPAN/DIV ..... 100 Hz
VERTICAL dB/DIVISION ..... 10 dB

(35) Adjust R105 for skirt symmetry.

(36) Change:

SPAN/DIV ..... 20 Hz
VERTICAL dB/DIVISION .... 1 dB

(37) Adjust C112 to centre the response on the dotted vertical reference line.

(38) Remove the 100 nF capacitor and link.

(39) Change to:

SPAN/DIV ..... 10 Hz
RESOLUTION BANDWIDTH .... 1 MHz
B VIEW
VERTICAL A B SELECT ..... B
VERTICAL dB/DIVISION .... 1 dB
TRACK GEN

(40) Connect TRACK GEN to INPUT.

(41) Press B SAVE (Stores reference level in B store).

(42) Change to:

RESOLUTION BANDWIDTH .... 3 Hz.

(43) Adjust R13 to equalize the level with that of the stored trace.

(44) Change to:

RESOLUTION BANDWIDTH .... 30 Hz

(45) Adjust R17 to equalize the level with that of the stored trace.

(46) Change to:

RESOLUTION BANDWIDTH .... 10 Hz

(47) Adjust R15 to equalize the level with that of the stored trace.

AC5 - 2.6 MHz CRYSTAL FILTERS

Circuit diagram : Chap. 7, Fig. 26

TEST EQUIPMENT
- None required -

Initial conditions

41. (1) Switch SUPPLY off and back ON. (This sets i.f. gain and filter tune lines to their preset voltage).

(2) Select:

PRESET
REF LEVEL ..... -5 dBm
REF FREQ ..... 10 MHz
SPAN/DIV ..... 100 Hz
RESOLUTION BANDWIDTH ..... 100 Hz
VERTICAL dB/DIVISION ..... 0.5 dB
TRACK GEN

(3) Connect TRACK GEN to INPUT.

Setting up

42. (4) Tune C12,C22,C33,C42 and C53 for maximum display value.

(5) Remove power from the board by disconnecting PLL, then unsolder the link from between TP11 and TP12 and reconnect PLL.

(6) Connect 10 MHz STD to INPUT.

(7) Change to:

SPAN/DIV ..... 20 kHz
RESOLUTION BANDWIDTH ..... 3 kHz/DIV (not AUTO)
B VIEW
VERTICAL A B SELECT ..... B
VERTICAL dB/DIVISION ..... 10 dB
MARKERS A B SELECT ..... B
PEAK FIND
MKR1 SETS REF FREQ

(8) Connect the shorting link between TP4 and TP12.

(9) Tune C9 for skirt symmetry.

(10) Change to:

SPAN/DIV ..... 2 kHz

(11) Tune L2 for centre frequency (note the response will dip at the centre frequency).

(12) Refit the link to connect TP12 and TP6.

(13) Change to:

SPAN/DIV ..... 10 kHz
PEAK FIND
MKR1 SETS REF LEVEL

(14) Tune C20 for skirt symmetry.

(15) Change to:

SPAN/DIV ..... 1 kHz

(16) Tune L3 for centre frequency.

(17) Refit the link to connect TP12 to TP8.

(18) Change to:

SPAN/DIV ..... 10 kHz
PEAK FIND
MKR1 SETS REF LEVEL

(19) Tune C31 for skirt symmetry.

(20) Change to:

SPAN/DIV ..... 1 kHz

(21) Tune L4 for centre response.

(22) Refit the link to connect TP12 to TP10.

(23) Change to:

SPAN/DIV ..... 5 kHz/DIV
PEAK FIND
MKR1 SETS REF LEVEL

(24) Tune C40 for skirt symmetry.

(25) Change to:

SPAN/DIV ..... 1 kHz

(26) Tune L5 for centre response.

(27) Remove PLL and resolder the link between TP12 and TP11. Reconnect PLL.

(28) Change to:

SPAN/DIV ..... 5 kHz
PEAK FIND
MKR1 SETS REF LEVEL

(29) Tune C51 for skirt symmetry.

(30) Change to:

SPAN/DIV ..... 1 kHz

(31) Tune L6 for centre response.

(32) Connect TRACK GEN to INPUT.

(33) Change to:

VERTICAL A B SELECT ..... B
VERTICAL dB/DIVISION ..... 0.5 dB
RESOLUTION BANDWIDTH ..... 1 MHz
TRACK GEN
REF LEVEL ..... -5 dB
B SAVE
RESOLUTION BANDWIDTH ..... 300 Hz

(34) Adjust R11 to equalize the level with the stored trace.

(35) Change to:

RESOLUTION BANDWIDTH ..... 100 Hz

(36) Adjust R7 to equalize the level with the stored trace.

AD1 - LOG AMPLIFIER Circuit diagram: Chap. 7, Fig. 29

TEST EQUIPMENT		
Description	Minimum specification	Example
Signal generator Step attenuator	Frequency range: 1 MHz to 500 MHz 40 dB ±0.2 dB	Marconi 2018A Hewlett Packard 8495A

Initial conditions

43. (1) Select:

PRESET
REF FREQ ..... 10 MHz
SPAN/DIV ..... 100 kHz
RESOLUTION BANDWIDTH ..... 10 kHz
VERTICAL VOLTS/DIV ..... 1 V full-scale
MKR1

(2) With no input connected adjust R207 until the marker reads between 0.000 and 0.005 V (Note that when correctly set the marker reading will change between values within this range).

(3) Change to:

PRESET
RF ATTEN ..... 0 dB
RESOLUTION BANDWIDTH ..... 30 kHz
REF LEVEL ..... 21 dB
VERTICAL dB/DIVISION ..... 0.5 dB
MKR1
MARKERS 1 2 MOVE 1

(4) Connect 10 MHz STD OUTPUT to INPUT.

Setting up

44. (5) Carefully position the marker half way down the right side of the response.

(6) Change to:

MKR1 SETS REF FREQ
SPAN/DIV ..... 1 kHz

(7) Adjust R155 so as to remove any discontinuity or snotchet on the trace - see Fig. 1 and Table 2.

Snotchets are steps appearing in the analyzer's response caused by incorrect attenuator settings, which may be as large as ±0.5 dB in an uncalibrated AD1. With the instrument set to -10 dBm top of screen (TOS) (for a log amp input of +16 dBm), then the snotchets, of which there are seven in all, will occur at the points given in Table 2.

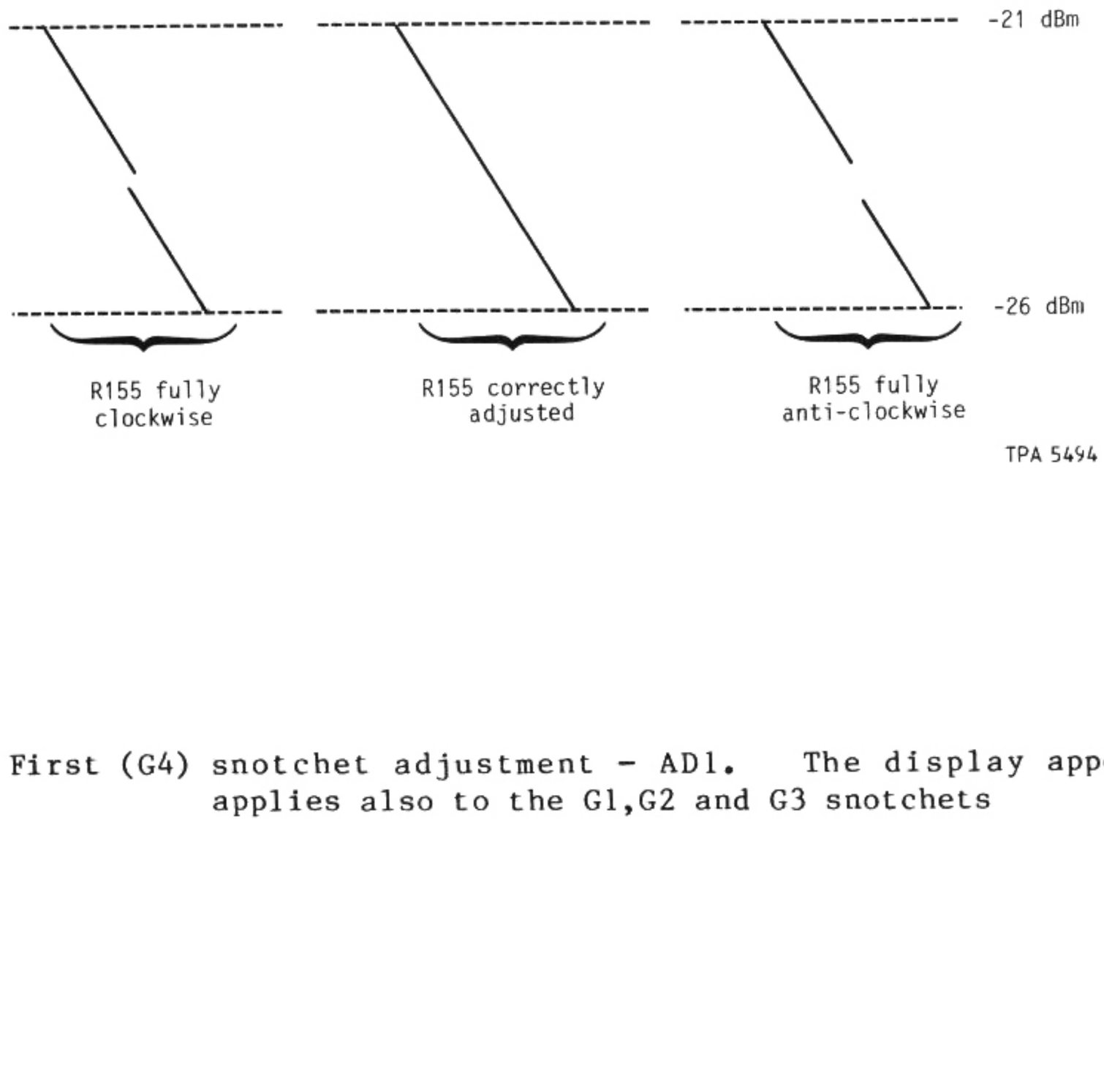


Fig. 1 First (G4) snotchet adjustment - AD1. The display appearance applies also to the G1,G2 and G3 snotchets

TABLE 2 ATTENUATOR SWITCH ADJUSTMENT - AD1

SNOTCHET NO.	ADJUSTMENT	SCREEN LEVEL (dBm)	LOG AMP INPUT LEVEL (dBm)
TOS	-	-10.0	+16
1	R155 (G4)	-23.998	+2.7016
2	R39 (G1)	-35.396	-9.396
3	-	-48.898	-22.898
4	R77 (G2)	-60.996	-34.996
5	-	-74.498	-48.498
6	R115 (G3)	-86.596	-60.596
7	-	-100.098	-74.098

Adjustments must be made in the order G4,G1,G2,G3

(8) Change to:

REF LEVEL ..... 32.5 dBm
SPAN/DIV ..... 50 kHz

(9) Again position the marker halfway down the right side of the response.

(10) Change to:

MKR1 SETS REF FREQ
SPAN/DIV ..... 1 kHz

(11) Adjust R39 so as to remove any discontinuity on the trace.

(12) Change to:

REF FREQ ..... 10 MHz
RESOLUTION BANDWIDTH ..... 100 Hz
SPAN/DIV ..... 100 Hz

(13) Insert the 40 dB pad between STD 10 MHz OUTPUT and INPUT.

(14) Again adjust the marker halfway down the right side of the response.

(15) Change to:

MKR1 SETS REF FREQ
SPAN/DIV ..... 10 Hz

(16) Adjust R77 so as to remove any discontinuity on the trace.

(17) It is not possible to calibrate the sixth snotchet by the above technique, set R115 midway. The inability to set this snotchet is of minor importance, since it is close to the instrument's phase noise floor and is lost or masked by measurement uncertainty.

(18) Change to:

PRESET
RESOLUTION BANDWIDTH ..... 1 MHz
VERTICAL dB/DIVISION ..... 10 dB
REF LEVEL ..... -10 dBm
MKR1
CAL

(19) Apply a known -10 dBm, 10 MHz signal to the INPUT socket.

(20) Adjust R207 so that the marker reading on the display reads -10.00 dBm ±0.05 dB.

(21) Change to:

PRESET
REF FREKQ ..... 10 MHz
SPAN/DIV ..... 200 kHz
RF ATTEN ..... 20 dB
MKR1
PEAK FIND
VOLTS/DIV

(22) Using the REF LEVEL controls select a full-scale setting of 100 mV.

(23) Make a note of the marker reading.

(24) Shift down one range to 50 mV full-scale.

(25) Adjust R164 so that the new marker reading equals that noted in (23) above.

AD4 - 10 MHz CALIBRATOR Circuit diagram: Chap. 7, Fig. 39

TEST EQUIPMENT		
Description	Minimum specification	Example
Frequency counter	To measure 10 MHz with an accuracy of ±1 part in 10^6.	Marconi 2432A with ext. freq. standard.
Signal generator	Frequency: 10 MHz	Marconi 2018A

Initial conditions

45. (1) After switching on allow 15 minutes for the TCXO to reach thermal equilibrium.

(2) Turn the back panel SET INT STD control fully anticlockwise into the detent.

(3) Connect the frequency counter to the STD 10 MHz OUTPUT socket.

Setting up

46. (4) Adjust R2 to obtain a reading of 10.00000 MHz.

(5) Change to:

PRESET
REF FREQ ..... 10 MHz
REF LEVEL ..... -8 dBm
VERTICAL dB/DIVISION .... 0.5 dB (for both A and B traces)
SPAN/DIV ..... 1 kHz
B VIEW

(6) Connect an accurate 10 MHz, -10 dBm signal to the INPUT socket.

(7) Store the level on the screen by pressing B SAVE.

(8) Connect STD 10 MHz OUTPUT to INPUT.

(9) Adjust R22 to give the same level on the screen as that stored on the B trace.

AE1 - 47.4 MHz CRYSTAL OSCILLATOR Circuit diagram: Chap. 7, Fig. 41

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

47. (1) Set the oscilloscope to 0.05 µs auto trig, CH1 0.1V/DIV and connect it to TP9 via the x10 probe.

(2) Set CH2 of the oscilloscope to 1V/DIV and connect to TP8 via the x10 probe.

(3) Select:

PRESET
TRACK GEN

Setting up

48. (4) Adjust L1 for a 47.4 MHz waveform on TP9 and 0 V on TP8 simultaneously.

(5) Set the oscilloscope to X Y mode, Y deflection 2V/DIV, d.c. centre graticule, X deflection 10V/DIV, d.c. left hand graticule.

(6) Connect the Y channel of the oscilloscope to PLE to monitor the a.l.c. loop voltage.

(7) Connect the X channel of the oscilloscope to AB1 TP9 to monitor the master oscillator sweep voltage.

(8) Adjust R17 for an average working level of -5 V as shown on the oscilloscope screen.

(9) Disconnect the oscilloscope probes.

AE3 - 502.6 MHz BAND-PASS FILTER Circuit diagram: Chap. 7, Fig. 42

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

49. (1) Select:

PRESET
TRACK GEN

(2) Set the oscilloscope to X Y mode, Y deflection 2V/DIV, d.c. centre graticule, X deflection 10V/DIV, d.c. left hand graticule.

(3) Connect the Y channel of the oscilloscope to PLE to monitor the a.l.c. loop voltage.

(4) Connect the X channel of the oscilloscope to AB1 TP9 to monitor the master oscillator sweep voltage.

Setting up

50. (5) Adjust C1,C2,C3 and C4 for maximum positive voltage displayed on the oscilloscope.

AE5 - 400 MHz LOW-PASS FILTER Circuit diagram: Chap. 7, Fig. 43

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235

Initial conditions

51. (1) Select:

PRESET
TRACK GEN

(2) Set the oscilloscope to X Y mode, Y deflection 2V/DIV, d.c. centre graticule, X deflection 10V/DIV, d.c. left hand graticule.

(3) Connect the Y channel of the oscilloscope to PLE to monitor the a.l.c. loop voltage.

(4) Connect the X channel of the oscilloscope to AB1 TP9 to monitor the master oscillator sweep voltage.

Setting up

52. (5) Adjust C1 and C4 for maximum positive voltage displayed on the oscilloscope.

AE6 - AMP/LEVELLER Circuit diagram: Chap. 7, Fig. 44

TEST EQUIPMENT		
Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235
Coaxial adapter	SMC female to N female, 50 Ω	Radiall R191147
Power meter	Frequency range: up to 500 MHz	Marconi 6960 & 6912 sensor
Spectrum analyzer	Frequency range: 100 Hz to 1 GHz	Marconi 2370 & 2373 extender

Note ...

All adjustments should be made with the AE tray lid fitted.

Initial conditions

53. (1) Select:

PRESET
TRACK GEN
SWEEP TIME ..... 1 s/DIV

(2) Disconnect the tracking generator and calibrator solid coaxial connections from the front of the AE tray. Slightly raise the front of the tray so as to gain access to these sockets, being careful not to strain the rear solid coaxial links from AA7 and AA9.

(3) Connect the 2373 input socket to the TRACKING GENERATOR output using a suitable adapter.

Setting up

54. (4) Adjust R12 for minimum harmonic content on the tracking generator output signal as it is swept from 0 to 400 MHz (R12 affects the complete calibration of the tracking generator and therefore should always be set up first).

(5) Change to:

PRESET
REF FREQ..... 50 MHz
ZERO SPAN
TRACK GEN

(6) Connect a calibrated power meter to AE7 calibrator output port using the adapter.

(7) Set the power meter averaging to 4.

(8) Change to:

Enter Self test mode (see Chap. 5-3, Diagnostic routines)
CAL (to enter debug mode)
2ND FUNCT:MKR1 SETS REF FREQ (to switch on the internal calibrator signal)

(9) Adjust R60 for exactly -10.00 dBm as displayed on the power meter.

(10) Change to:

REF FREQ ..... 350 MHz

(11) Adjust R12 AE7 for exactly -10.00 dBm as displayed on the power meter.

(12) Disconnect the power meter from the AE7 calibrator output and connect to AE6 tracking generator output port.

(13) Change to:

PRESET
CAL (to enter debug mode)
2ND FUNCT:MKR1 SETS REF LEVEL
MARKERS A B SELECT to select B
2ND FUNCT:MKR1
REF FREQ ..... 50 MHz

(14) Rotate the MARKERS MOVE control to set the tracking generator D to A at 255 as displayed on the 2380 screen.

(15) Adjust R50 for -9.5 dBm on the power meter.

(16) Change to:

REF FREQ ..... 350 MHz

(17) Adjust R35 for -9.5 dBm on the power meter.

(18) Change to:

REF FREQ ..... 50 MHz

(19) Rotate the MARKERS MOVE control to set the tracking generator D to A at 000.

(20) Adjust R55 for -20.5 dBm on the power meter.

(21) Calibrate the tracking generator using the procedure described in Chap. 5-3, Diagnostic routines - Mode 5(a).

AE7 - CAL SWITCH Circuit diagram: Chap. 7, Fig. 44

55. Adjustments on this board are performed when calibrating AE6.

AR2 - POWER SUPPLY INTERFACE Circuit diagram: Chap. 7, Fig. 52

TEST EQUIPMENT		
Description	Minimum specification	Example
Digital voltmeter	Function: d.c. volts	Solartron 7150

Initial conditions

56. (1) Select:

PRESET

57. Setting up

(2) Connect the d.v.m. to TP4.

(3) Adjust R8 for a reading of +15.0 ±0.05 V.

(4) Connect the d.v.m. to TP1.

(5) Adjust R2 for a reading of -5.5 V ±0.05 V.

(6) Connect the d.v.m. to TP2.

(7) Adjust R5 for a reading of -15.0 ±0.05 V.

Chapter 5-3

FAULT DIAGNOSIS

CONTENTS

Para.
1 General procedure
6 Fuse replacement

- Diagnostic routines -
7 Introduction
10 Access to self-test and self-cal modes
13 Mode 1 - Display synthesizer conditions
28 (a) - Oscillator measurement delay
29 (b) - Sweep flyback delay
31 Mode 2 - Trace
35 Mode 3 - Examine master oscillator frequencies
41 Mode 4 - Calibration test routines
46 (a) - Check filter tuning and level
50 (b) - Swept D to A checks
51 (c) - View internal calibrator signal
52 (d) - Decade calibrations only
53 (e) - Full calibration in debug mode
54 Mode 5 - Oscillator voltage/frequency calibration
63 (a) - Full synthesizer calibration
65 (b) - Single oscillator calibration
67 (c) - Single oscillator linearizer control
68 (d) - Sweep gain adjust control
69 Mode 6 - Tracking generator calibration
72 Mode 7 - Error codes
73 Menu driven diagnostic tests
83 Signal path levels
83 Levels
85 Attenuator and gain settings
86 Filter selection

- Board check-out procedures
87 AA1a - Input attenuator
88 AA2a - Input filter and mixer
89 AA3, AA3a - 502.6 MHz i.f. filter and 2nd mixer
93 AA4 - Sampling gate
94 AA5 - Master VCO
95 AA6 - Divider
96 AA7 - Slave VCO
97 AA8 - Master/slave phase detector
98 AA9 - 2nd local oscillator VCO
99 AA10 - Sampling gate

CONTENTS (continued)

Para.
100 AA11 - Line cleaner
101 AB1 - D to A board
102 AB2 - Interpolation oscillator
103 AB3 - Master VCO
104 AB4 - Sampling gate
105 AB5 - Slave VCO
106 AB6 - Phase detector
107 AB7 - Oscillator select
108 AB8 - Overload detector
109 AC1 - 50 MHz crystal oscillator
110 AC2 - 47.4 MHz i.f. amplifier
118 AC3 - 2.6 MHz LC filter
119 AC4 - 100 kHz i.f. crystal filter
120 AC5 - 2.6 MHz crystal filters
121 AC6 - Phase detector
122 AD1 - Log amplifier
123 AD2 - Log amplifier interface
125 AD3 - Microprocessor board
135 AD4 - 10 MHz calibrator
136 AE1 - 47.4 MHz crystal oscillator
137 AE2 - Buffer
138 AE3a - Narrow band mixer/buffer
139 AE4 - Tracking generator buffer
140 AE5a - Wide band mixer/buffer
141 AE6 - Amplifier/leveller
142 AE7 - Cal switch
143 AR2 - Power supply interface

Table Page
1 Error message list 62
2 dBm/mV conversion 69
3 Auto mode log operation - attenuator and gain settings 71
4 Auto mode lin operation - attenuator and gain settings 72
5 IF attenuator selection 73
6 IF filter selection 73
7 IF attenuation selection logic 90

Fig.
- Fault location charts -
1 Overview 5/6
2 Top level 7
3 Top level, overall system 18

CONTENTS (continued)

Fig.		Page
4	DATA LINK section	19
5	SWEEP MODE SINGLE ARM	20
6	Failure to PRESET	23
7	RF/IF gain switching	24
8	Tracking generator fault	25
9	Wrong system gain	28
10	Power system	29
11	10 MHz STD fault	30
12	Filter bandwidth	31
13	Linearization	32
14	Synthesizer fault	33
15	LOG AMP fault	36
16	RF/IF gain switching fault	37
17	CAL fault	38
18	Filter bandwidth fault	41
19	Marker controls	42
20	Logic section - frequency count	43
21	Auto trig diagnostics	43
22	Line trig diagnostics	44
23	EXT trig diagnostics	44
24a	Overlayed sampled ZERO SPAN diagnostics	45
24b	No VIDEO trigger	45
25	Sampled ZERO SPAN diagnostics	46
26	Triggering diagnostics	46
27	Signal path levels for auto log operation (3 Hz to 3 kHz bandwidths	65/66
28	Signal path levels for auto log operation (10 kHz to 1 MHz bandwidths	67/68

Annex A Synthesizer fault location

Annex B Auxiliary information
Linearization
Frequency count

GENERAL PROCEDURE

1. If a fault is suspected, go first to the overall fault location chart. This will indicate, by reference to display symptoms, which function is suspect. The branches will lead you to area fault location charts and board check-out procedures or to diagnostic routines which should localize the fault to a relatively small group of components or functional area.

2. At the same time it is useful to look at the overall block diagrams in Chap. 4 which show the relationship between functional areas and may suggest possible causes and effects. These diagrams also indicate the next level of block diagram where a more detailed treatment is given. For a complete understanding of the fault you should read the relevant part of the technical description in conjunction with the circuit diagrams.

3. A further guide to detailed fault location is provided by the test point waveforms and data shown opposite the circuit diagrams.

4. Test equipment recommended for fault finding is listed in Chap. 5-0.

5. Note that performance limits quoted in this chapter are for guidance only and should not be taken as guaranteed performance specifications unless they also appear in the Performance Data in Chap. 1.

FUSE REPLACEMENT

6. Either one or two cartridge-type fuses are located on the 2382 rear panel. These main supply fuses are slow blow, 4 A for 95 to 130 V a.c. and 2.5 A for 190 to 260 V a.c. A 3.15 A quick acting fuse on board AR2 protects the +5 V logic supply. Switch off the power supply when replacing a fuse.

FAULT CHART LOCATION

Fig. 2:

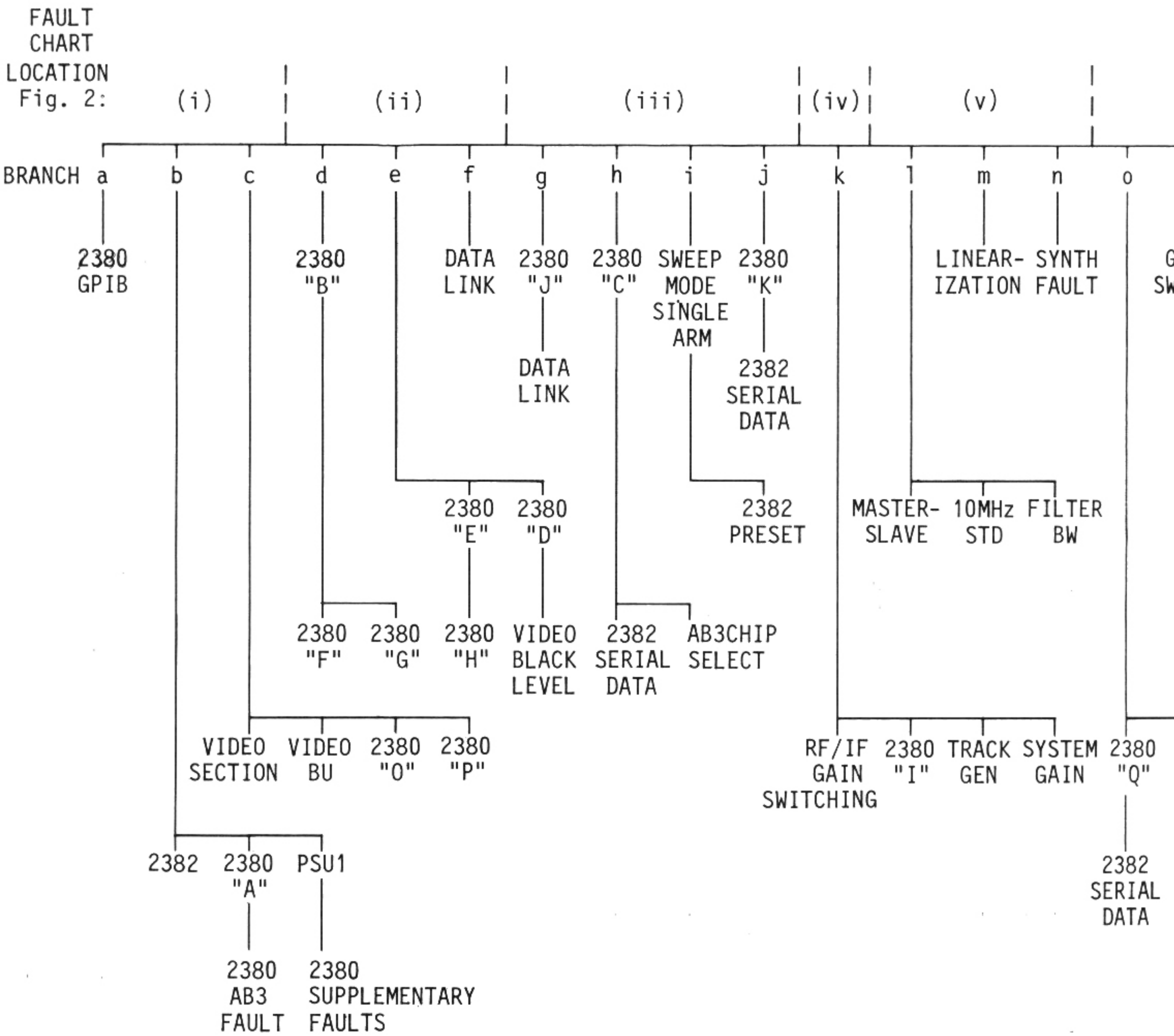
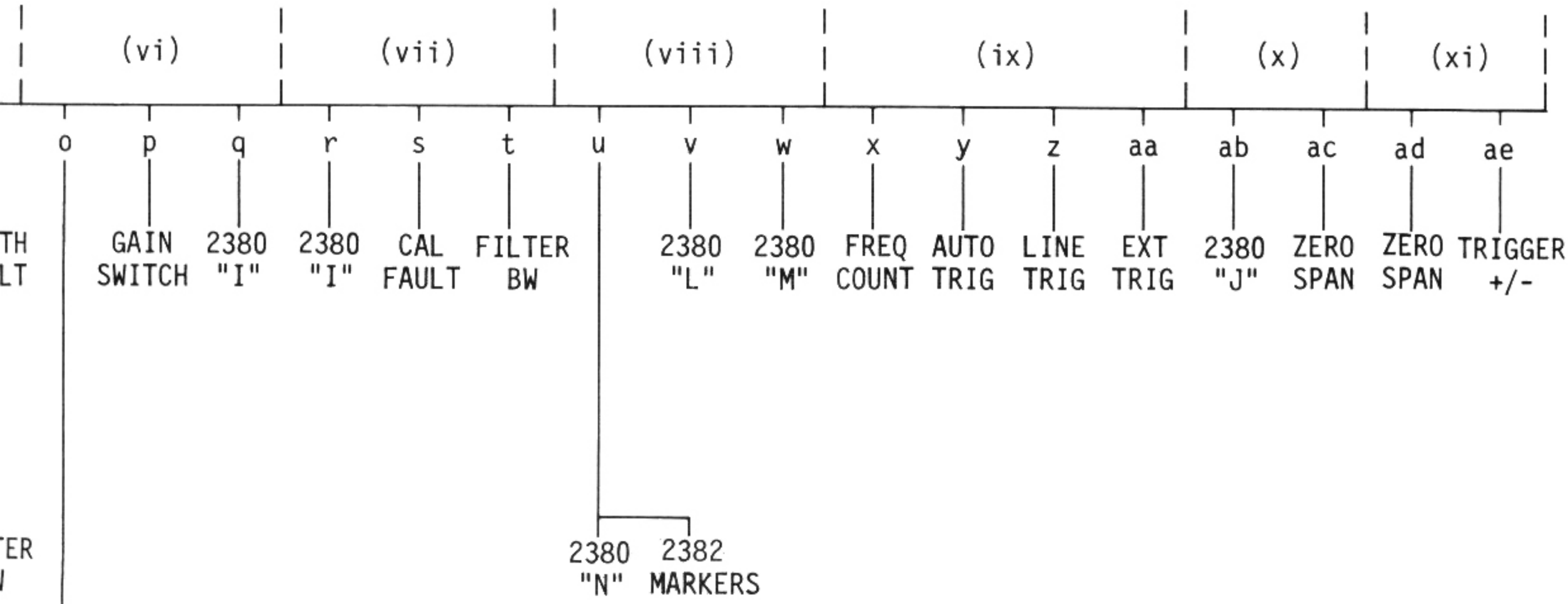


Fig. 1 Fault loca

May 86



This fault tree summarizes the structure of the Top Level charts, Figs. 2(i) to 2(xi). Each functional area or topic is grouped into 31 branches, designated a to ae, and each chart gives a fault location procedure related to the branch(es) indicated.

This enables you to go quickly to the correct chart if a particular topic is suspect. For example, if you think that the video black level is faulty go to step (e) of Fig. 2(ii). If the faulty area is unknown, start at Fig. 2(i), and work systematically through the charts. Note that with topics prefixed 2380 you may be referred to fault location charts in the Display Unit manual.

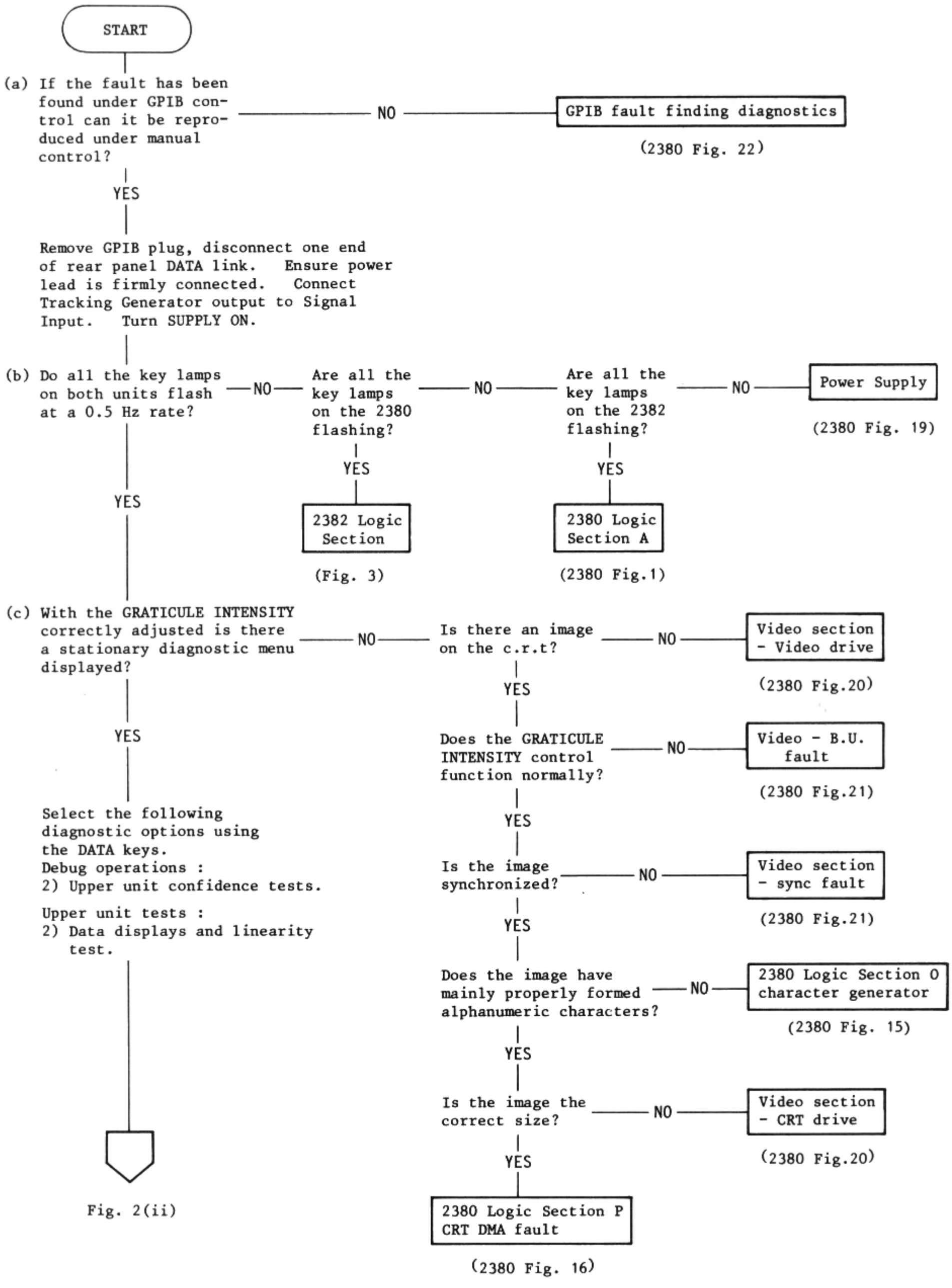


Fig. 2(ii)

Fig. 2(i) Fault location chart - top level, overall system

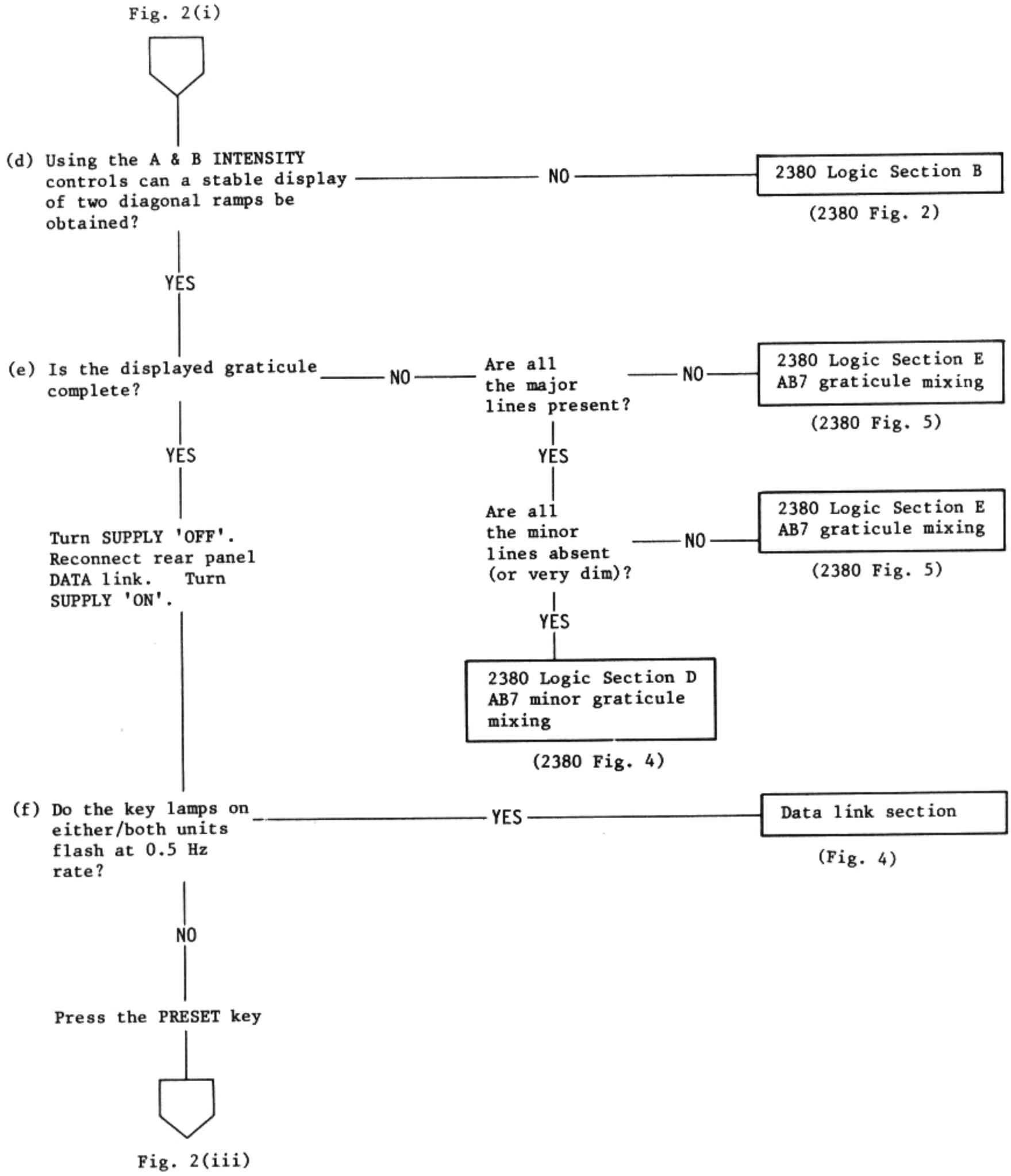


Fig. 2(ii) Fault location chart - top level, overall system

Fig. 2(ii)

(g) Is the display graticule synchronized? — NO — 2380 Logic Section J interunit locking

(2380 Fig. 10)

YES

(h) Is a static test ramp displayed on the screen? — YES — 2380 Logic Section C

(2380 Fig. 3)

NO

(i) Press SWEEP MODE SINGLE ARM

Did the green key lamp go ON? — NO — No response from keyboard

(Fig. 5(a))

YES

Did the yellow key lamp go ON and then, after the sweep time, go OFF? — NO — Did yellow lamp go ON? — NO — Failing to set synthesizer

(Fig. 5(b))

YES

YES

No sweep

(Fig. 5(c))

Press the PRESET key

Is the display annotation showing 400 MHz/div., 0 dBm against the top line, -100 dBm against the bottom line? — NO — 2382 Logic Section - failure to PRESET

(Fig. 6)

YES

(j) Is there a normal noise waveform displayed at any level on the screen? — NO — 2380 Logic Section K

(2380 Fig. 11)

YES

Press the TRACK GEN key

Fig. 2(iv)

Fig. 2(iii) Fault location chart - top level, overall system

Fig. 2(iii)

(k) Does display show a level of -10 dBm from 10 MHz to 400 MHz?

NO — Is the TG displayed at some level?

NO — With ZERO SPAN is TRACK GEN output -10 dBm at 200 MHz?

YES — NO

TG fault
(Fig. 8)

YES

YES — YES

Select in turn 0 dB to 60 dB RF ATTEN settings.

Does the signal appear? — NO — Synthesizer fault
(Annex A, Fig. 2)

YES

Does the displayed TG level remain constant

NO — RF/IF gain switching or LOG AMP fault.*
(Fig. 16 or 15)

YES

Save Display A.
Select in turn -10, 0,+10,+20,+30 dBm Ref. Level.

Does the displayed TG level in dBm remain constant at -10 dBm?

YES — NO

2380 Logic Section I AB4 Shift latch and adder.
(2380 Fig. 9)

Disconnect lead to TRACK GEN output. Connect the STD 10 MHz output to the signal INPUT.

Fig. 2(v)

*Use 47.4 MHz (IF) OUTPUT to check the RF attenuator.

Fig. 2(iv) Fault location chart - top level, overall system

Fig. 2(iv)

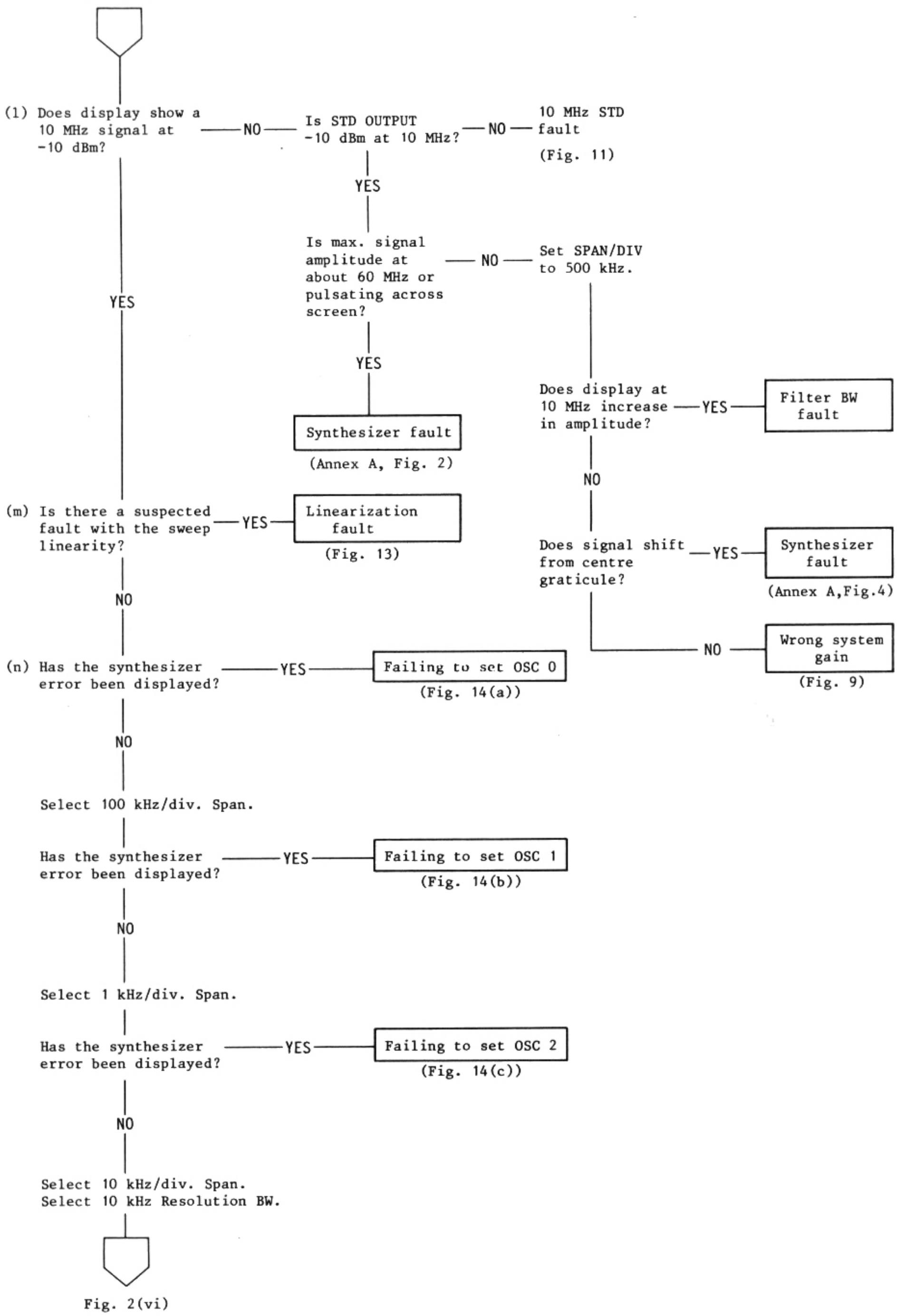


Fig. 2(vi)

Fig. 2(v) Fault location chart - top level, overall system

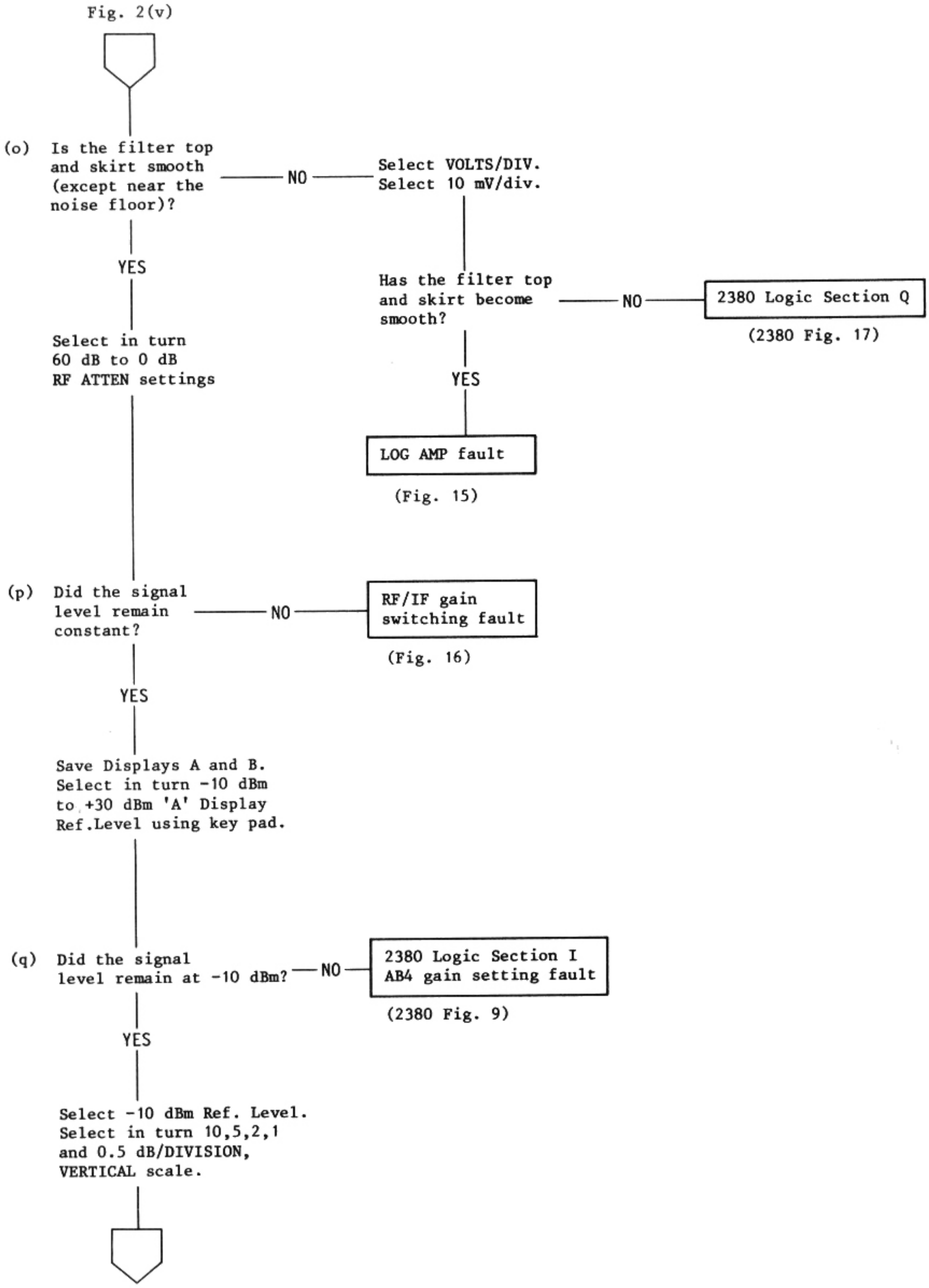


Fig. 2(vi) Fault location chart - top level, overall system

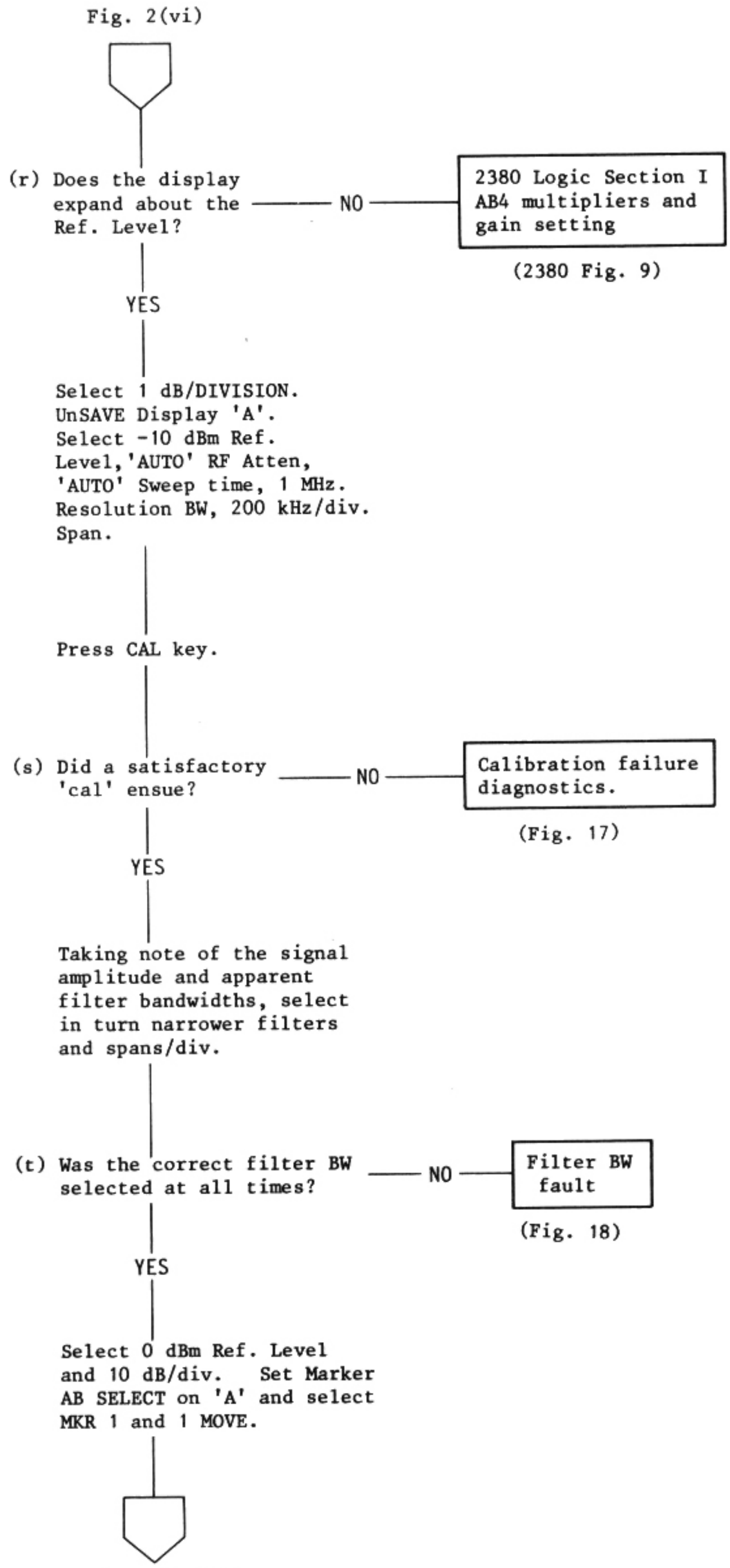


Fig. 2(vii) Fault location chart - top level, overall system

Fig. 2(vii)

(u) Can marker be moved correctly using the MARKERS MOVE control?

NO → Is the marker visible?

NO → 2380 Logic Section N Marker generation

(2380 Fig. 14)

YES → 2382 Marker control diagnostics

(Fig. 19)

Is the marker visible? YES

Press PRESET. Select 1 MHz/div., 3 kHz Resolution BW, 10 MHz. Ref. Freq. Note appearance of noise on display.

Select 'B' VIDEO AVG '1'. Note appearance of noise.

(v) Did the appearance of the noise change from a band of about 1 cm deep to an irregular open noise waveform? (Level of signal may change.)

NO → 2380 Logic Section L Detector max/min latch

(2380 Fig. 12)

YES

Press 'B' VIDEO AVG key. Select 10 s/div. Sweep Time. Decrease Video BW in steps down to 22 Hz.

(w) Did the depth of the noise band decrease in steps, as each lower Video BW was selected, to a depth less than 5 mm?

NO → 2380 Logic Section M Video filter

(2380 Fig. 13)

YES

Select 'AUTO' Video BW, 300 kHz Resolution BW MKR 1, and '1' MOVE.

Fig. 2(ix)

Fig. 2(viii) Fault location chart - top level, overall system

Fig. 2(viii)

Move marker using the MARKERS MOVE control so that the indicated marker frequency is 10.5 MHz.

Select FREQ COUNT

(x) Is the indicated marker frequency now 10 MHz? — NO → 2382 Logic Section - Frequency count (Fig. 20)

YES

Deselect AUTO TRIG.

(y) Does the sweep stop? — NO → Auto Trig diagnostics (Fig. 21)

YES

Select TRIGGER SOURCE 'LINE'

(z) Does the sweep start to run again? — NO → Line Trig diagnostics (Fig. 22)

YES

Select TRIGGER SOURCE 'EXT'. Apply a 1 V p-p signal between 50 Hz and 100 kHz to the rear panel EXT TRIG socket.

(aa) Is the sweep triggered by this signal? — NO → Ext. Trig diagnostics (Fig. 23)

YES

Fig. 2(x)

Fig. 2(ix) Fault location chart - top level, overall system

Fig. 2(ix)

Turn supply OFF. Remove 2380 top cover. Put AB7 on an extender. Turn supply ON. Press PRESET key.

If a counter is available check freq. of clock on PLAE. If a counter is not available, select 1 MHz/div. and 25 MHz Ref. Freq. Use a low loss probe to display the signal on PLAE. Progressively centring the displayed signal, decrease span to 1 kHz/div.

(ab) Is the frequency 25 MHz ±1 kHz? — NO — 2380 Logic Section J Faulty interunit locking

(2380 Fig. 10)

Using a suitable AM signal generator connect a 25 MHz signal modulated at 1 kHz and 50% depth at a level of -10 dBm to Signal Input. Set Ref. Freq at 25 MHz and view signal at 1 kHz/div.

Select ZERO SPAN and 1 ms/div. Sweep Time.

(ac) Is the 1 kHz modulating signal correctly displayed? — NO — 2382 Zero Span diagnostics - overlaid sampled

(Fig. 24(a))

YES

Set signal modulating frequency to 20 kHz and select 5 us/div. sweep time.

Fig. 2(xi)

Fig. 2(x) Fault location chart - top level, overall system

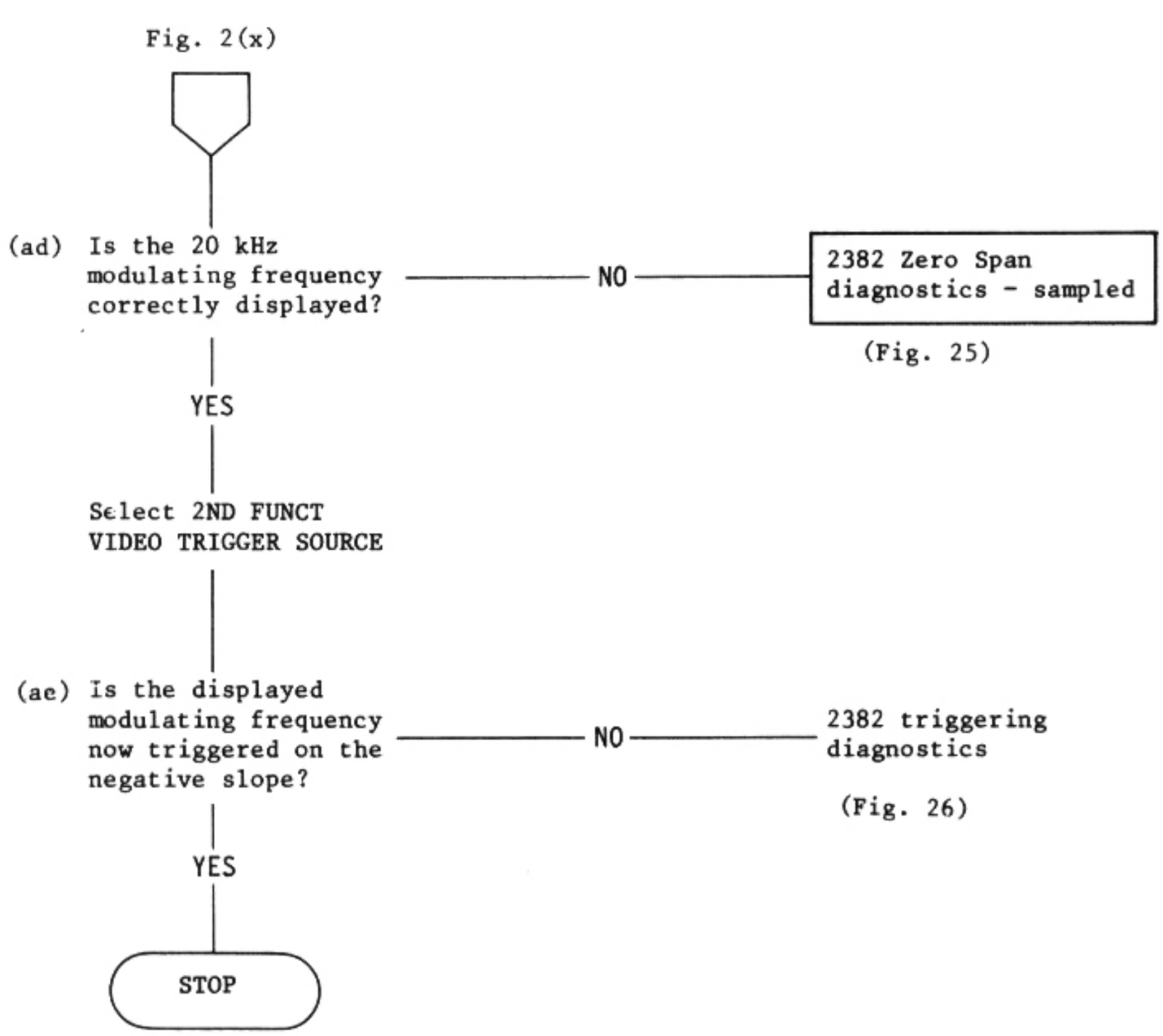


Fig. 2(xi) Fault location chart - top level, overall system

Fig. 2(i)(b)

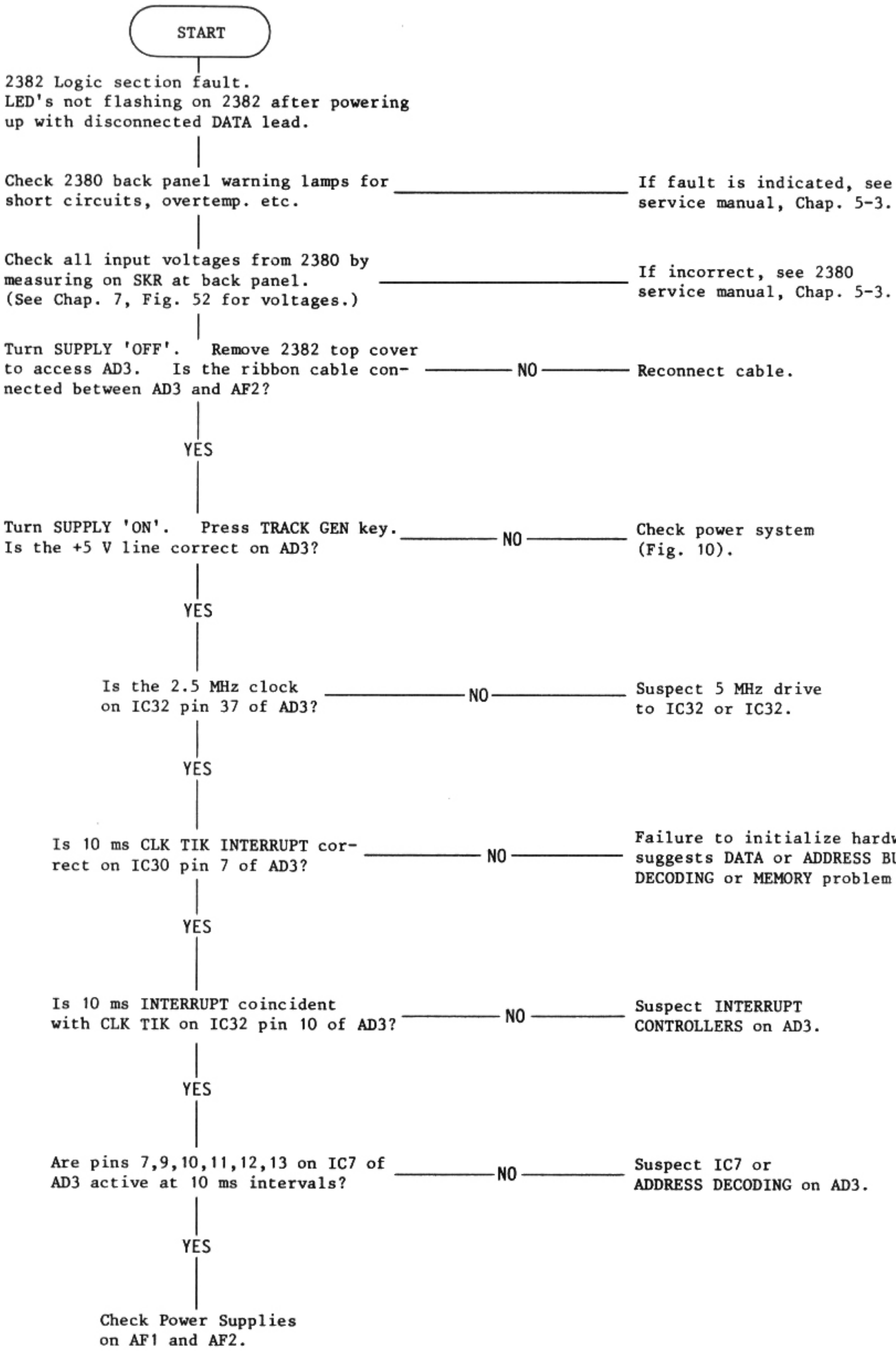


Fig. 3 Fault location chart - Logic section fault

Fig. 2(ii)(f)

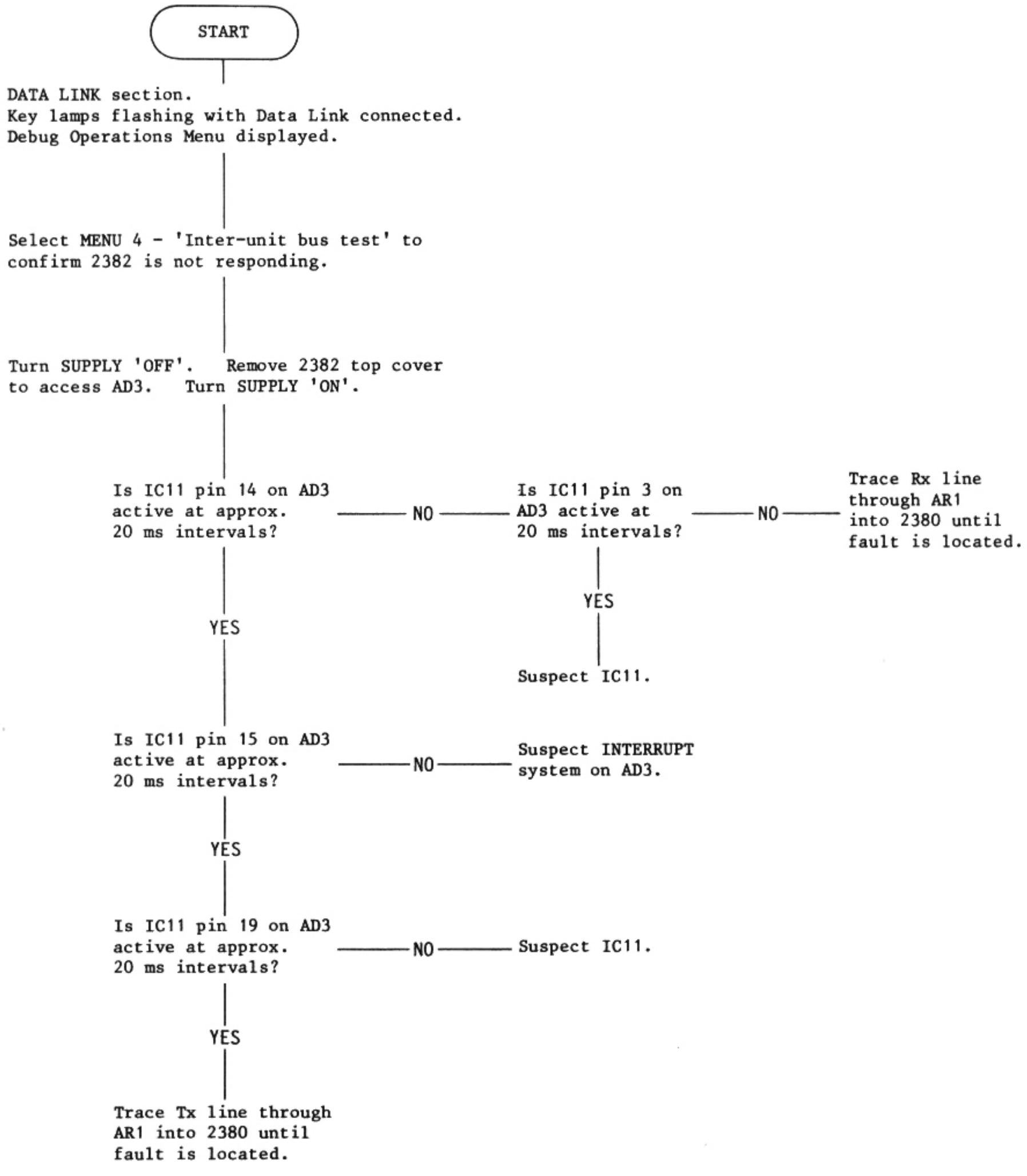


Fig. 4 Fault location chart - DATA LINK section

Fig. 2(iii)(i)

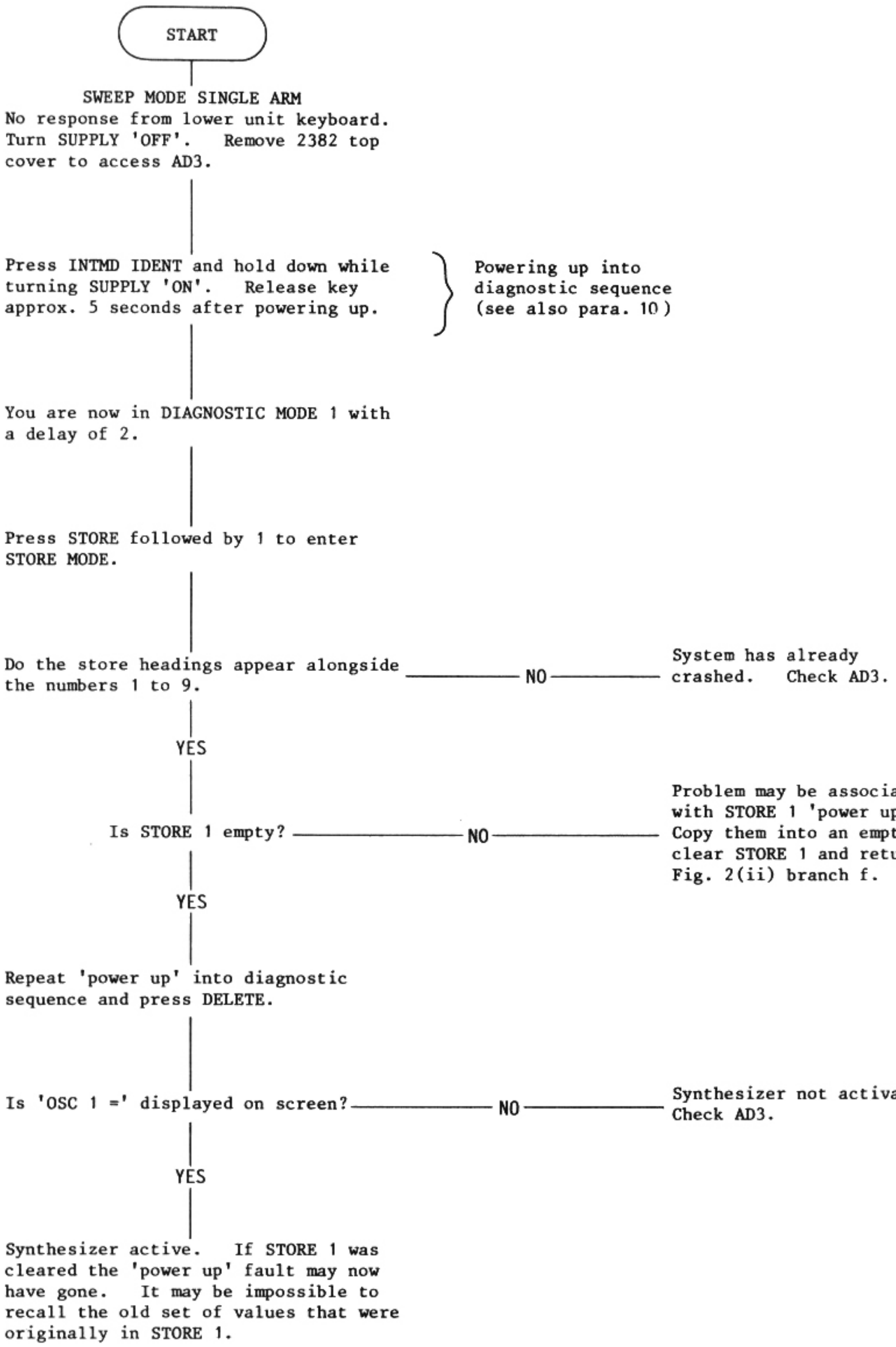


Fig. 5(a) Fault location chart - SWEEP MODE SINGLE ARM

Fig. 2(iii)(i)

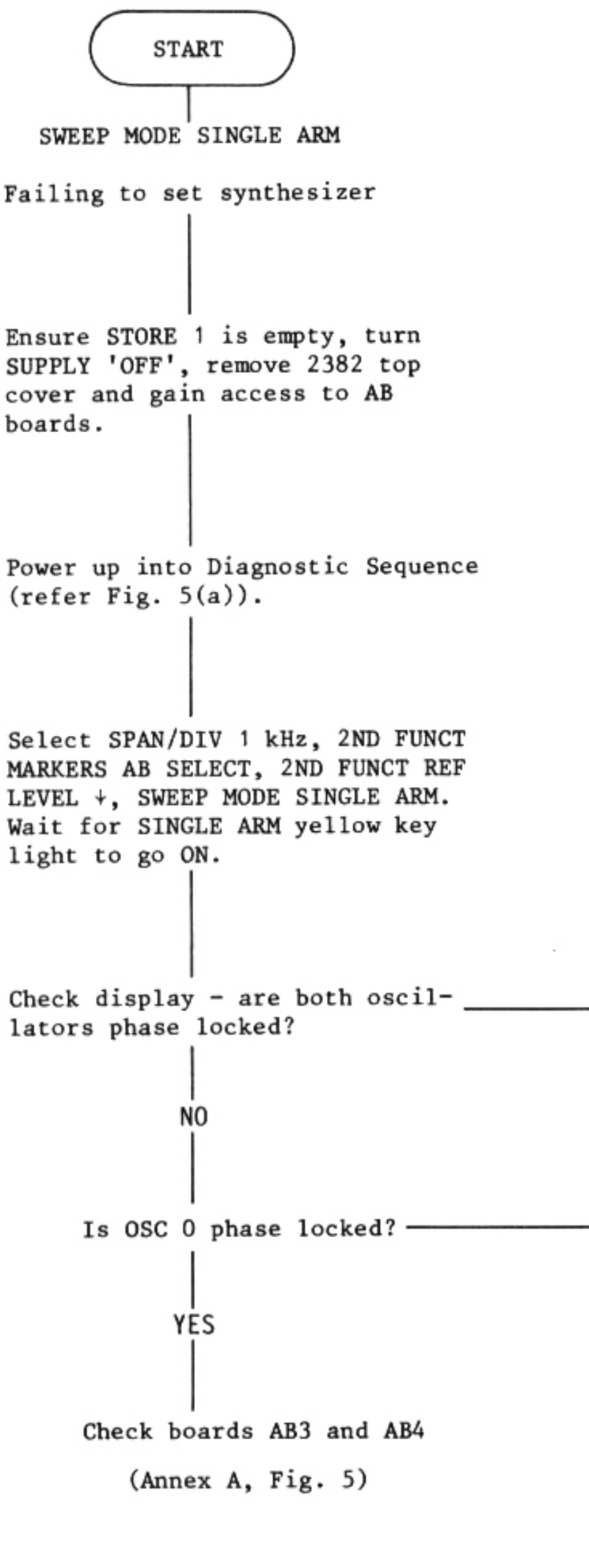


Fig. 5(b) Fault location chart - SWEEP MODE SINGLE ARM

Fig. 2(iii)(i)

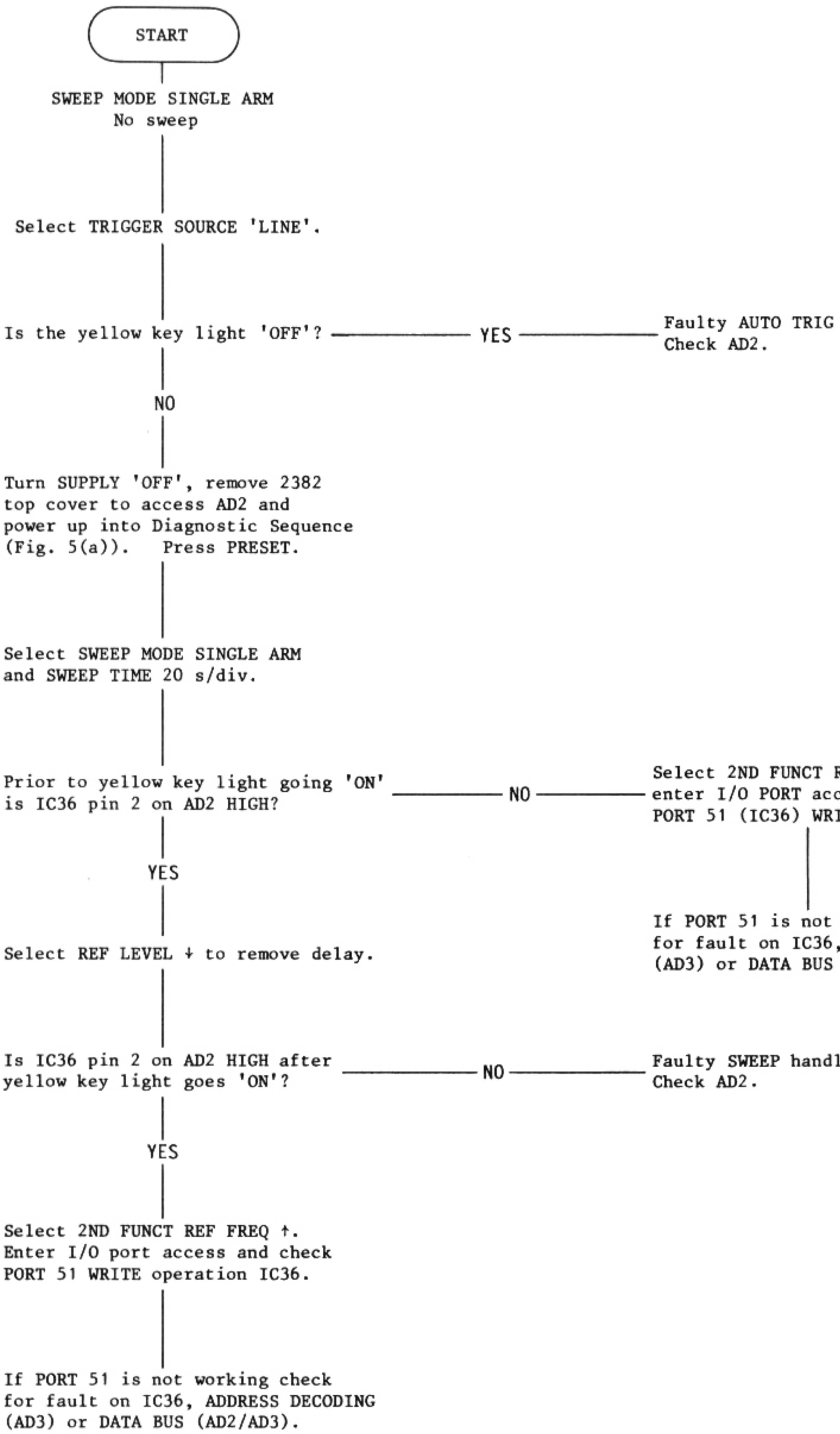


Fig. 5(c) Fault location chart - SWEEP MODE SINGLE ARM

Fig. 2(iii)(i)

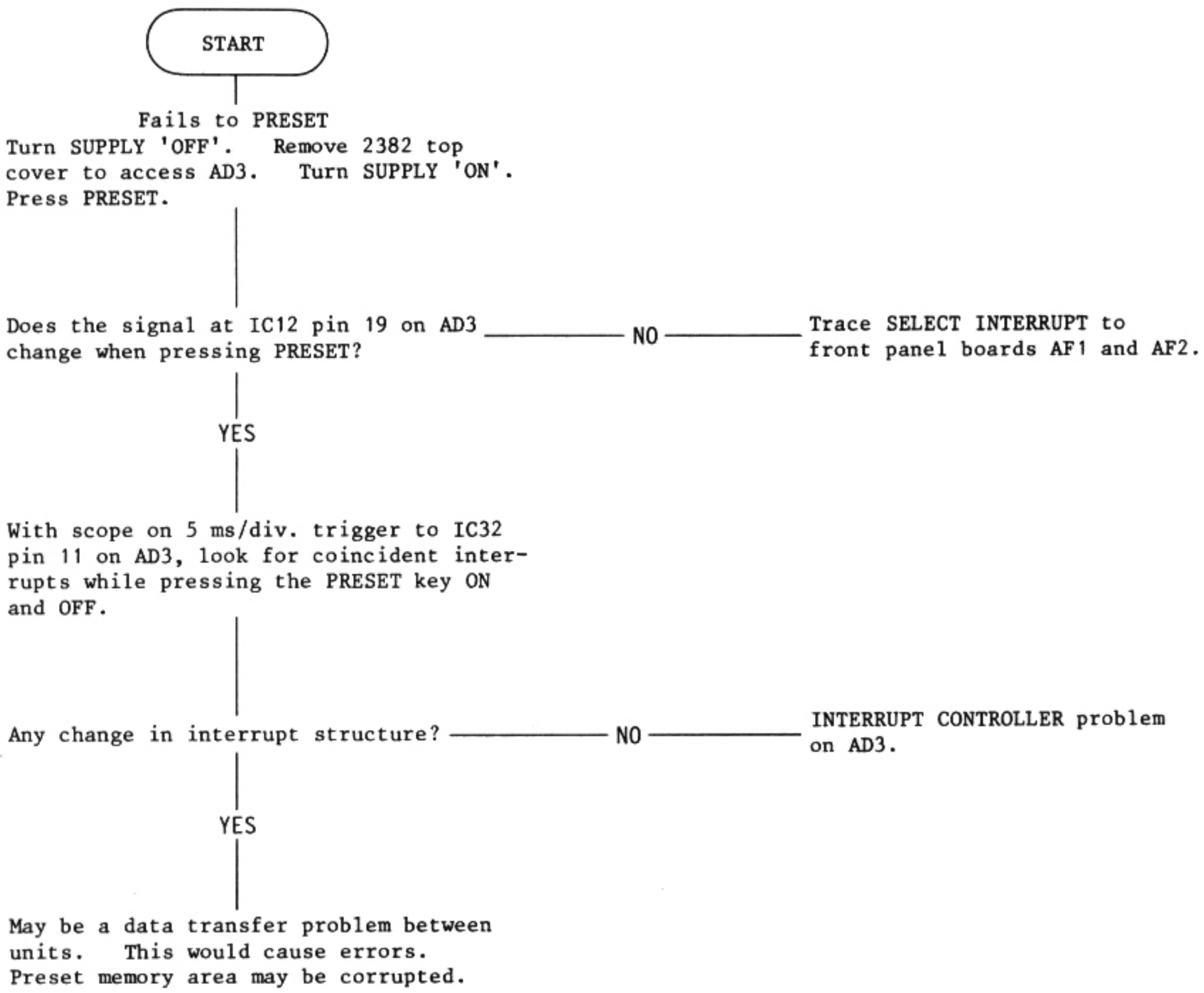


Fig. 6 Fault location chart - Failure to PRESET

Fig. 2(iv)(k)

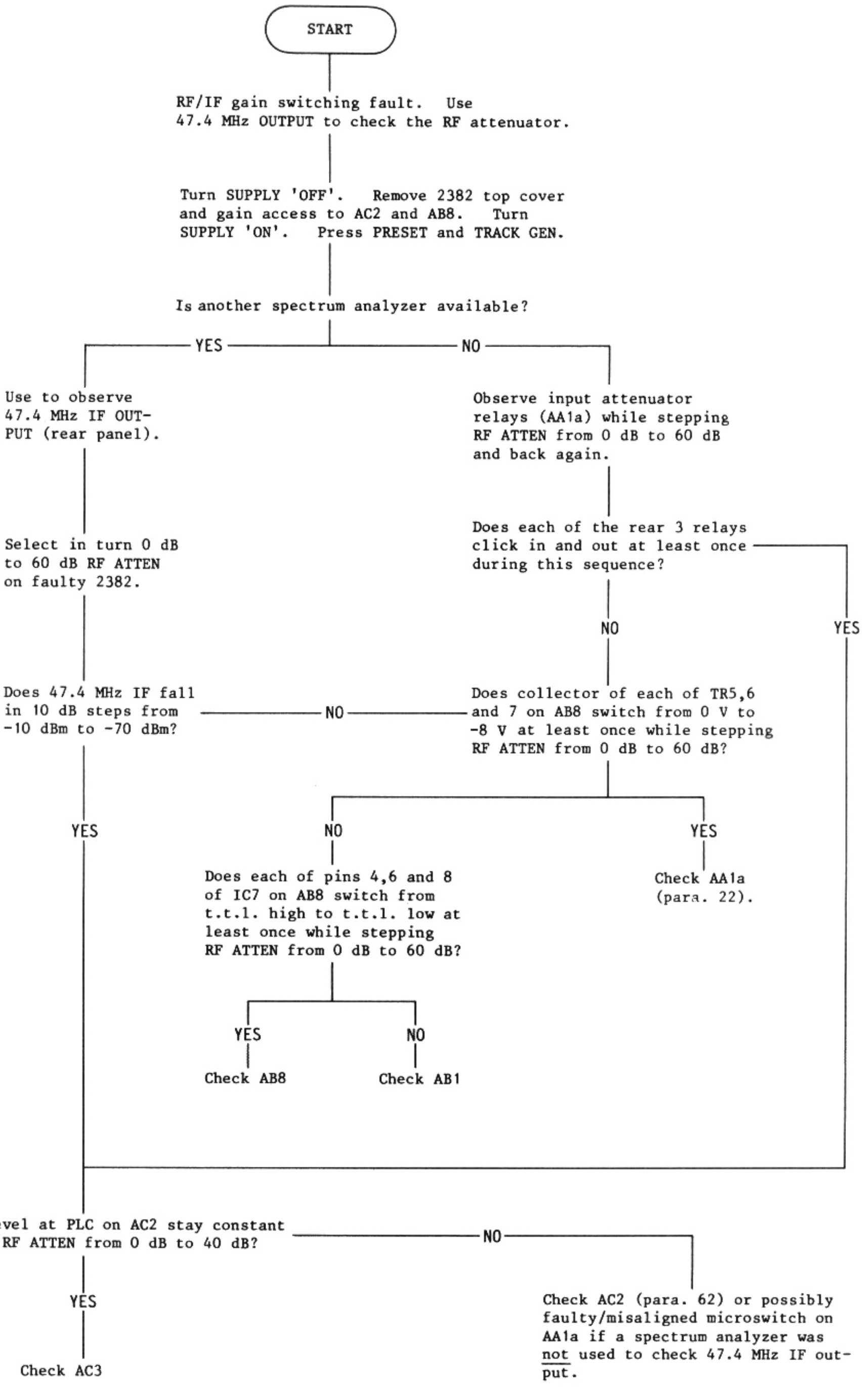


Fig. 7 Fault location chart - RF/IF Gain switching

Fig. 2(iv)(k)

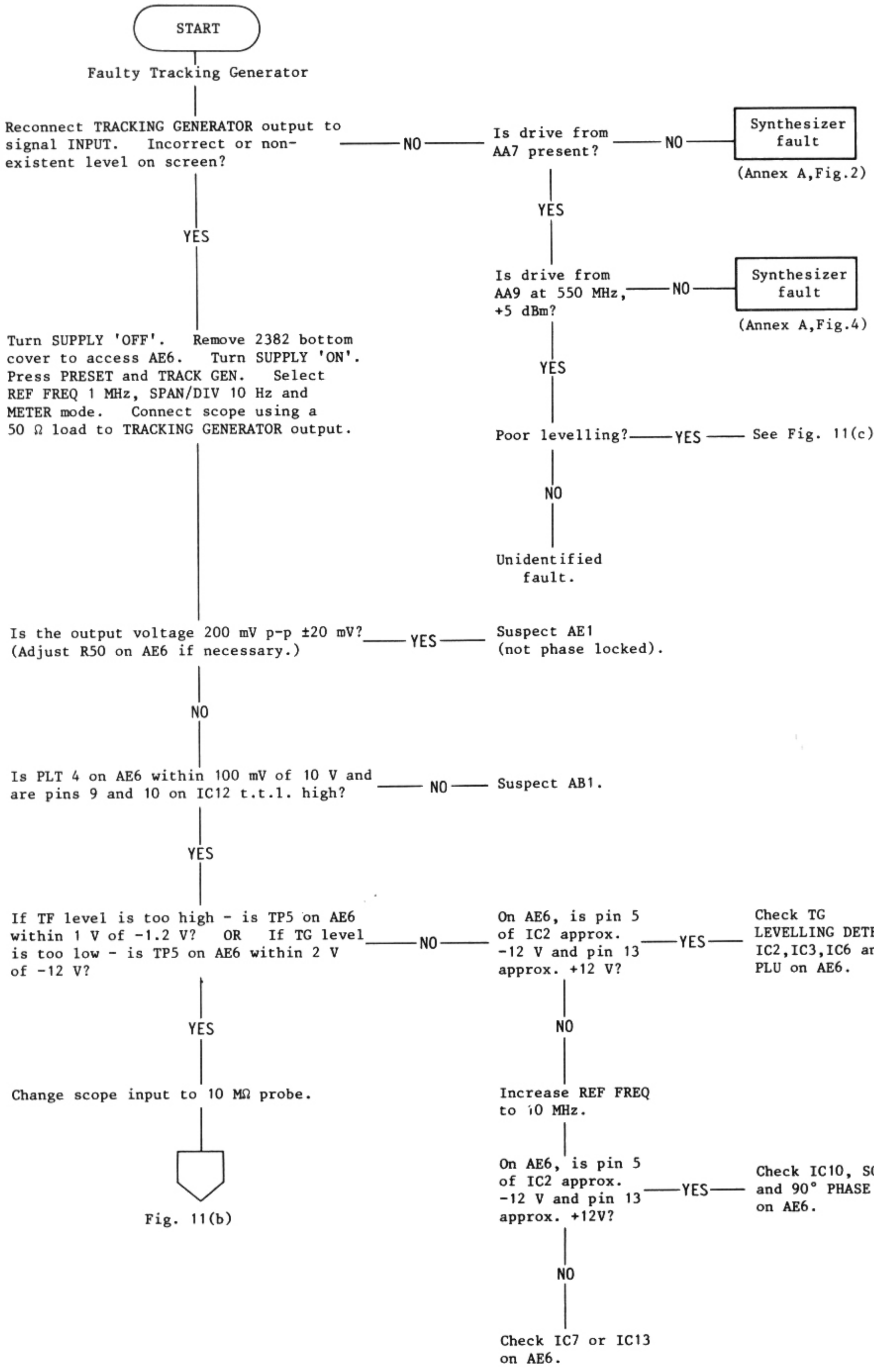


Fig. 11(b)

Fig. 8(a) Fault location chart - Faulty tracking generator

Fig. 11(a)

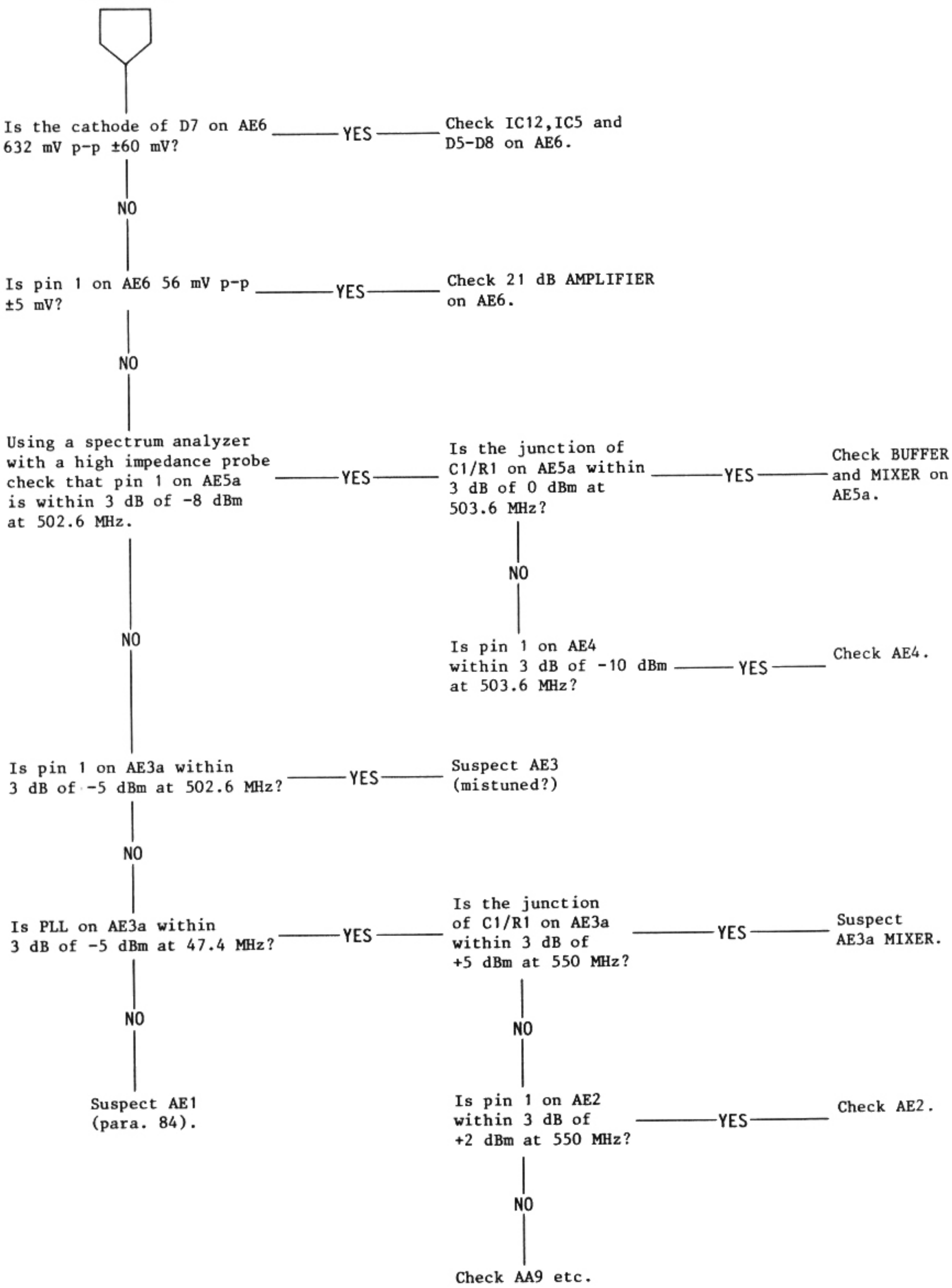


Fig. 8(b) Fault location chart - Faulty tracking generator

Fig. 11(a)

Poor levelling. Select REF FREQ 200 MHz, FULL SPAN and METER mode.

Is the average level within the range -12 dBm to -8 dBm? — NO — Refer back to Fig. 11(a). Incorrect level.

YES

Turn SUPPLY 'OFF'. Remove 2382 bottom cover to access AE1. Turn SUPPLY 'ON'. Press PRESET and TRACK GEN. Select REF FREQ 200 MHz and METER mode.

Attempt to adjust R17 on AE1 to give -4 V at TP5 on AE6. Voltage correct? — NO — Refer back to Fig. 11(a). Incorrect level.

YES

Select /DIV to start analyzer sweeping. Fault still present? — NO — Fault was in Levelling loop - R17 incorrectly set.

YES

Increase SWEEP TIME to 5 s/div. Fault still present? — NO — Suspect TR10 on AE6.

YES

Select AUTO SEEEP TIME. Remove SKE on AE1 and connect PLE to -5 V (available on AE4).

Adjust C8 on AE6 and AE5 for flat response. Does lack of flatness exceed 6 dB total? — NO — Unidentified fault.

YES

Suspect 21 dB AMPLIFIER on AE6, AE4 and AE5(a).

Fig. 8(c) Fault location chart - Faulty tracking generator

Fig. 2(iv)(k)

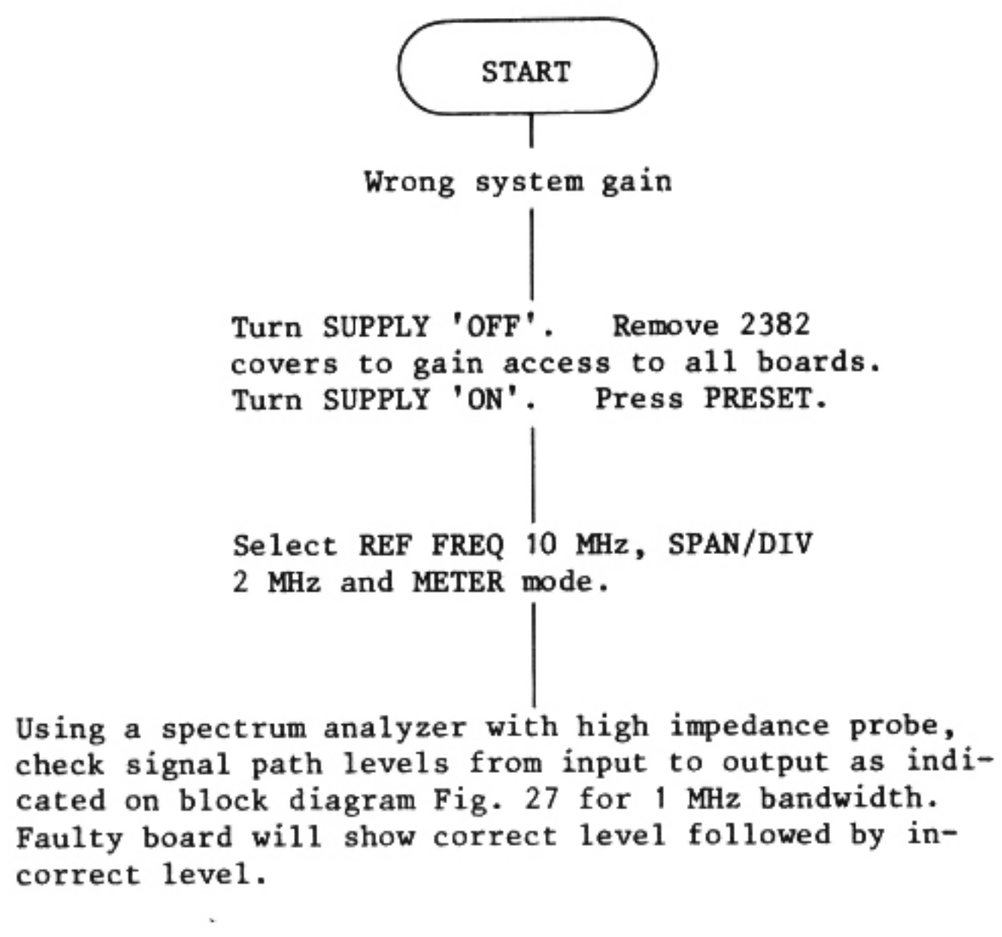


Fig. 9 Fault location chart - Wrong system gain

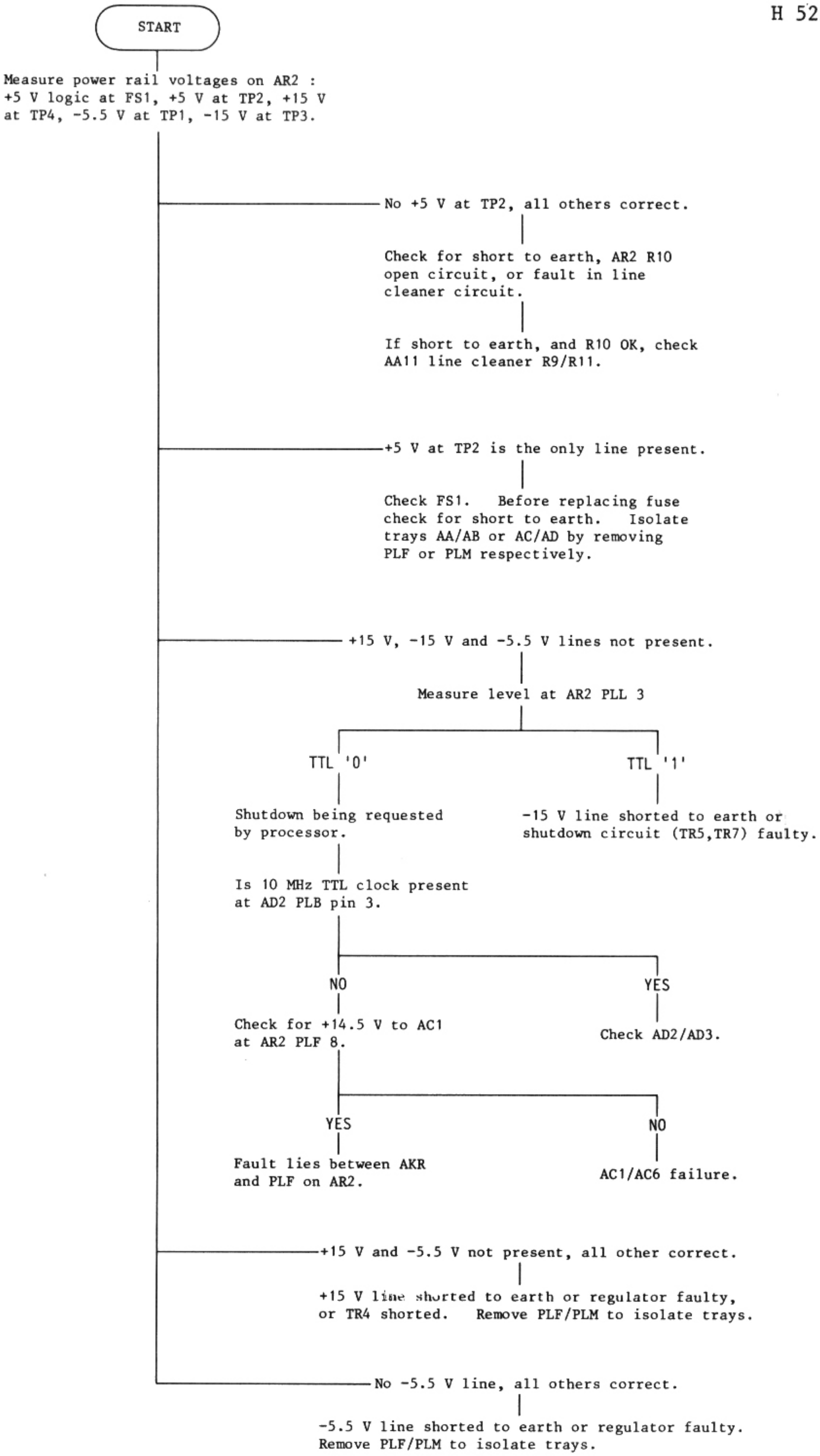


Fig. 10 Fault location chart - Power system

Fig. 2(v) (1)

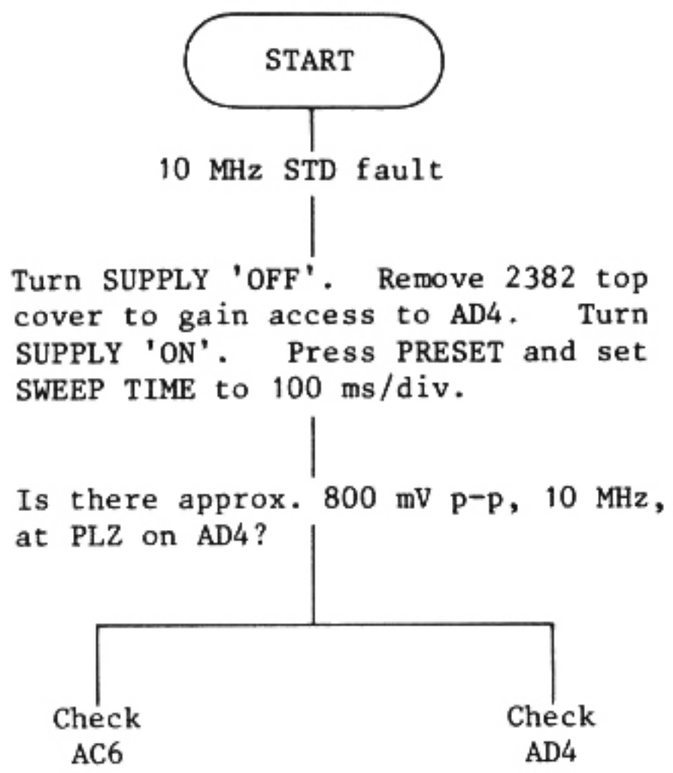


Fig. 11 Fault location chart - 10 MHz STD fault

Fig. 2(v)(1)

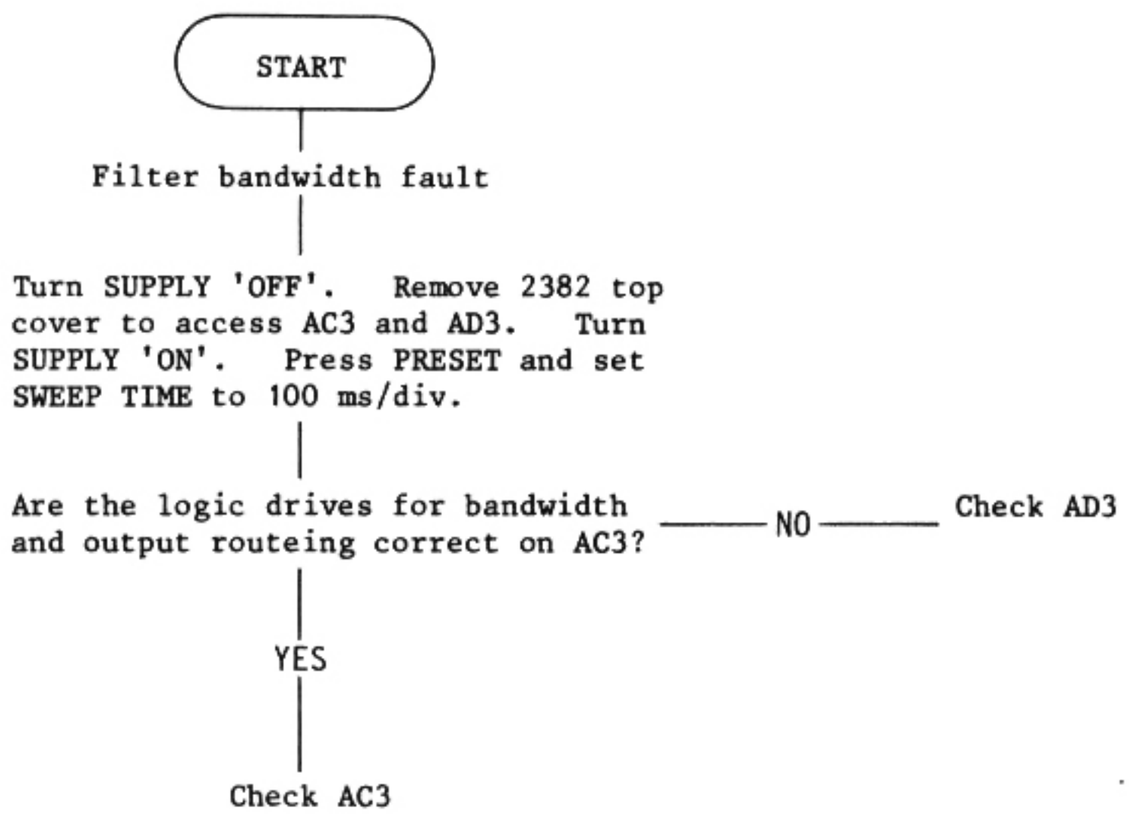


Fig. 12 Fault location chart - Filter bandwidth

Fig. 2(v)(m)

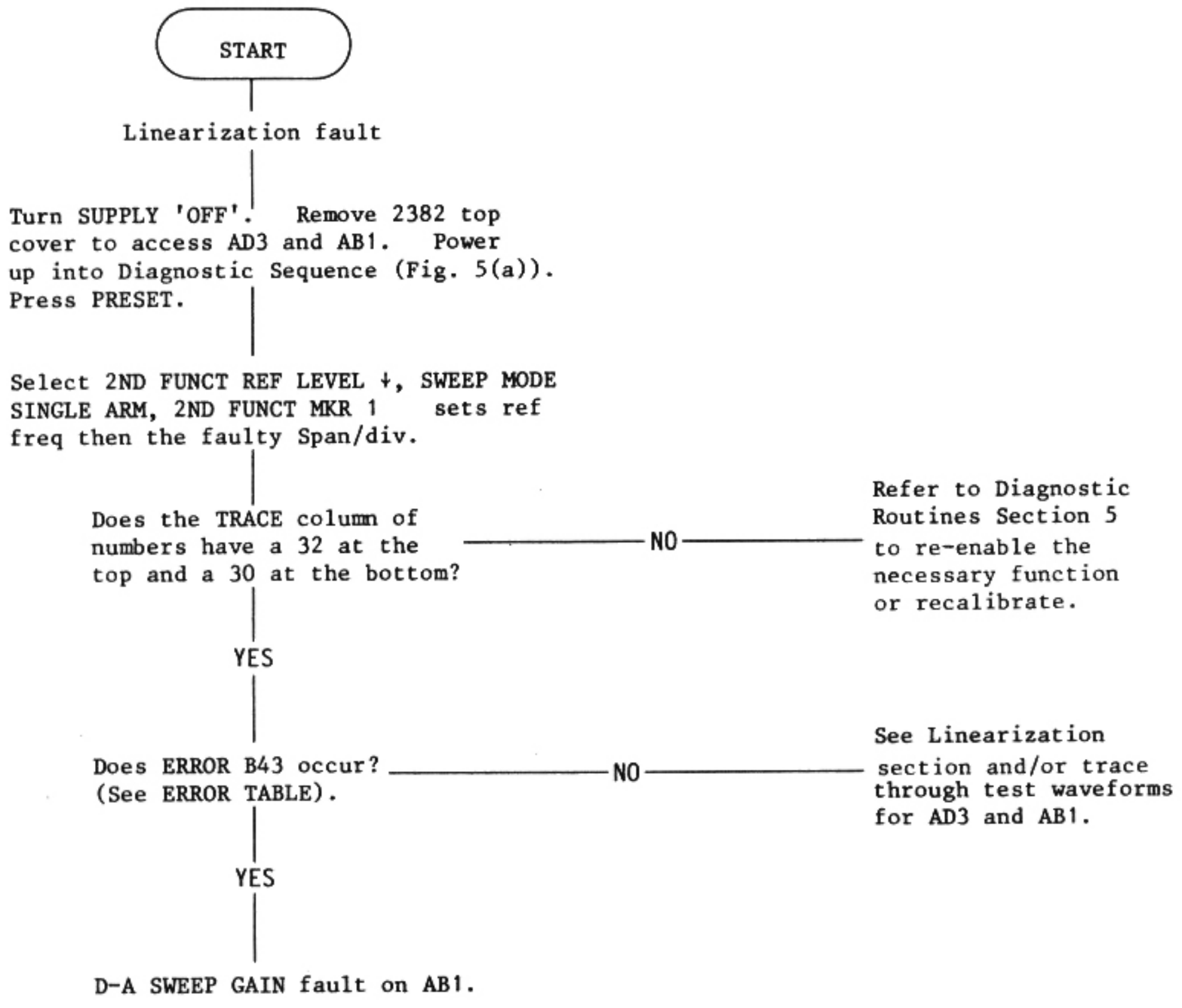


Fig. 13 Fault location chart - Linearization

Fig. 2(v)(n)

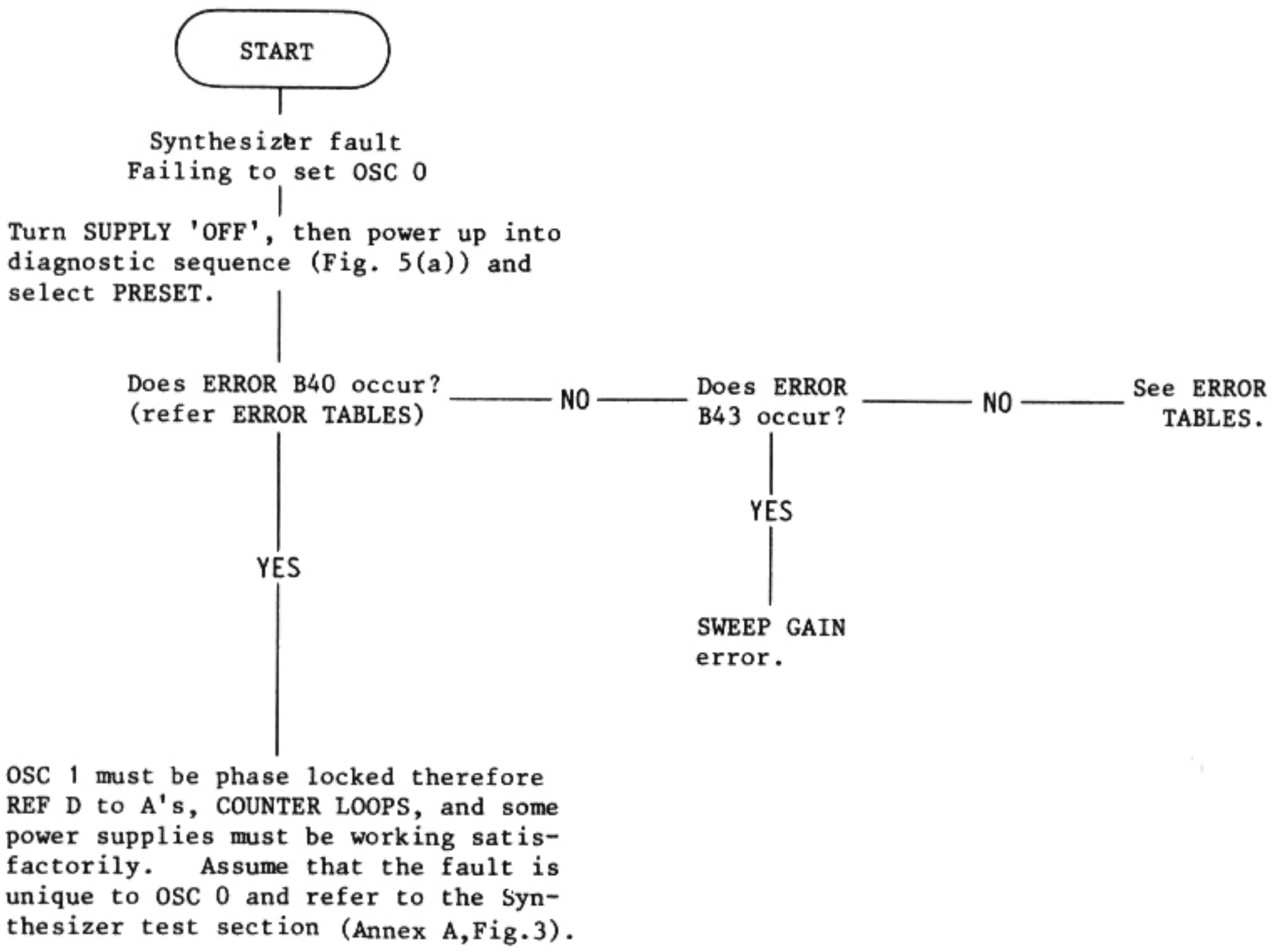


Fig. 14(a) Fault location chart - Synthesizer fault

Fig. 2(v)(n)

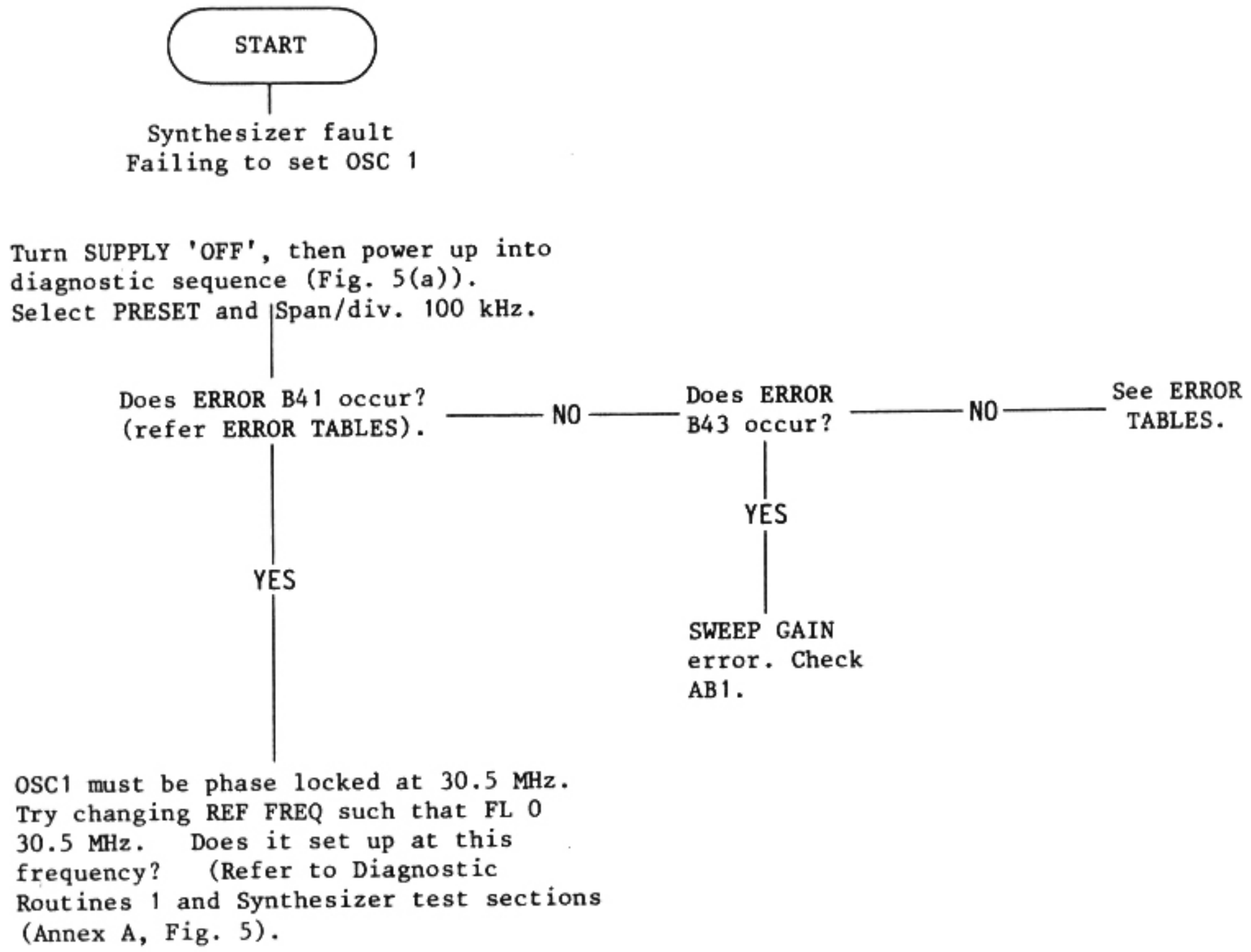


Fig. 14(b) Fault location chart - Synthesizer fault

Fig. 2(v)(n)

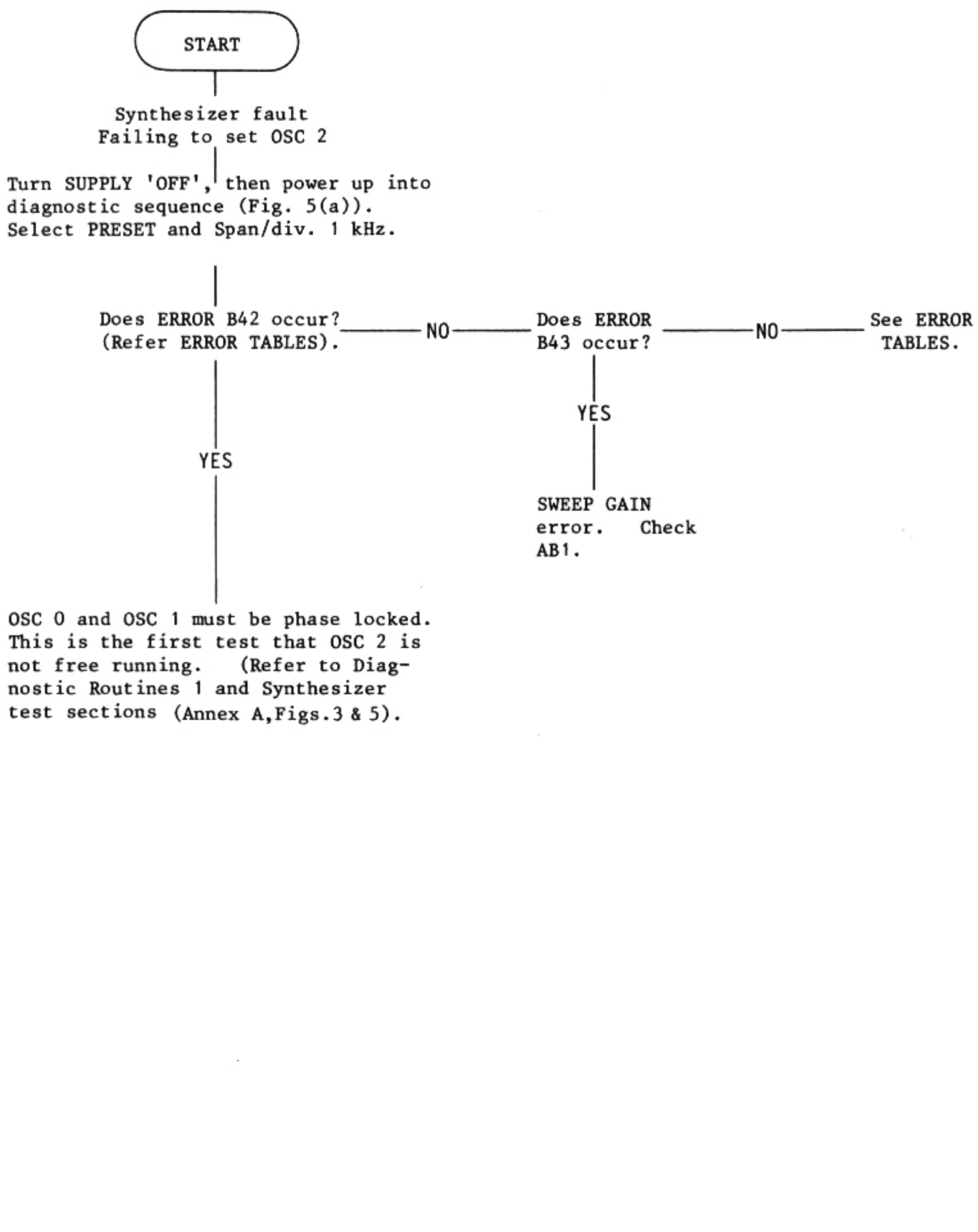


Fig. 14(c) Fault location chart - Synthesizer fault

Fig. 2(vi)(o)

MARKER LEVEL (dBm)	AD1 LOGIC OUTPUTS			
	G1	G2	G3	G4
-16	H	H	H	H
-29	H	H	H	L
-42	L	H	H	H
-68	L	L	H	H
-93	L	L	L	H

Fig. 15 Fault location chart - LOG AMP fault

Fig. 2(vi)(p)

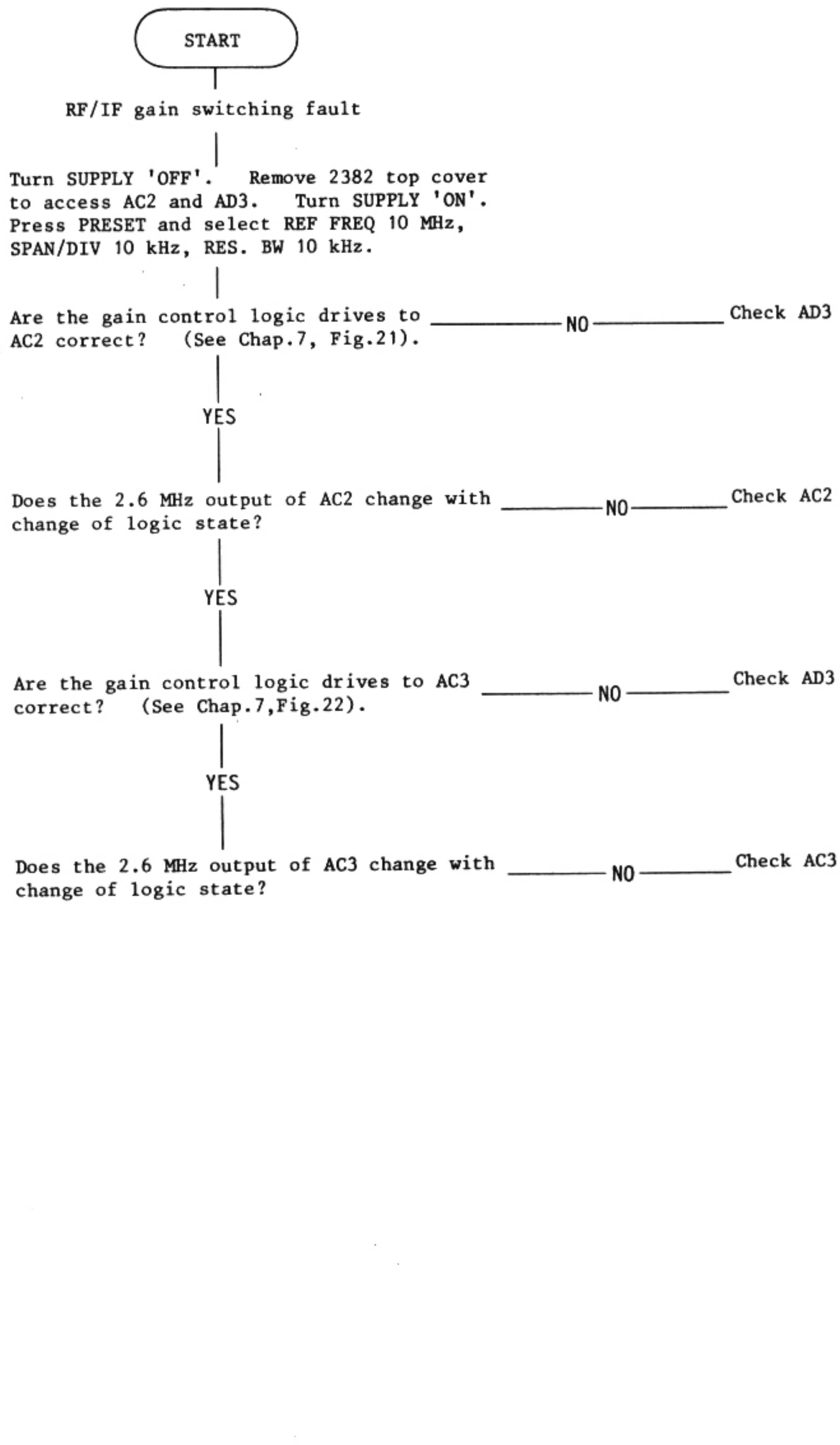


Fig. 16 Fault location chart - RF/IF gain switching fault

Fig. 2(vii)(s)

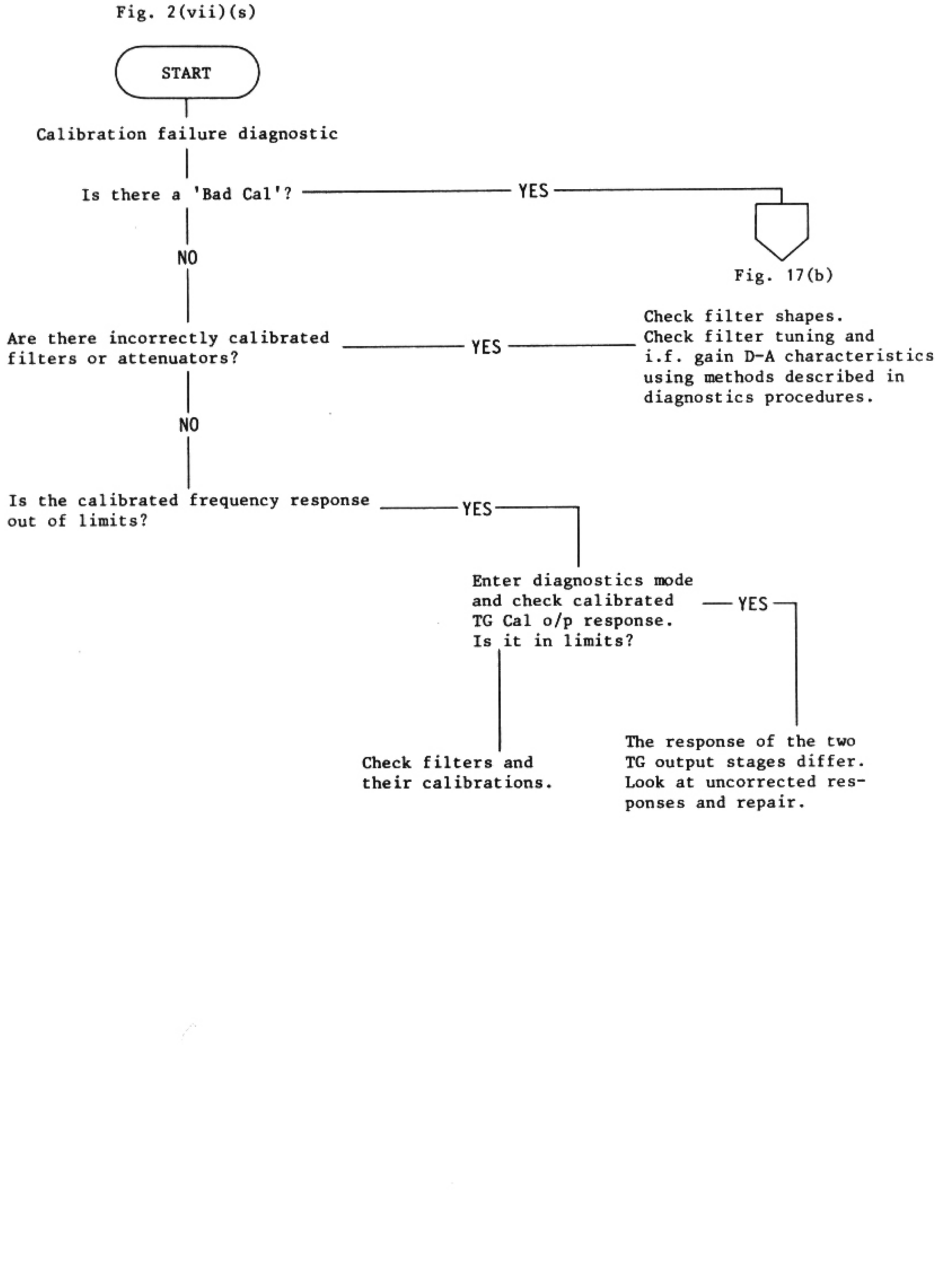


Fig. 17(a) Fault location chart - Calibration fault

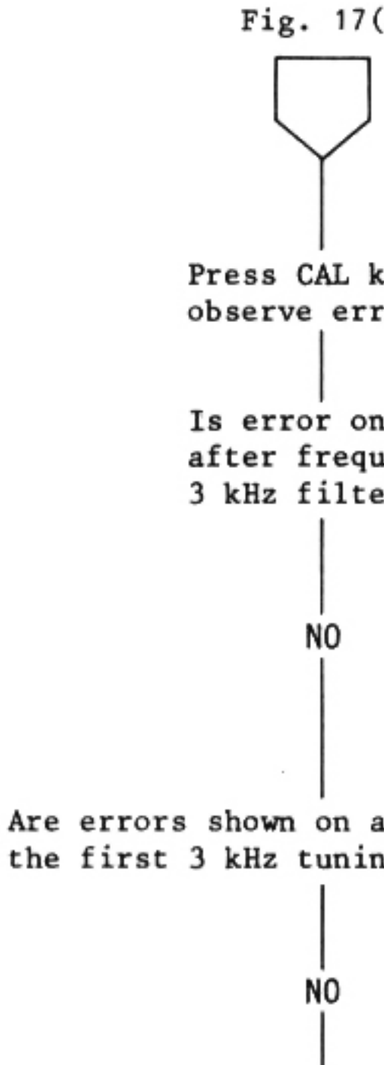


Fig. 17(b) Fault location chart - Calibration fault

Fig. 17(b)

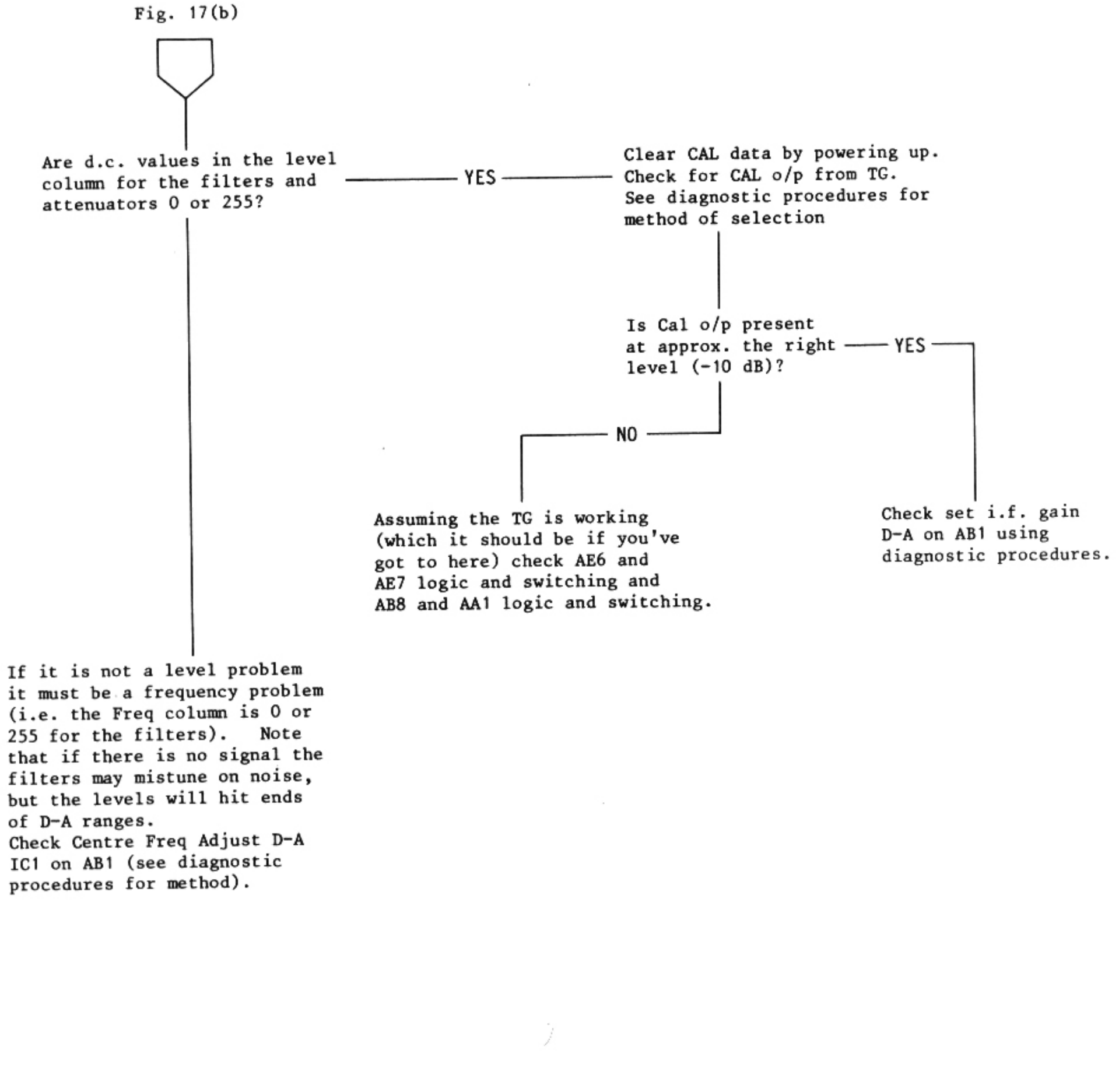


Fig. 17(c) Fault location chart - Calibration fault

Fig. 2(vii)(t)

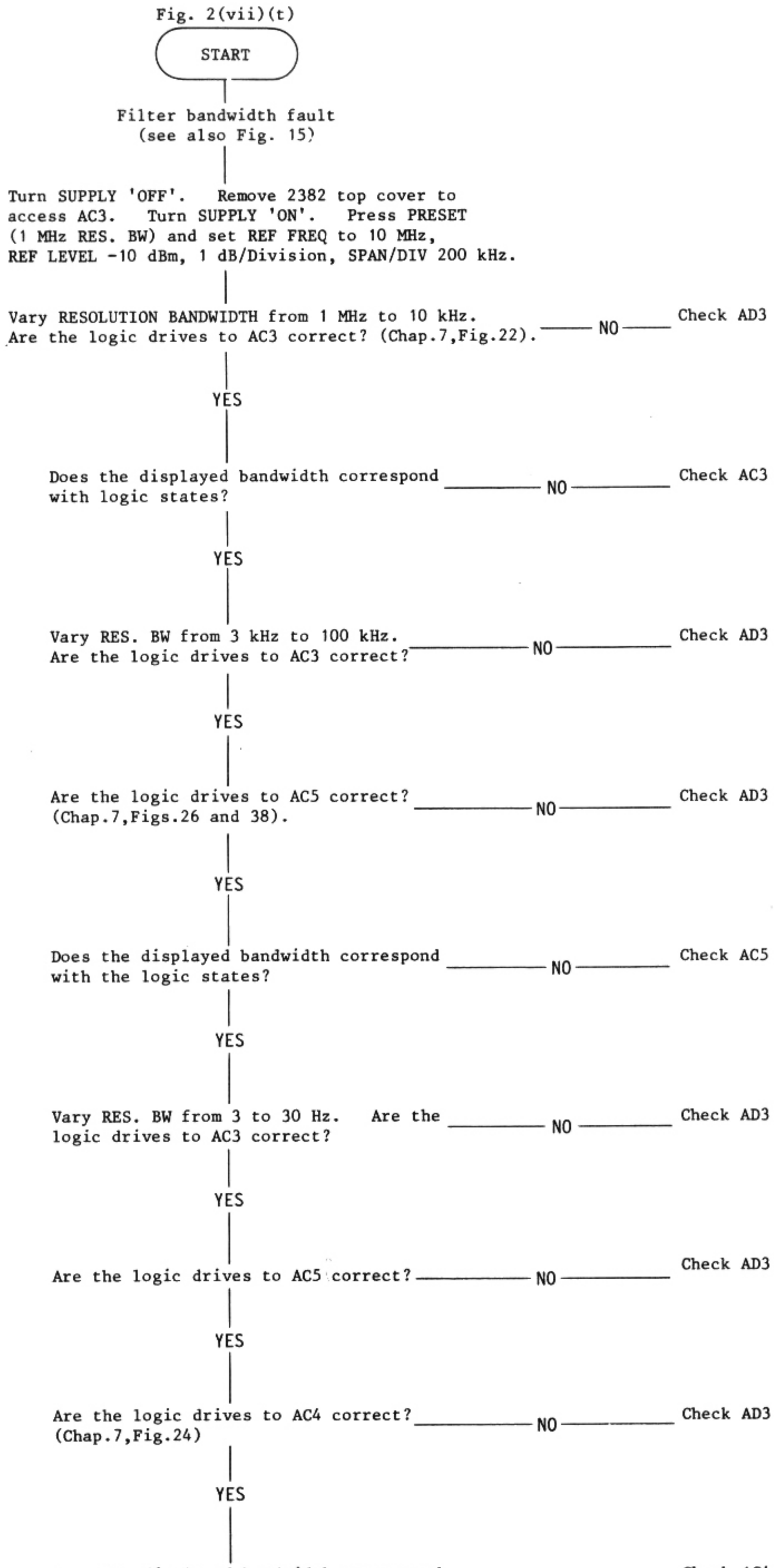


Fig. 18 Fault location chart - Filter bandwidth fault

Fig. 2(viii)(u)

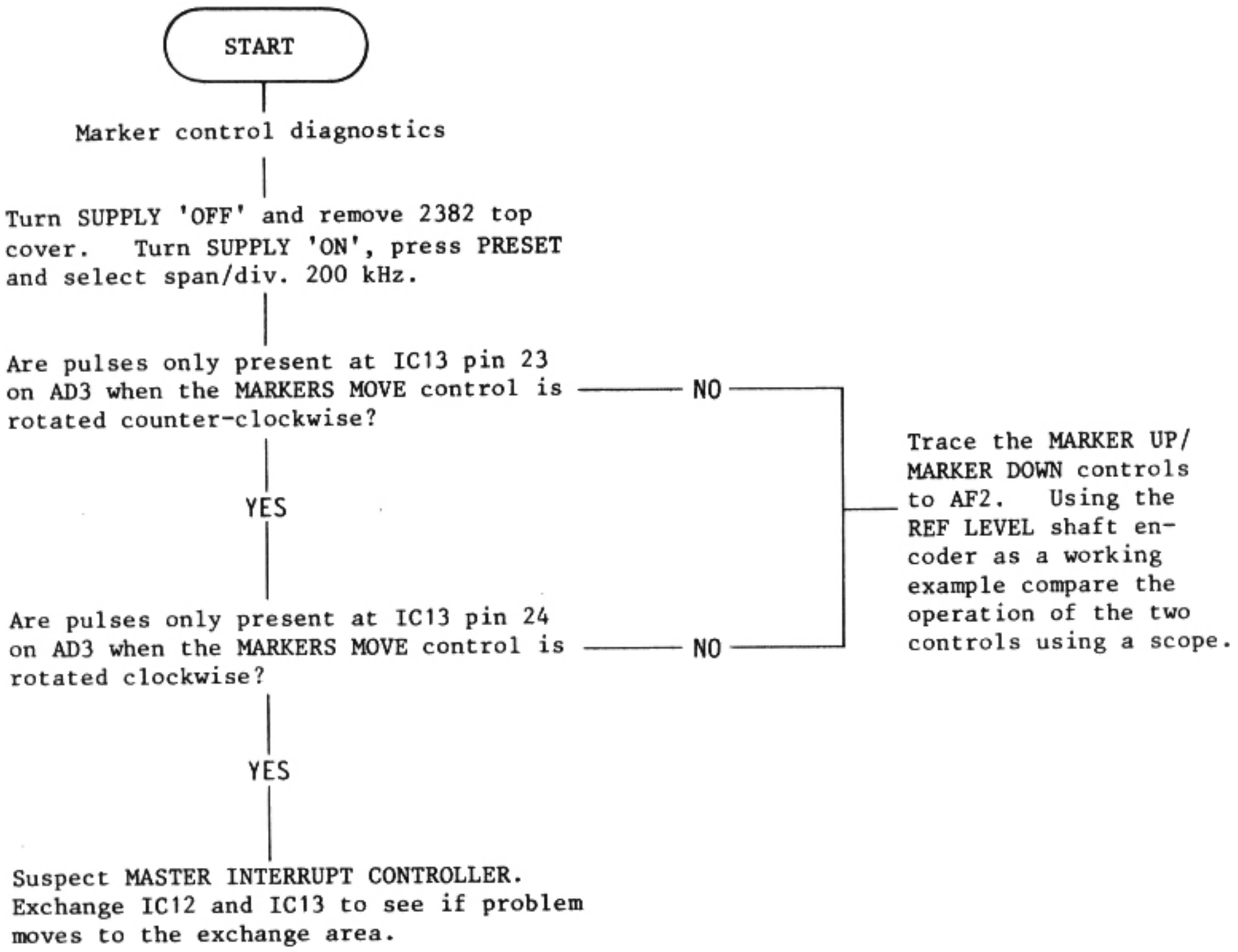


Fig. 19 Fault location chart - Marker controls

Fig. 2(ix)(x)

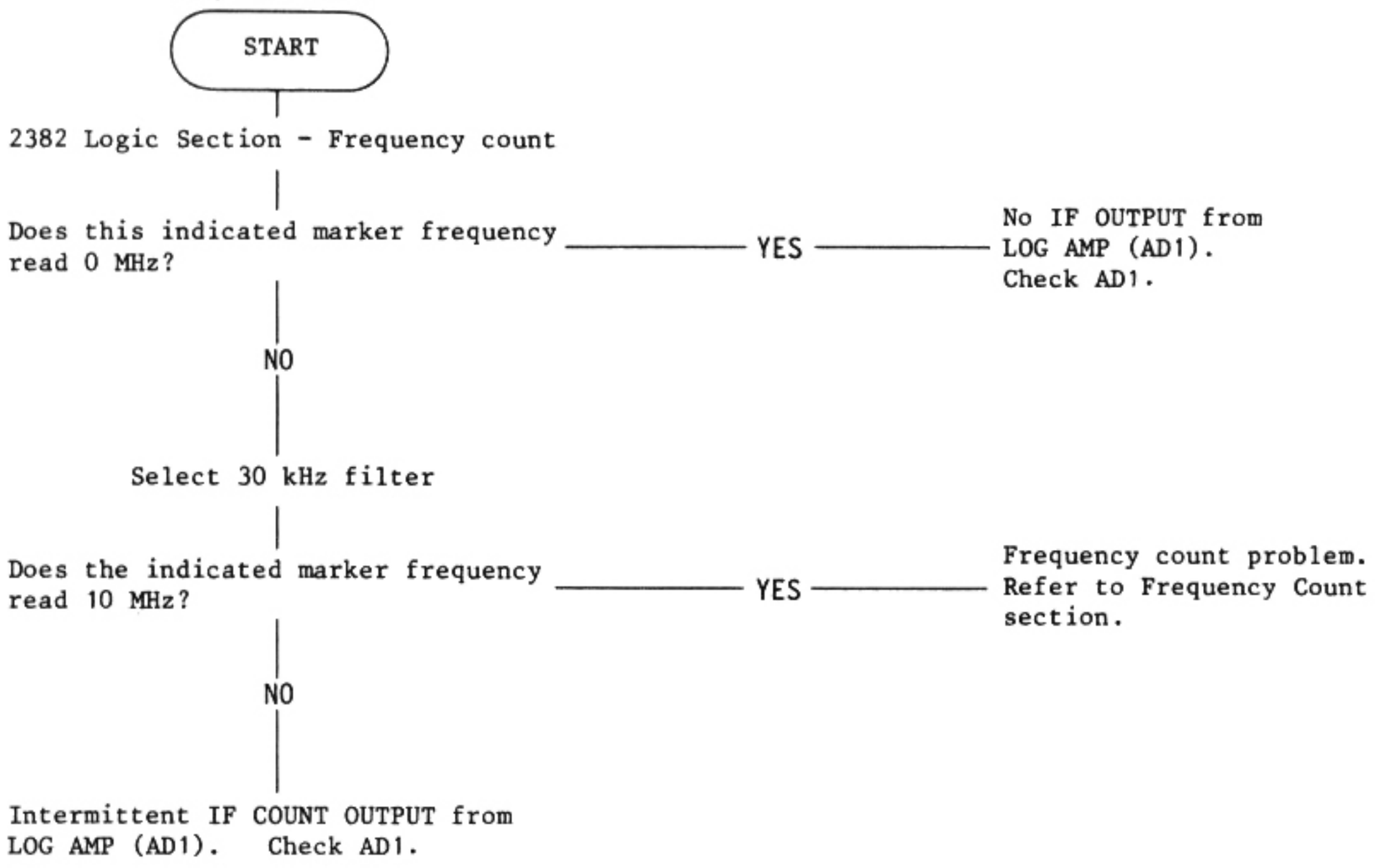


Fig. 20 Fault location chart - 2382 Logic section frequency count

Fig. 2(ix)(y)

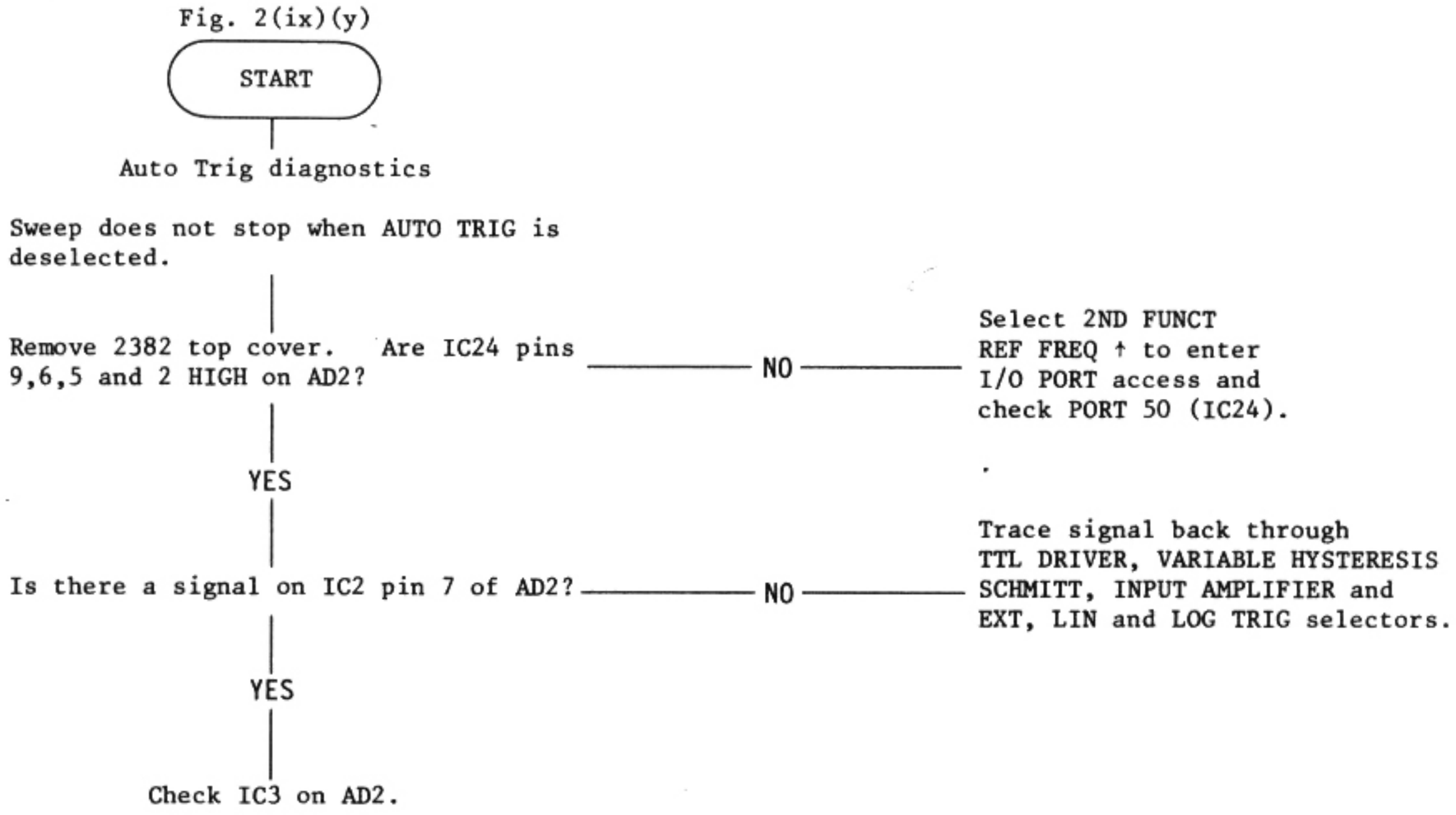


Fig. 21 Fault location chart - Auto Trig diagnostics

Fig. 2(ix)(z)

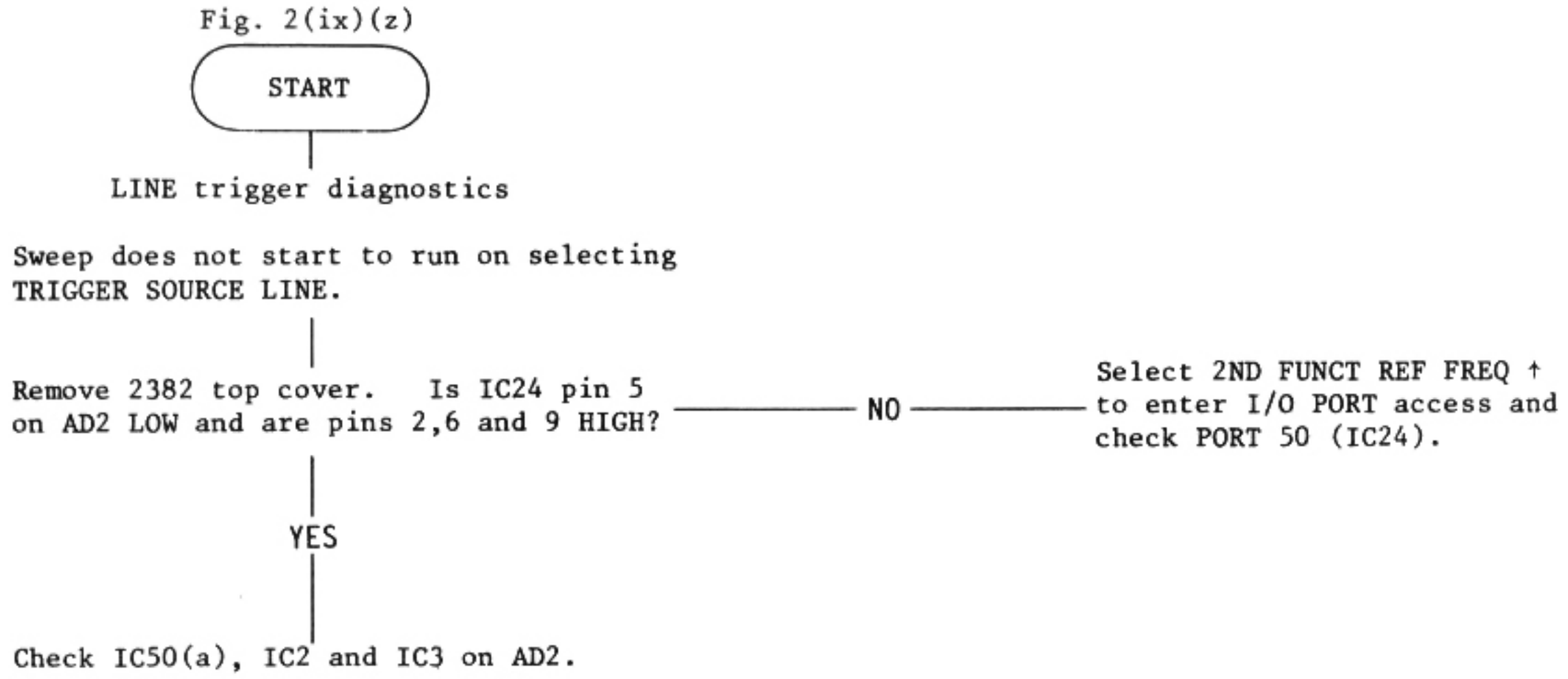


Fig. 22 Fault location chart - Line Trig diagnostics

Fig. 2(ix)(aa)

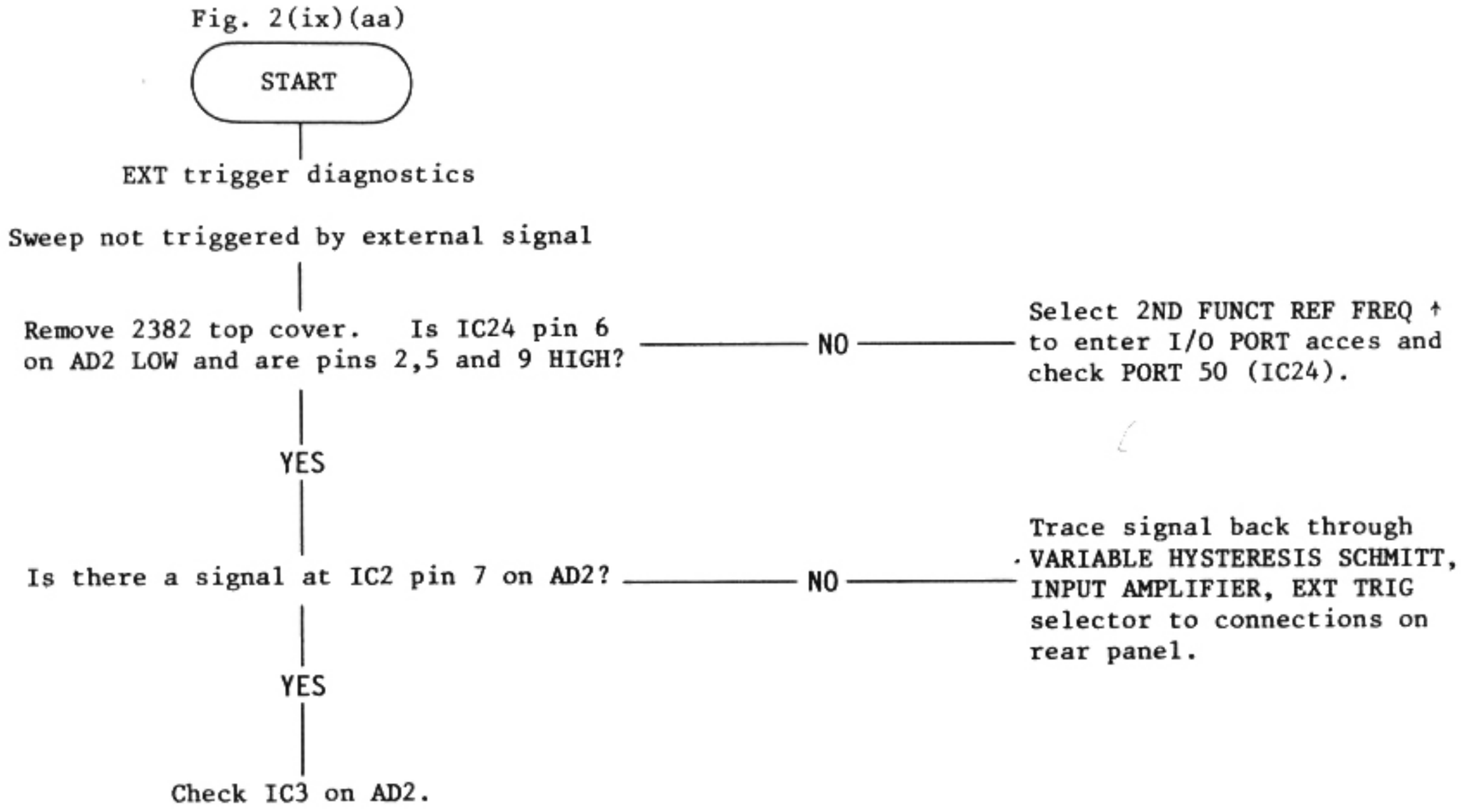


Fig. 23 Fault location chart - Ext Trigger diagnostics

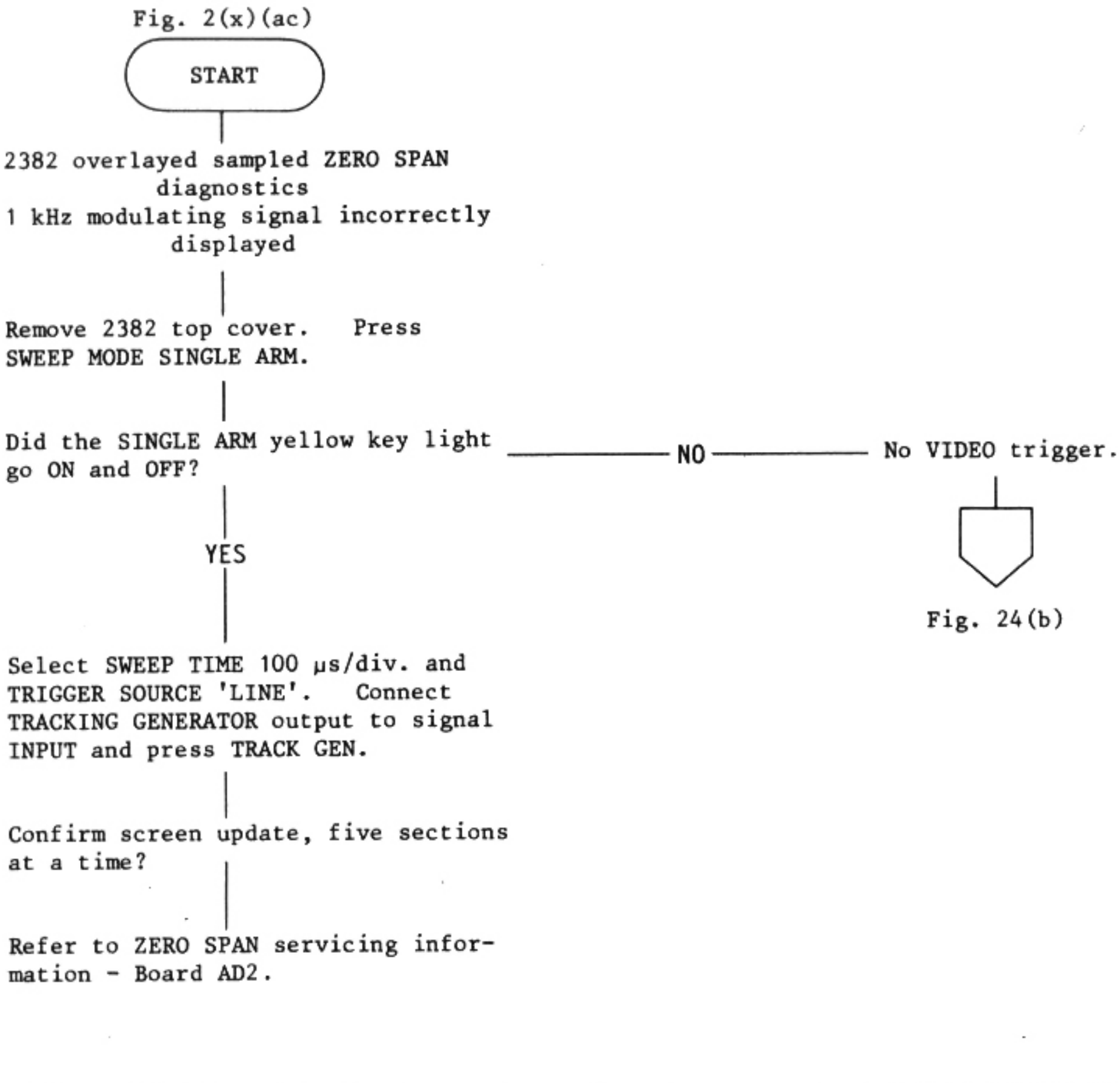


Fig. 24(a) Fault location chart - Sampled ZERO SPAN diagnostics

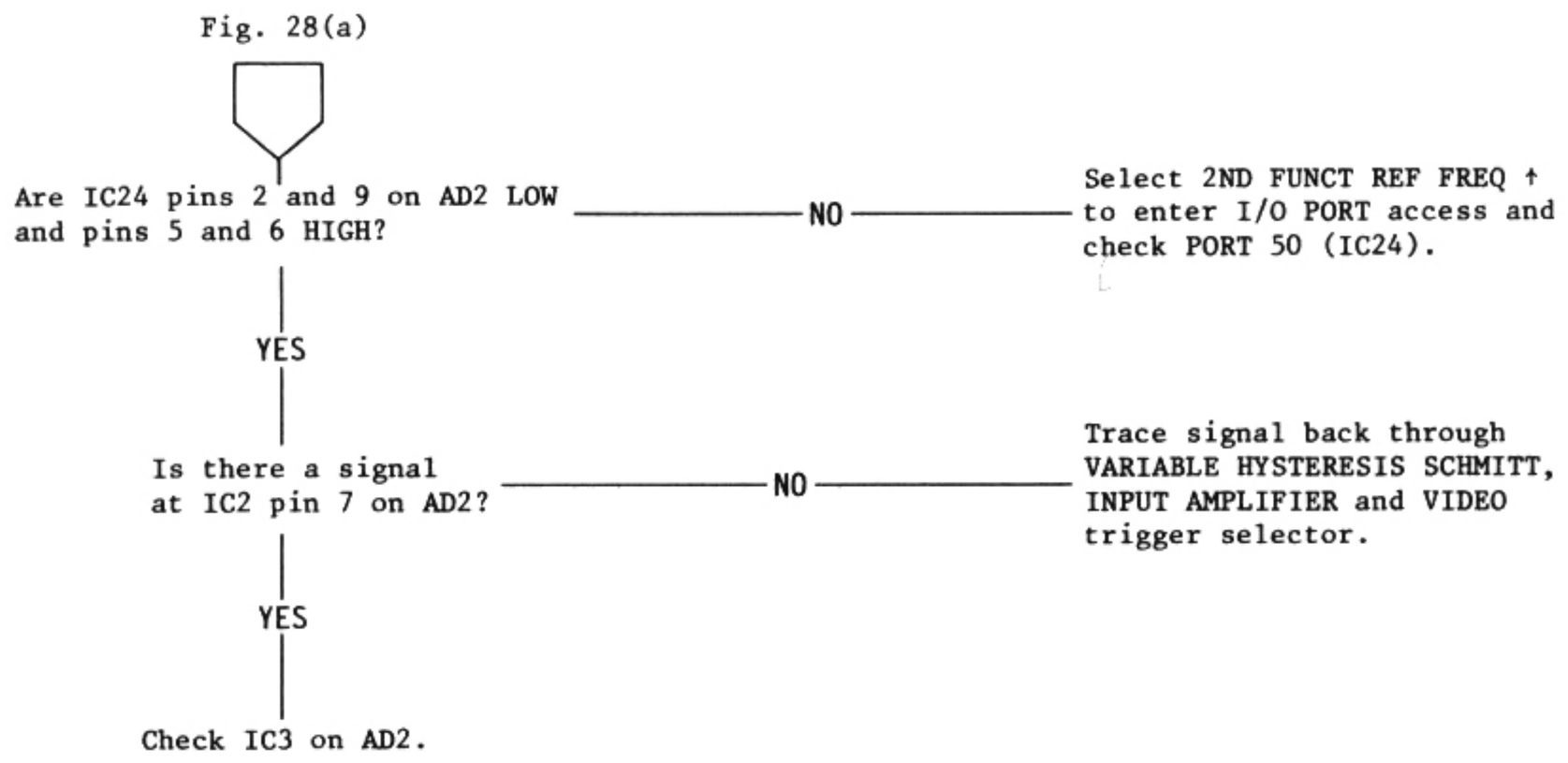


Fig. 24(b) Fault location chart - No VIDEO trigger

Fig. 2(xi)(ad)

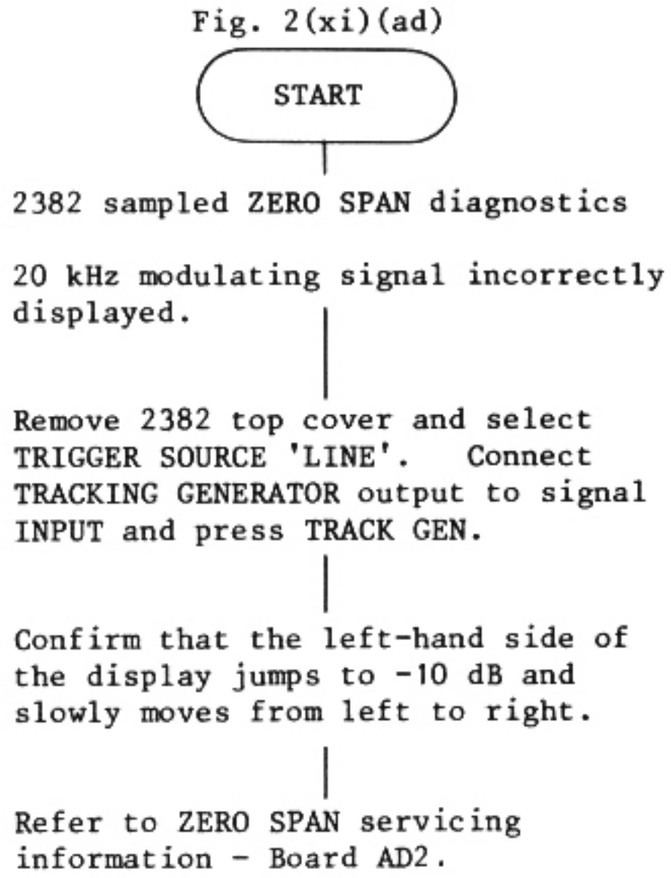


Fig. 25 Fault location chart - Sampled ZERO SPAN diagnostics

Fig. 2(xi)(ae)

Fig. 26 Fault location chart - 2382 triggering characteristics

- DIAGNOSTIC ROUTINES -

INTRODUCTION

7. As an aid to fault location the analyzer has a number of programmed diagnostic routines, grouped into self-test and self-calibration modes. The routines in the self-test mode are used to examine and set up various sections of the instrument. The routines in the self-cal mode are used to permanently calibrate appropriate sections; this calibration information is stored in non-volatile memory and is continuously used by the instrument until updated by running the calibration routine again.

8. The self-test mode allows access to four routines relating to the lower unit (2382) and also to a menu-driven diagnostic routine for the upper unit (2380) - see para. 72. The lower unit routines are:

(1) Display synthesizer conditions, comprising:

(a) Oscillator measurement delay
(b) Sweep fly-back delay

(2) Trace.

(3) Examine master oscillator frequencies.

(4) Calibration test routines, comprising:

(a) Check filter tuning and level
(b) Swept D - A checks
(c) View internal calibrator
(d) Decade calibration only
(e) Full calibration in debug mode

9. The self-cal mode allows access to two routines which affect sections of non-volatile memory.

(5) Oscillator voltage/frequency calibration, comprising:

(a) Full synthesizer calibration
(b) Single oscillator calibration
(c) Single oscillator linearizer control
(d) Sweep gain adjust control

(6) Tracking generator calibration

CAUTION ...

If the instrument should crash during a self-cal routine the non-volatile memory will remain corrupted even after power down. (If it should crash during a self-test routine no damage will occur and after the next power up the instrument will perform as usual.)

ACCESS TO SELF-TEST AND SELF-CAL MODES

10. To prevent unintended activation of these modes, access to them is protected by the following passwords:

Self-test mode

Select PRESET
Select and hold down INTMD IDENT while entering SET TG...23.82 dB
Release INTMD IDENT

Self-cal mode

Select PRESET
Select and hold down INTMD IDENT while entering SET TG...27.88 dB
Release INTMD IDENT

11. While either the self-test or self-cal mode is enabled a letter **D** (for Diagnostics) is displayed in the top right corner of the screen. To deselect either mode press 2nd FUNCT:ΔF SETS INC FREQ.

12. Access to each routine within these modes requires a further password as given after each heading. These password key entries are toggled so that a routine is deselected by re-entering the password.

Mode 1 - DISPLAY SYNTHESIZER CONDITIONS

13. Access. When in self-test mode (see para. 10),

Select 2nd FUNCT:MKR1 SETS REF LEVEL

This routine displays changes to the synthesizer as they take place. In order to generate a fixed set of conditions, enable the routine as shown above, then select PRESET and SWEEP MODE:SINGLE ARM in quick succession to stop the sweep, with six lines of synthesizer information displayed on the screen.

14. PRESET makes the instrument sweep and display the frequency range 0 to 400 MHz. The sweep is generated internally with several D to A converters which supply a shaped voltage waveform to one of three master voltage controlled oscillators: Osc0(AA5), Osc1(AB3), and Osc2(AB2). This waveform aims to sweep one of these oscillators from its left to right hand frequency in a linear fashion. The relationship between the input frequency (Fin) and that of the master oscillators is as follows:-

$$Fin = Osc0 - (502.6\ MHz + Osc1 + Osc2/32) \quad \ldots\ldots\ldots\ldots\ldots 1$$

15. Three special input frequencies are the left hand frequency (Finleft) the centre frequency (Fincentre) and the right hand frequency (Finright). These three points correspond to three sweep oscillator frequencies, FL, FC and FR. Rearranging equation 1 gives the following relationships:-

$$Osc0 = Fin + 502.6\ MHz + Osc1 + Osc2/32 \quad \ldots\ldots 2$$

$$Osc1 = Osc0 - (Fin + 502.6\ MHz + Osc2/32) \quad \ldots\ldots 3$$

$$Osc2 = 32(Osc0 - (Fin + 502.6\ MHz + Osc1)) \quad \ldots\ldots 4$$

16. If Osc0 is swept, equation 2 can be expanded to give the three sweep parameters as follows:-

$$FL = Finleft + 502.6\ MHz + Osc1 + Osc2/32 \quad \ldots\ldots 2a$$

$$FC = Fincentre + 502.6\ MHz + Osc1 + Osc2/32 \quad \ldots\ldots 2b$$

$$FR = Finright + 502.6\ MHz + Osc1 + Osc2/32 \quad \ldots\ldots 2c$$

17. In PRESET, with 400 MHz span/div, Finleft = 0 Hz, Fincentre = 200 MHz, Finright = 400 MHz; Osc0 is swept, Osc1 is phased locked at 30.5 MHz and Osc2 is free running at the displayed frequency. Substitution of these values into equations 2a, 2b and 2c will give the frequencies displayed to the right of FL, FC and FR.

18. In the /DIV mode the SPAN/DIV determines which oscillator is swept. Osc0 is swept on spans greater than 200 kHz/div, Osc2 on spans less than 5 kHz/div and Osc1 on all spans in between. For every span and input frequency combination, one oscillator sweeps between the frequencies FL and FR and the other two oscillators have fixed frequencies.

19. Enter a SPAN/DIV of 200 kHz. This will phase lock Osc0 at 735 MHz and change FL, FC and FR which are now defined by equations 3a, 3b and 3c.

$$FL = Osc0 - (Finleft + 502.6\ MHz + Osc2/32) \quad \ldots\ldots 3a$$

$$FC = Osc0 - (Fincentre + 502.6\ MHz + Osc2/32) \quad \ldots\ldots 3b$$

$$FR = Osc0 - (Finright + 502.6\ MHz + Osc2/32) \quad \ldots\ldots 3c$$

Reducing the span to 2 kHz/div will phase lock Osc0 at 735 MHz, phase lock Osc1 to 31.4 MHz and set FL, FC and FR as defined by equations 4a, 4b and 4c.

$$FL = 32(Osc0 - (Finleft + 502.6\ MHz + Osc1)) \quad \ldots\ldots 4a$$

$$FC = 32(Osc0 - (Fincentre + 502.6\ MHz + Osc1)) \quad \ldots\ldots 4b$$

$$FR = 32(Osc0 - (Finright + 502.6\ MHz + Osc1)) \quad \ldots\ldots 4c$$

Having checked the above equations select FULL SPAN.

20. After selecting any one of PRESET, FULL SPAN, /DIV, LOG, ZERO SPAN, FM DEMOD, METER, TRACK GEN, or changing REF FREQ, the instrument will calculate new sweep parameters FL, FC and FR, having decided on fixed frequencies for the other two oscillators.

21. Prior to starting the new sweep the master oscillators will be set to their theoretical frequencies and phase locked if necessary. This setting up sequence can be observed more clearly by introducing a delay into the system. Selecting 2nd FUNCT:REF LEVEL↑ five times sets the delay count to five as shown on the new line of information. Having set up the delay, select a SPAN/DIV of 100 Hz using the keypad.

22. The setting up procedure starts by clearing the screen. Osc0 is then set to 735 MHz. This is an iterative process which measures the oscillator and compensates for the frequency error by adjusting the Ref D to A's.

23. This measure-and-correct routine may be repeated as many as five times before the oscillator is within the capture range of the phase locked loop. The measured frequency of Osc0 is shown to the right of its theoretical frequency of 735 000 000 MHz. This same iterative process is used to set Osc1 to 30.5 MHz. When this is complete the sweep oscillator, in this case Osc2, is set to the frequency specified by FL. The left hand frequency is set when the two frequencies alongside FL differ by less than 0.2% of the span. Measured frequencies always appear to the right of the theoretical frequencies. Osc0 and Osc1 are then phase locked and remeasured to check that they have locked correctly before displaying the message **Phased locked.** Remove the delay by selecting 2nd FUNCT:RF LEVEL↓.

24. Select a span of 20 Hz/DIV and then select SWEEP MODE NORM. In SWEEP MODE NORM the frequency of the sweep oscillator is measured, at the reference position, and corrected if any drift has taken place. This is performed every ten seconds or at the end of a sweep, whichever is the greater. In this mode the oscillator is corrected at the end of every sweep and is shown immediately to the left of the * which indicates which oscillator is being swept. On this span setting the oscillator is set to the exact frequency, in this case 32 MHz. However, on other span settings the difference between the theoretical and measured frequencies should not differ by more than 0.2% of span. On spans less than 5 kHz/div the tolerance is 32 x 0.2%. Select 2nd FUNCT:MARKERS A B SELECT to display the Ref D to A's which are adjusted to maintain the centre frequency at 32 MHz. Changing the HORIZ POSN from centre, to left and back to centre will illustrate how the Ref D to A's are used. Displaying the Ref D to A's values may be of use if an oscillator is reluctant to set to the correct frequency. They will give a good indication of the troublesome area and the nature of the problem. For instance the Ref D to A adjustment may be unrelated to the required frequency correction. As above they may be used to monitor the sweep oscillator drift compensation. Remove the displayed Ref D to A values by selecting 2nd FUNCT:MARKER A B SELECT.

25. Set the span to 5 kHz/div and note the free running frequency of Osc2 and the frequency FL. On spans greater than 2 kHz/div, the free running frequency of Osc2 is measured at one minute intervals. Any change to the frequency of Osc2 is compensated for by a change to the sweep parameters. During these changes the screen is cleared and the new conditions are rewritten on the display.

26. The information on the bottom line relates to two of the D to A's which generate the sweep. The Sweep gain D to A adjusts the magnitude of the sweep. Its nominal value of 200 means a 1 bit change adjusts the sweep magnitude by 0.5%. In PRESET the value should lie between 198 and 202. Other synthesizer conditions may generate values between 190 (-5%) and 204 (+2%). Values outside this range may indicate that this adjustment is compensating for deficiencies elsewhere in the sweep generator. This may be due to incorrect shaping, faulty sweep amplifiers or sweep attenuators.

27. The other number indicates the number of sweep clocks which are required to sweep the oscillator to the right hand side of the screen, using a 12 bit Sweep D to A. Different synthesizer conditions will generate different right hand Sweep D to A values. This value will not exceed 4095 which indicates the maximum sweep voltage is being generated. The more volts that are required to sweep the oscillator the larger the number. This number therefore gives an indication of the voltage/frequency characteristic of the oscillator. Select a SPAN/DIV of 100 kHz and repeatedly select REF FREQ ↑. This will show the variation in sweep magnitude and hence the variation of voltage versus frequency as a function of FC.

Mode 1 (a) - OSCILLATOR MEASUREMENT DELAY

28. Access. When in mode 1 (see para. 13),

Select VERTICAL:A B SELECT to A

Selecting 2nd FUNCT:REF LEVEL↑ introduces a delay to the measurement of any oscillator. Successive selections of this control will increase the delay in half second increments. The number of half second delays is shown immediately to the right of DELAY on the top line of diagnostic information. This delay is removed by selecting 2nd FUNCT:REF LEVEL↓.

Mode 1 (b) - SWEEP FLYBACK DELAY

29. Access. When in mode 1 (see para. 13).

Select VERTICAL:A B SELECT to B

Selecting 2nd FUNCT:REF LEVEL↓ introduces a half second delay to the time between sweeps. Successive selections of this control will increase the delay in half second increments. The number of half second delays is shown immediately to the right of the top line diagnostic information. This delay is removed by selecting 2nd FUNCT:REF LEVEL↓.

30. This may be of use to confirm that the left hand sweep frequency is correct prior to the sweep restarting. Selecting TRACK GEN, having connected its output to a counter, will confirm whether the left hand frequency is stable and correct. If the frequency is wrong this test may indicate that a slave oscillator is wrong, having eliminated the master oscillators using Mode 3.

Mode 2 - TRACE

31. Access. When in self-test mode (see para. 10),

Select 2nd FUNCT:MKR1 SETS REF FREQ

This routine traces certain synthesizer activities and displays them as a 2-character column of numbers taking values between 01 and 99. Enabling this routine prior to a PRESET will trace the synthesizer activity and then clear the trace on the start of the new sweep. Pressing SWEEP MODE SINGLE ARM before /DIV will trace without clearing the screen. The displayed trace may be similar to the following:-

32
01
31
30

This indicates that the sweep linearity routine is enabled (32), that Osc0 (AA5) was measured once (01), that setting the left hand side of the sweep oscillator was delayed until the necessary calculations were completed (31) and that the sweep gain adjust routine is enabled (30). These numbers may be cleared by pressing SWEEP MODE START.

32. Entering a SPAN/DIV of 1 kHz via the 2380 keypad may result in the following trace:-

32
05
14
23
30

This indicates that Osc0 was measured five times (05), prior to Osc1 (AB3) being measured four times (14) and Osc2 (AB2) being measured three times (23).

33. The following list defines the trace codes already allocated

01)
02)
03)
04)
05 > 2nd column indicates the number of times Osc0 is measured
06)
07)
08)
09)

11)
12)
13)
14)
15 > 2nd column indicates the number of times Osc1 is measured
16)
17)
18)
19)

```
20    Measure free running frequency of Osc2
21 )
22 )
23 )
24 )
25  > 2nd column indicates the number of times Osc2 is measured
26 )
27 )
28 )
29 )

30    Adjust Sweep D to A gain routine enabled
31    Setting up of sweep oscillator delayed until completion of
      linearization calculations
32    Sweep linearization routine enabled
33    Sweep attenuator adjusted at insensitive region of oscillator
      voltage/frequency characteristic

44    Failed to phase lock Osc1
45    Failed to phase lock Osc1
```

34. In a faulty instrument the oscillators may be measured more than ten times in an attempt to set them to their required frequency. If this is not achieved within twenty attempts an error message is displayed and the routine is aborted and, in some cases, repeated indefinitely. This means that a TRACE of 01 to 20 can apply to Osc0, 11 to 30 to Osc1 and 21 to 40 to Osc2. It follows that TRACE numbers 11 to 40 have double definitions. Since the traces have a predicted pattern when switching between two instrument settings it is possible to determine what is happening. If in doubt enabling the Display Synthesizer Conditions with a suitable delay, as described in Mode 1, will clarify the situation.

Mode 3 - EXAMINE MASTER OSCILLATOR FREQUENCIES

35. Access. When in self-test mode (see para. 10),

Select 2nd FUNCT:MKR1 SETS INC FREQ

This routine puts the instrument into a special mode of operation. The sweep stops, the hardware is reconfigured to repeatedly measure and display the frequency of one of the master oscillators. Some of the MARKERS controls are redefined for oscillator selection and Ref D to A adjustment.

36. Selecting PRESET and then entering this routine displays the values of the Ref D to A's and states that Osc0 is tuneable. Rotating the MARKERS MOVE shaft encoder adjusts the value of the Coarse Ref D to A, indicated by the < pointer and as a result changes the frequency of Osc0. Selecting 2nd FUNCT:MARKERS 1 2 MOVE now addresses the Medium ref D to A which gives finer control of the oscillator frequency. The Fine ref D to A is addressed by selecting 2nd FUNCT:MKR2 and 2nd FUNCT:MKR1 returns to the original state addressing the Coarse ref D to A. The Ref D to A's can be set to any voltage within range, hence the oscillator to any frequency, using these four controls. This provides a simple way of checking the Ref D to A's for any hardware problems.

37. SELECT MARKER 1 2 MOVE to display the frequency of Osc1, which is phase locked at 30.5 MHz. The two frequencies displayed alongside Osc1, theoretical and measured, should not differ by more than the counter accuracy which is shown below to be ±128 Hz. Selecting MKR2 measures the free running frequency of Osc2. Its measured frequency, which by now will have drifted slightly, is shown to the right of its expected frequency. Return to Osc0 by selecting MKR1.

38. Select a SPAN/DIV of 200 kHz using the 2380 keyboard. This changes the synthesizer and phase locks Osc0 at 735 MHz. Measure Osc1 by selecting MARKERS 1 2 MOVE. Osc1 is now the sweep oscillator and as a result can be tuned. Select a SPAN/DIV of 2 kHz. Osc1 is now phase locked at 31.4 MHz and selecting MKR2 measures Osc2, the sweep oscillator, which is now tuneable.

39. Using the Ref D to A controls set the frequency of Osc2 to 32 MHz. Select MARKERS A B SELECT and set the frequency of Osc2 to 30 MHz. This exercise has set up two Ref D to A values which correspond to the above two frequencies. Continuously selecting MARKERS A B SELECT toggles between the two D to A values and hence the two selected frequencies. This may be of use for checking oscillator reactions to step frequency changes. Further adjustment to the Fine ref D to A values may be necessary to compensate for drift that takes place while setting up the two values.

40. Selecting 2nd FUNCT:MARKERS A B SELECT presets the D to A values to a maximum and minimum value, which is different for each oscillator, such that toggling the MARKERS A B SELECT now shows the maximum range of the oscillator. Typical ranges and measurement accuracies are listed below for each of the three oscillators.

	RANGE		MEASUREMENT ACCURACY
	Bottom	Top	
Osc0	523 ± 3 MHz	950 ± 5 MHz	±8.192 kHz
Osc1		34.35 ± 100 kHz	±128 Hz
Osc2		32.85 ± 400 kHz	±32 Hz

If the measured frequencies are under suspicion putting the jumper, on AD3 PLFT, between pins 2 and 3 should return measured values of 10 MHz for Osc1 and Osc2 and 640 MHz for Osc0. If this is the case any faults on the microprocessor board AD3 and the software are eliminated. Remember to replace the jumper between pins 1 and 2 of PLFT after completing this test.

Mode 4 - CALIBRATION TEST ROUTINES

41. Summary of operation. When in the self-test mode, selecting CAL on the 2380 keyboard displays the heading **Select debug mode.** This is followed by selecting 2nd FUNCT and one of the six MARKERS keys, which are redefined to allow different aspects of the CAL routine to be checked manually. When the test is complete selecting PRESET returns the system to its previous mode of operation. It is normal practice to enter one mode, check out the required area, then exit and re-enter another mode rather than jump between modes while Select debug mode is displayed.

The routines available are:

Check filter tuning and level

(i) All filters except 1 and 3 kHz

(ii) 1 and 3 kHz filter tune

Swept D to A checks

View internal calibrator signal

Decade calibrations only

Full calibrations in debug mode.

42. The spectrum analyzer CAL function is executed in order to set the gain of the signal path. The signal path is defined as the route that a signal takes in passing from the INPUT socket to the 2380 display. At a single frequency the gain of the signal path will depend on the following: the insertion loss and tuning of the resolution bandwidth filters, the gain of a series of amplifiers, the insertion loss of the input attenuators and the conversion loss of a number of mixers. Most of these parameters, as well as varying with age and temperature, vary with frequency.

43. A signal displayed at a level of -10 dB should remain so irrespective of the RF ATTEN setting. If for example the RF ATTEN is increased by 20 dB the signal path gain is maintained constant by increasing the i.f. gain by 20 dB. Some RESOLUTION BANDWIDTH filters introduce two more mixers into the signal path, others have different tuning characteristics and all have a different insertion loss. The input attenuator (RF ATTEN), input amplifier, input filter and input mixer all are frequency dependent so changes to the SPAN/DIV will have different effects on the signal path gain at different frequencies. Changes to the RF ATTEN, RESOLUTION BANDWIDTH or the SPAN/DIV will require a new set of gain correction figures. These correction figures are determined during the CAL routine, which first of all determines the filter tuning and insertion loss, using a fixed 10 dB RF ATTEN. Using a fixed 300 Hz RESOLUTION BANDWIDTH it then measures the gain for all the RF ATTEN to i.f. gain combinations and finally measures the instrument frequency response over the seven decades 100 Hz to 100 MHz.

44. There are three resolution filter groups; the 100 kHz i.f. (3 Hz to 30 Hz bandwidth) crystal filter bank, the 2.6 MHz i.f. 100 Hz to 3 kHz bandwidth) crystal filter bank and the 2.6 MHz i.f. 10 kHz to 1 MHz bandwidth) LC filter bank. Each group has varactor tuning and is adjusted from the d.c. output of an 8-bit D to 8 converter. The 100 kHz filter bank is connected to the tuning voltage at all times whilst the 2.6 MHz i.f. groups are only controlled when selected. During calibration, each group is peaked for a maximum signal on the 10 MHz calibration signal. Only the narrowest filter in each group is adjusted (i.e. the 3 Hz, 100 Hz and 10 kHz filters) since the wider bandwidth filters are automatically corrected by this adjustment.

41.1 Both crystal filter groups have the shunt stray capacitance of the bandwidth determining resistor neutralized by an inductor to avoid filter detuning at wide bandwidths when the damping resistor has a high value. On the 2.6 MHz filter bank, the temperature coefficient of the coil needs to be neutralized by adjustment of the bias to a varactor in shunt with the coil. Since the effect is

only significant on the 3 kHz filter, the same tuning D to A is used as LC detuning effects on this filter are negligible. This ´Null Strays´ compensation is also applied to the 1 kHz filter since the damping resistor detuning effect is just visible on this bandwidth. The value applied to this filter is 7 bits less than that applied to the 3 kHz filter to allow for small changes in circuit capacitance due to the reconfigured f.e.t. switching.

45. Single frequency gain compensations are made by writing the gain correction figures into a D to A to generate a voltage which then controls the gain of an i.f. amplifier by means of a pin diode. Gain compensation at different frequencies is achieved by software scaling the displayed data as it is transferred from the input store of the display unit to the display store and then the screen. This software scaling algorithm uses the data obtained during the decade section of the calibration routine.

Mode 4(a) - CHECK FILTER TUNING AND LEVEL

46. Select

RF ATTEN	10 dB
REF LEVEL	0 dB
dB/DIVISION	2 dB
REF FREQ	10 MHz
RESOLUTION BANDWIDTH	filter under test
SPAN/DIV	nearest span to ten times filter bandwidth under test

(i) All filters except 1 and 3 kHz

47. Enter the self-test mode (see para. 10) and select CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR1 to enter a manual cal mode where rotation of the MARKERS MOVE control updates the value of Freq D to A. This action varies the signal level count, which should be tuned for a maximum value. Some filters have many D to A values which give the same signal level count so, in this case, take the mean D to A value. Having set the maximum value exit from this test by selecting RESET.

48. To set the signal path gain press CAL followed by 2nd FUNCT:MKR1 2 MOVE. the MARKERS MOVE control now adjusts the Level D to A. In this mode a -10 dB calibration signal is internally fed through the signal path and its level is measured and displayed alongside the heading **Signal level.** When the signal path is correct the signal level count is 3904. A change of 1 count, to 3905, represents an increase in level or change in signal path gain of 0.025 dB. Set the signal level count to 3904 using the MARKERS MOVE control before leaving this routine via PRESET having calibrated this particular filter.

(ii) 1 and 3 kHz filter tune

49. Enter the self-test mode (see para. 10) and select CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR1 SETS REF LEVEL to enter a swept manual cal mode where rotation of the MARKERS MOVE control updates the value of the Filter tune D to A. Tune the filter so that it is symmetrical about the centre graticule line. Exit from this routine via PRESET before setting the signal path gain as described above.

Mode 4(b) SWEPT D to A CHECKS

50. Enter the self-test mode (see para. 10) and select CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR1 SETS REF LEVEL to enter a swept manual cal mode where rotation of the MARKERS MOVE control can update various D to A's which are selected using the re-defined MARKERS keys.

On entry the MARKERS MOVE control varies the Filter tune D to A. Select MARKERS A B SELECT to A and then select the following:-

2nd FUNCT:1 2 MOVE to vary the Sweep gain D to A.

2nd FUNCT:MKR2 to vary the Step D to A.

2nd FUNCT:MKR1 to vary the Filter tune D to A.

Select MARKERS A B SELECT to B and then select the following:-

2nd FUNCT:MKR1 to vary the TG level D to A.

These four routines allow the hardware to be checked while viewing either a signal or the tracking generator output.

Mode 4(c) VIEW INTERNAL CALIBRATOR SIGNAL

51. Enter the self-test mode (see para. 10) and select CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR1 SETS REF FREQ to view the internal calibrator. Exit via PRESET.

Mode 4(d) DECADE CALIBRATIONS ONLY

52. Connect INPUT to TRACKING GENERATOR output.

Select TRACK GEN.

Enter the self-test mode (see para. 10) and press CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR2 to start the decade calibrations. Exit via PRESET or automatically after 100 MHz decade.

Mode 4(e) FULL CALIBRATION IN DEBUG MODE

53. Enter the self-test mode (see para. 10) and press CAL to display the heading **Select debug mode.** Follow this with 2nd FUNCT:MKR1 SETS INC FREQ to start the calibration sequence. Exit via PRESET or automatically after 100 MHz decade.

In this mode it is possible to use the delay facilities, described in Modes 1(b) and 1(c), to look more closely at the calibration figures.

Mode 5 - OSCILLATOR VOLTAGE/FREQUENCY CALIBRATION

54. Summary of operation. When in the self-cal mode selecting 2nd FUNCT:SWEEP MODE NORM displays the heading **Select cal mode.** This is then followed by one of the eight HORIZONTAL keys, which either starts a voltage frequency calibration or enables/disables sweep generator correction algorithms.

55. There are three L-C master oscillators in the 2382 which have a non-linear voltage/frequency characteristic. In the past, diode shapers were used to distort a sweep ramp before applying it to an oscillator to set a linear frequency sweep. Many man-hours were required to set up these shapers to give the 10% linearity figures they achieved. The 2382 uses digital techniques, in the form of look-up tables and interrupts, to generate the voltage waveform applied to the master oscillators.

56. The information necessary to generate the sweep is stored in non-volatile memory during the oscillator calibration procedures. In this calibration sequence the oscillator is stepped through its frequency range, using the Ref D to A's, in increments of either 5 MHz, 200 kHz or 120 kHz for Osc0, 1 and 2 respectively. These increments are known as the frequency zones. Another voltage, from the Sweep D to A, is switched through to the oscillator and varied until it offsets the oscillator by the amount specified by the frequency zone. The resulting number of bits is the voltage required to move the oscillator by its frequency zone at that particular frequency.

57. After a successful calibration the unit enables the two linearity functions which are then used each time the sweep is changed. The major function is the digital sweep shaper which maintains sweep performance non-linearity figures of 2%. Analogue sweep gain adjustment, which is the other function, makes a fine adjustment to the sweep in order to guarantee the specification. Even though a unit is calibrated it is possible to switch off the linearity functions to look at the true oscillator characteristic. In order to demonstrate the effects of these routines follow the examples below. It is however essential to warn you that any changes you make are recorded in non-volatile memory and so remain changed even after power down.

58. Access. When in the self-cal mode (see para. 10),

Select 2nd FUNCT:MKR1 SETS REF FREQ

Select:

PRESET
HORIZ POSN ..... left hand reference
SPAN/DIV ..... 10 MHz
REF FREQ ..... 0 MHz
SWEEP TIME ..... 1 s/div
B VIEW
SWEEP MODE SINGLE ARM

Connect INPUT to STD 10 MHz OUTPUT.

59. At the end of the sweep, select B SAVE followed by HORIZONTAL/DIV. If the instrument is calibrated the TRACE column should display 32, a number between 1 and 20, and 30. Display A and B should have the 10 MHz harmonics displayed on the major graticule lines. Select 2nd FUNCT:SWEEP MODE NORM, to display the heading **Select cal mode**, followed by 2nd FUNCT:SWEEP MODE START to disable the sweep gain adjust algorithm. While watching the display select SWEEP MODE START to see the new A display differ slightly from that of the stored B display. Selecting HORIZONTAL/DIV will display a new TRACE column which no longer includes a 30 and so indicates that the sweep gain adjust routine is disabled.

60. Select 2nd FUNCT:SWEEP MODE NORM, to display the heading **Select cal mode**, followed by 2nd FUNCT:RESOLUTION BANDWIDTH ↓ to disable the digital sweep shaper algorithm. While watching the display, select SWEEP MODE START to see the new A display differ considerably from that of the stored B display. Selecting HORIZONTAL/DIV will display a new TRACE column which no longer includes a 32 and so indicates that the linearizer or digital sweep shaper routine is disabled.

61. The sweep gain adjust routine is either on or off but each oscillator has its own linearizer which can be enabled or disabled using the three RESOLUTION BANDWIDTH selection keys.

62. Return the instrument back to its original state by selecting 2nd FUNCT:SWEEP MODE NORM, 2nd FUNCT:RESOLUTION BANDWIDTH ↓, 2nd FUNCT:SWEEP MODE NORM and 2nd FUNCT:SWEEP MODE START. Select 2nd FUNCT:MKR1 SETS REF FREQ to remove the TRACE.

Mode 5(a) - FULL SYNTHESIZER CALIBRATION

63. Select

PRESET
A VIEW ..... off
B VIEW
B SAVE

Enter the self-cal mode (see para. 10), and then select 2nd FUNCT:SWEEP MODE NORM to display the heading **Select cal mode.** Follow this with 2nd FUNCT:AUTO TRIG to start the calibration sequence.

64. Displayed to the right of TOP and BOT is the upper and lower frequency of the zone being calibrated. To the left of the * are the measured frequencies which occur during the iterative setting up procedure. The bottom frequency is set using the Ref D to A and the top by the Sweep D to A. When the top frequency is correct the Sweep D to A value is displayed alongside Sweep gain D to A 200 as well as being plotted on the B display. This routine steps up to a frequency of 943 MHz, and indicates whether the Osc0 calibration is successful before moving on to calibrate Osc1. This calibration, as well as Osc2, steps down in frequency tracing the new characteristic over the last one. The total calibration sequence is complete when the calibration message is removed from alongside Osc2. This routine can be slowed down by selecting 2nd FUNCT:REF LEVEL ↑ or ↓ to introduce delays as described in Mode 1 (b). Pressing PRESET returns the instrument to its previous mode of operation.

Mode 5(b) - SINGLE OSCILLATOR CALIBRATION

65. Select:

PRESET
A VIEW ..... off
B VIEW
B SAVE

Enter the self-cal mode and then select 2nd FUNCT:SWEEP MODE NORM to display the heading **Select cal mode.**

Follow this with either:-

2nd FUNCT:SWEEP TIME ↓ for OscO
or 2nd FUNCT:SWEEP TIME for OsCl
or 2nd FUNCT:SWEEP TIME ↑ for Osc2

66. This routine is a means of investigating one oscillator calibration that may have failed a FULL SYNTHESIZER CAL. It is part of a FULL SYNTHESIZER CAL routine and so all information applies equally to both routines.

Mode 5(c) - SINGLE OSCILLATOR LINEARIZER CONTROL

67. Enter the self-cal mode (see para. 10), and then select 2nd FUNCT:SWEEP MODE NORM to display the heading **Select cal mode.** Following this with either:-

2nd FUNCT:RESOLUTION BANDWIDTH ↓ for OscO
or 2nd FUNCT:RESOLUTION BANDWIDTH AUTO for Oscl
or 2nd FUNCT:RESOLUTION BLANDWIDTH ↑ for Osc2

The above sequence, if repeated, enables and disables the relevant routine on successive selections. If unsure of its use refer to the example described at the beginning of Mode 5 above.

Mode 5(d) - SWEEP GAIN ADJUST CONTROL

68. Enter the self-cal mode (see para. 10), and then select 2nd FUNCT:SWEEP MODE NORM to display the heading **Select cal mode.** Follow this with 2nd FUNCT:SWEEP MODE START to select or deselect this routine on successive selections. If unsure of its use refer to the example described at the beginning of Mode 5 (para. 54).

Mode 6 - TRACKING GENERATOR CALIBRATION

69. Access. When in the self-cal mode (see para. 10), selecting 2nd FUNCT:SWEEP MODE NORM displays the heading **Select cal mode.** When the instrument is set up in a particular way 2nd FUNCT:TRACK GEN will calibrate the TRACKING GENERATOR levels.

The purpose of this calibration is to load into non-volatile memory the tracking generator D to A settings which give all the levels between, and including, -9.7 dB to -20.3 dB in 0.1 dB steps.

Select:

PRESET
TRACK GEN
CAL

Connect INPUT to TRACKING GENERATOR output

Wait for the System Calibration routine to finish and then select 2nd FUNCT:SWEEP MODE NORM to display the heading **Select cal mode.** Follow this with 2nd FUNCT:TRACK GEN to start the cal routine.

70. First of all this procedure recalibrates the 100 Hz filter for setting the tracking generator level to a minimum by writing zero to the D to A. It then increases the D to A count until the 2380 received Signal level is greater than the required (Req) level. At this point it stores away the D to A value for this particular Cal zone and then increases the required level by 4 counts which is equivalent to 0.1 dB. It steps from the first Req level of 3492 (-20.3 dB), 4 counts at a time, past 3504 (-20.0 dB), 3904 (-10.0 dB) to 3916 which is -9.7 dB.

71. This routine can be slowed down by selecting 2nd FUNCT:REF LEVEL ↑ or ↓ to introduce delays as described in Mode 1 (b). It is possible to abort the calibration at any time by selecting PRESET.

Mode 7 - ERROR CODES

72. Access: Whilst in either self-test mode or self-cal mode. The error message is displayed in the format:-

Error (B or T) (number) (address) (error message)

e.g. **Error T4 20BF 0038 Invalid operation**

Where:

B	=	error originated from bottom unit
T	=	error originated from top unit
Number	=	error code
address	=	address at which error was detected
error message	=	corresponding message to error code in the range 1 to 39.

When not in diagnostics if the error codes 1 to 39 are generated the corresponding message in Table 1 is flagged. If error codes 40 to 53 are generated then the message ´Synthesizer error´ is flagged.

MENU DRIVEN DIAGNOSTIC TESTS

73. This section describes a number of menu driven test facilities, mainly concerned with the upper unit (2380).

74. Access. When in self-test mode (see para. 8),

Select 2nd FUNCT:REF FREQ ↑

This will display the debug menu with 5 options:

0 Exit debug operation
1 I/O port access [upper & lower units]
2 Upper unit confidence tests
3 Lower unit confidence tests
4 Inter unit bus test

75. Select the required option, as below, using the numeric keypad.

[0] **Exit debug operation.** This returns the instrument to the self-test mode.

TABLE 1 ERROR MESSAGE LIST

Error number	Description
1	Unrecognized header on inter-unit bus
2	Unrecognized key
3	Sweep out of sync
4	Invalid operation
5	Options not installed
6	DO CASE over-run
7	Invalid store operation
8	Illegal DATA entry
9	Data entry out of range
10	Divide error
11	Invalid sweep condition
12	Out of range
13	- Not allocated -
14	Failed on calibration
15	Noise in 1 Hz selected on ZERO SPAN
16	No response from lower unit
17	Integer arithmetic overflow
18	GPIB: Unidentified block data
19	Overheating
20	GPIB: Max line length exceeded
21	GPIB: Unrecognized header
22	GPIB: Unavailable item
23	GPIB: Invalid data field
24	GPIB: No listeners - output aborted
25	GPIB: Invalid checksum
26	GPIB: Incompatible binary data
27	GPIB: Too many mask limits
28	GPIB: No tracking generator fitted
29	-
30	Lost track
31	Write protected store NOT cleared
32	I/P buffer full error
33	-
34	-
35	GPIB: Array BLOCK DATA overflow
36	GPIB: Attempt to read an empty input buffer
37	-
38	GPIB: Output buffer overflow
39	GPIB: Failed to write output data
40	Failed to set oscillator 0
41	Failed to set oscillator 1
42	Failed to set oscillator 2
43	Sweep gain D to A adjust range exceeded
44	Osc 0 not phase locked
45	Osc 1 not phase locked
46	Sweep D to A error in osc. calibration
47	Sweep D to A error in osc. calibration
48	Non-volatile memory cleared
49	Oscillator 1 and 2 out of range
50	
51	Log amplifier sweep abort failure
52	Log amplifier sweep abort failure
53	Linearization failure

[1] **I/O port access.** This allows a byte to be written to any port in either the upper or lower unit. When this mode is selected the following choice is offered:

0 Exit I/O operations
1 Enter upper unit I/O port parameters
2 Enter lower unit I/O port parameters

76. Selecting 0 will return to the debug menu. Selecting 1 or 2 will display the message **Enter port number [Hex]** or, for the lower unit, **[Oct]**. (This is to tie up with the circuit diagrams as upper unit chip selects are hexadecimal, and lower unit ones octal). The message **Terminate entry with minus [-] key** is also displayed. After entering a port number and terminating using the numeric keypad the message **Enter port value [Bin]** 00000000 is added to the display. The value can be changed using the '1' and '0' keys, and terminating with the '-' key. The screen is then cleared, and the above menu is displayed.

CAUTION ...

Be very careful in using this facility, as it is possible to write to any of the complex microprocessor peripherals, with unpredictable results.

[2] **Upper unit confidence tests.** This will display the upper unit test menu with 6 options:

0 Exit upper unit tests
1 Enter keyboard & shaft encoder tests
2 Enter data display & linearity tests
3 Enter marker tests
4 Enter read in bright up test
5 Enter options board test

Selecting 0 will return to the debug menu.

77. Selecting 1 will enter the keyboard and shafter encoder tests. For the key test, boxes display the last key pressed and the next key to press in the test sequence. Turning the shaft encoder moves an asterisk left and right across the screen whilst incrementing counts in boxes on either side.

78. Selecting 2 puts two ramps on the screen, the 'A' trace going from top left to bottom right, and the 'B' trace bottom left to top right. The ramps are software generated, and therefore test the display storage system. A border on the outside of the picture area, with an outline around the corner character cell and a cross through its centre, aids focusing and display size setting. The VIEW and INFILL keys for both Channels, and the GRAT key (and therefore display on/off) all work, allowing the associated hardware to be tested. The hardware on the display maths board (AB4) can be tested using the shaft encoder to drive the shift latches, thus moving the ramp up and down; the numeric keys 1-4 drive the 2 to 16 sections and the numeric key 0 drives the x1, x5 section, thus changing the slope of the ramp. The SAVE keys for the A and B displays are interlocked, and the LED indicates which display is being changed.

79. Selecting 3 puts the same two ramps on the screen, but turning the shaft encoder moves a flashing marker along either the A or B trace depending on the SAVE keys. This tests smooth operation of the marker circuitry.

80. Selecting 4 puts the same two ramps on the screen, but turning the shaft encoder moves the read in bright up across the screen.

81. Selecing 5 displays the options menu. The **Beeper** tests are found by selecting 1. The modes 1-7 test different modes of operation of the beeper. The **Colour palette** selection is on 2, and switches between strong and normal colours. Finally **Pen Plot** is entered with 3, putting the instrument into normal pen plot mode with the ramps for display.

82. In modes 1 to 4 pressing the ´DELETE´ key twice returns to the upper unit diagnostic menu.

[3] **Lower unit confidence tests.** This option is not used - refer to the self-test mode routines (para. 9) for lower unit diagnostics.

[4] **Inter unit bus test.** In this option the upper unit sends an LF (line feed) byte to the lower unit every 100 ms and checks that the lower unit echoes them back. This confirms that the inter unit link is correct.

SIGNAL PATH LEVELS

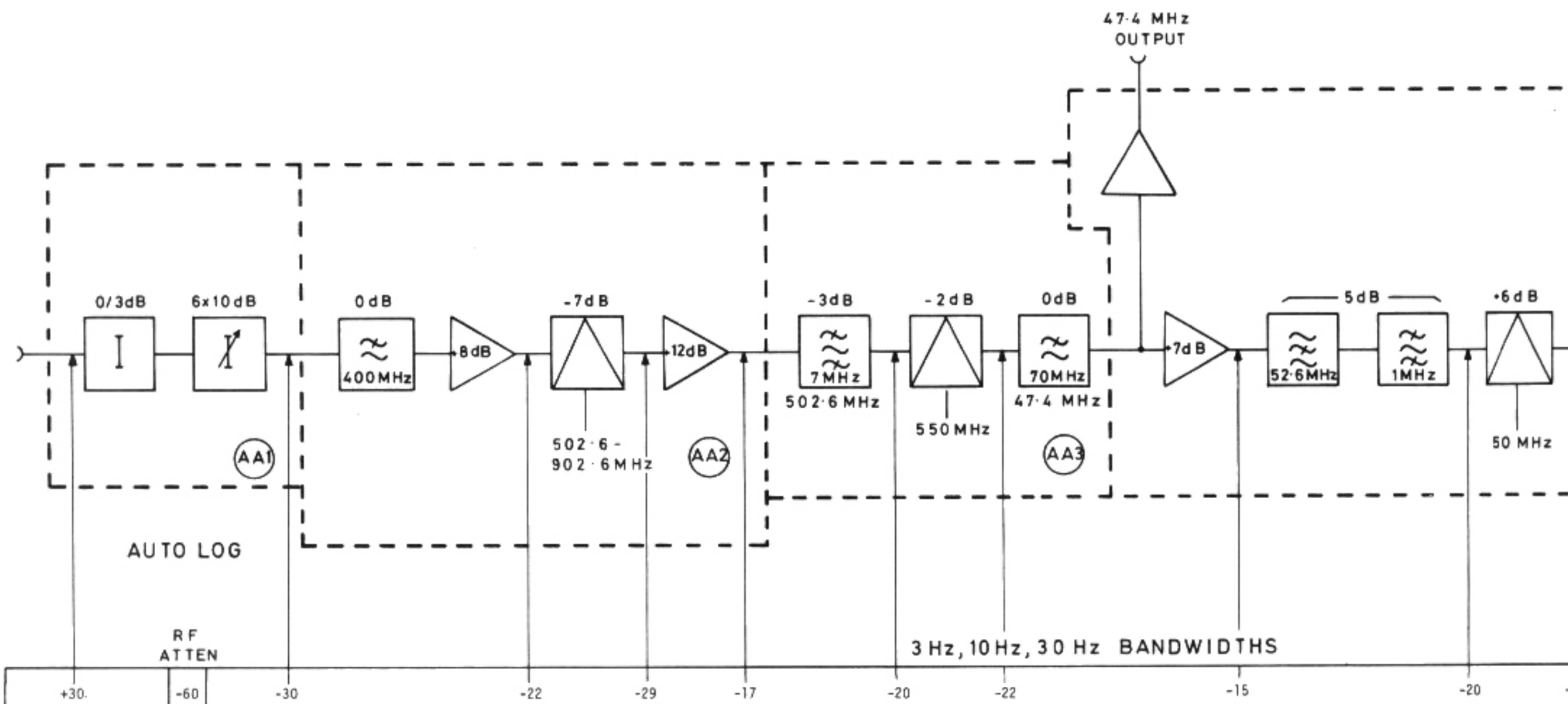
Levels

83. For maintenance purposes Figs. 27 and 28 show simplified block diagrams of the r.f. unit under which are tabulated the main signal path levels for logarithmic operation in the auto mode. Signal input levels are those for a 50 Ω terminated signal applied to the INPUT socket. For dBm to millivolt conversion see Table 2.

Useful relationships

84. The following relationships are applicable to this instrument:-

0 dBm, 50 Ω = 223.61 mV r.m.s.
-10 dBm, 50 Ω = 70.71 mV r.m.s.
dBV = dBm, 50 Ω -13.01 dB
dBμV = dBm, 50 Ω +106.99 dB
0 dBc - Top of screen at time of selecting ´dB´.



RF ATTEN									
+30	-60	-30	-22	-29	-17	-20	-22	-15	-20
+20	-60	-40	-32	-39	-27	-30	-32	-25	-30
+10	-50	-40	-32	-39	-27	-30	-32	-25	-30
0	-40	-40	-32	-39	-27	-30	-32	-25	-30
-10	-30	-40	-32	-39	-27	-30	-32	-25	-30
-20	-20	-40	-32	-39	-27	-30	-32	-25	-30
-30	-10	-40	-32	-39	-27	-30	-32	-25	-30
-40	0	-40	-32	-39	-27	-30	-32	-25	-30
-50↔150	0	-50	-42	-49	-37	-40	-42	-35	-40

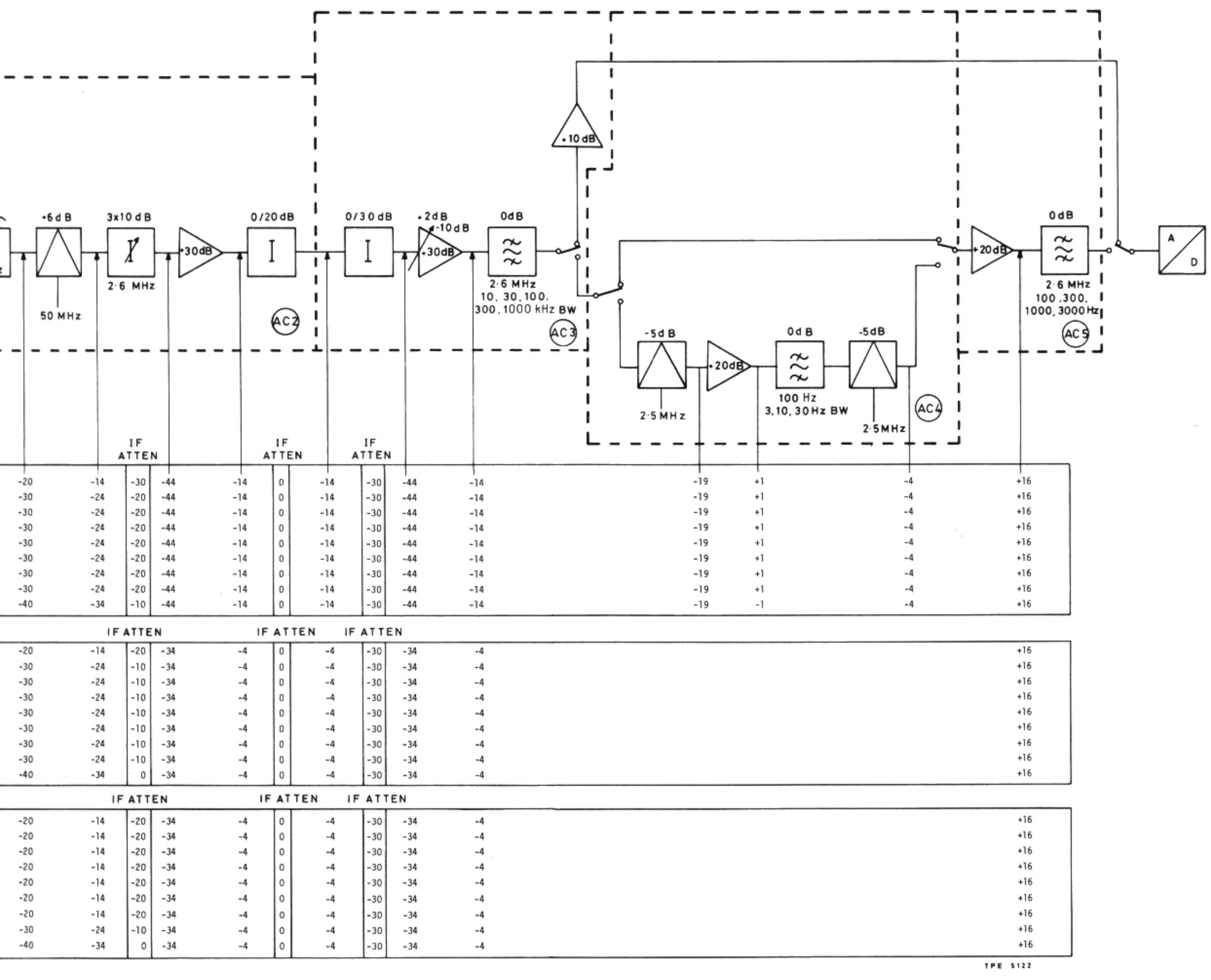
100 Hz BANDWIDTHS

RF ATTEN									
+30	-60	-30	-22	-29	-17	-20	-22	-15	-20
+20	-60	-40	-32	-39	-27	-30	-32	-25	-30
+10	-50	-40	-32	-39	-27	-30	-32	-25	-30
0	-40	-40	-32	-39	-27	-30	-32	-25	-30
-10	-30	-40	-32	-39	-27	-30	-32	-25	-30
-20	-20	-40	-32	-39	-27	-30	-32	-25	-30
-30	-10	-40	-32	-39	-27	-30	-32	-25	-30
-40	0	-40	-32	-39	-27	-30	-32	-25	-30
-50↔150	0	-50	-42	-49	-37	-40	-42	-35	-40

300 Hz, 1kHz, 3kHz BANDWIDTHS

RF ATTEN									
+30	-60	-30	-22	-29	-17	-20	-22	-15	-20
+20	-50	-30	-22	-29	-17	-20	-22	-15	-20
+10	-40	-30	-22	-29	-17	-20	-22	-15	-20
0	-30	-30	-22	-29	-17	-20	-22	-15	-20
-10	-20	-30	-22	-29	-17	-20	-22	-15	-20
-20	-10	-30	-22	-29	-17	-20	-22	-15	-20
-30	0	-30	-22	-29	-17	-20	-22	-15	-20
-40	0	-40	-32	-39	-27	-30	-32	-25	-30
-50↔150	0	-50	-42	-49	-37	-40	-42	-35	-40

Fig. 27 Signal path levels for auto



-20	-14	-30	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-30	-24	-20	-44	-14	0	-14	-30	-44	-14	-19	+1	-4	+16
-40	-34	-10	-44	-14	0	-14	-30	-44	-14	-19	-1	-4	+16

IF ATTEN IF ATTEN IF ATTEN

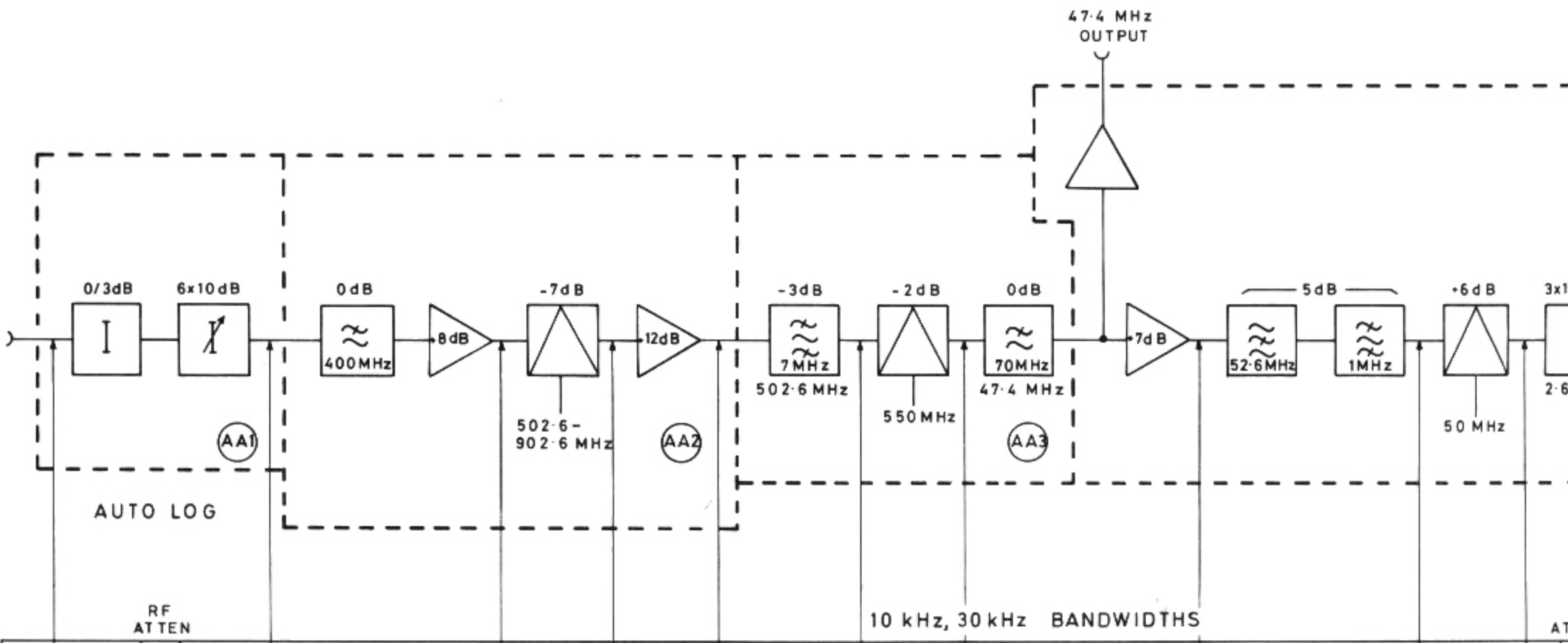
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-40	-34	0	-34	-4	0	-4	-30	-34	-4	+16

IF ATTEN IF ATTEN IF ATTEN

-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-20	-14	-20	-34	-4	0	-4	-30	-34	-4	+16
-30	-24	-10	-34	-4	0	-4	-30	-34	-4	+16
-40	-34	0	-34	-4	0	-4	-30	-34	-4	+16

TPE 5122

for auto log operation (3 Hz to 3 kHz bandwidths)



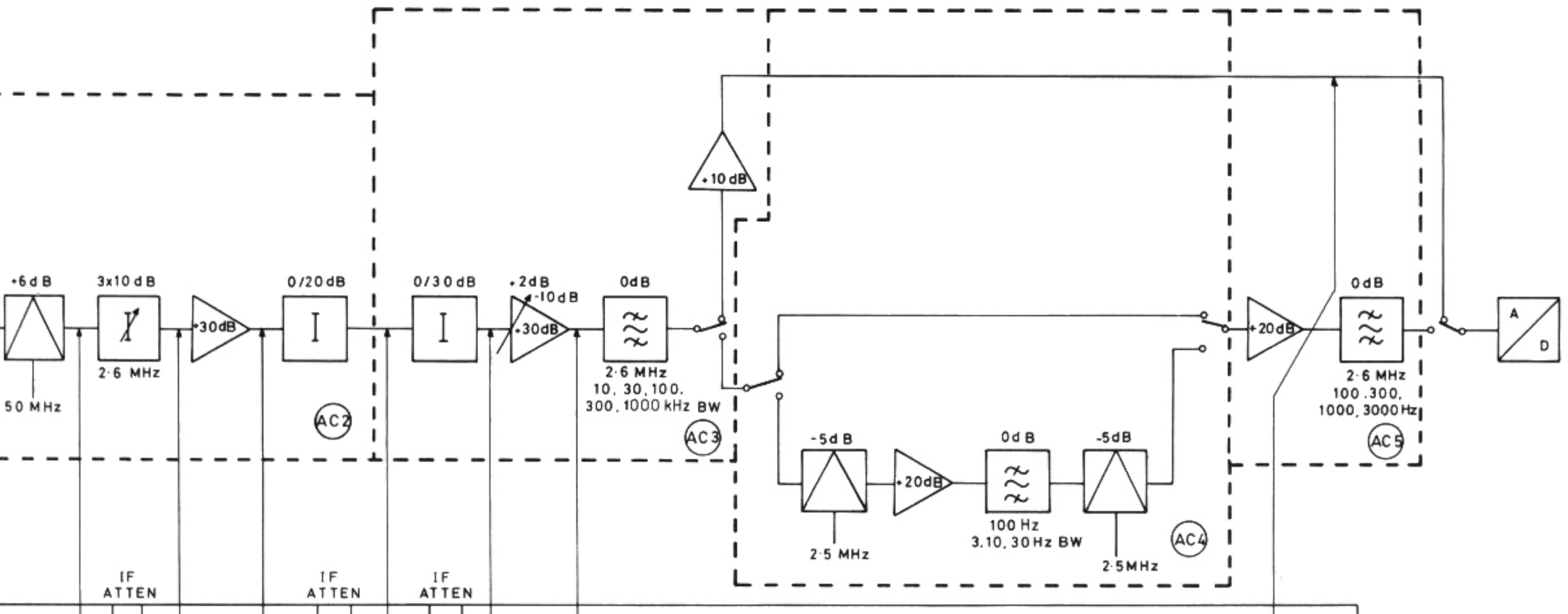
+30	-60	-30	-22	-29	-17	-20	-22	-15	-20	-14
+20	-50	-30	-22	-29	-17	-20	-22	-15	-20	-14
+10	-40	-30	-22	-29	-17	-20	-22	-15	-20	-14
0	-30	-30	-22	-29	-17	-20	-22	-15	-20	-14
-10	-20	-30	-22	-29	-17	-20	-22	-15	-20	-14
-20	-10	-30	-22	-29	-17	-20	-22	-15	-20	-14
-30	0	-30	-22	-29	-17	-20	-22	-15	-20	-14
-40	0	-40	-32	-39	-27	-30	-32	-25	-30	-24
-50↔150	0	-50	-42	-49	-37	-40	-42	-35	-40	-34

0·1 MHz, 0·3 MHz, 1 MHz BANDWIDTHS

RF ATTEN

+30	-50	-20	-12	-19	-7	-10	-12	-5	-10	-4
+20	-40	-20	-12	-19	-7	-10	-12	-5	-10	-4
+10	-30	-20	-12	-19	-7	-10	-12	-5	-10	-4
0	-20	-20	-12	-19	-7	-10	-12	-5	-10	-4
-10	-10	-20	-12	-19	-7	-10	-12	-5	-10	-4
-20	0	-20	-12	-19	-7	-10	-12	-5	-10	-4
-30	0	-30	-22	-29	-17	-20	-22	-15	-20	-14
-40	0	-40	-32	-39	-27	-30	-32	-25	-30	-24
-50↔-150	0	-50	-42	-49	-37	-40	-42	-35	-40	-34

Fig. 28 Signal path levels for auto l



-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-24	0	-24	+6	0	+6	-30	-24	+6
-34	0	-34	-4	-20	-24	0	-24	+6

IF ATTEN				IF ATTEN		IF ATTEN		
-4	-20	-24	+6	0	+6	-30	-24	+6
-4	-20	-24	+6	0	+6	-30	-24	+6
-4	-20	-24	+6	0	+6	-30	-24	+6
-4	-20	-24	+6	0	+6	-30	-24	+6
-4	-20	-24	+6	0	+6	-30	-24	+6
-4	-20	-24	+6	0	+6	-30	-24	+6
-14	-10	-24	+6	0	+6	-30	-24	+6
-24	0	-24	+6	0	+6	-30	-24	+6
-34	0	-34	-4	-20	-24	0	-24	+6

TPE 5120

r auto log operation (10 kHz to 1 MHz bandwidths)

TABLE 2 dBm/mV CONVERSION

dBm	(50 Ω)		(75 Ω)	
	Millivolts (r.m.s.)	Millivolts (p-p)	Millivolts (r.m.s.)	Millivolts (p-p)
20.0	2236.068	6324.562	2738.613	7745.975
17.5	1676.814	4742.752	2053.670	5808.662
15.0	1257.434	3556.563	1540.035	4355.882
12.5	942.942	2667.046	1154.864	3266.451
10.0	707.107	2000.002	866.025	2449.492
7.5	530.255	1499.790	649.427	1836.860
5.0	397.635	1124.684	487.002	1377.451
2.5	298.184	843.394	365.200	1032.942
0.0	223.607	632.456	273.861	774.597
-2.5	167.681	474.275	205.367	580.866
-5.0	125.743	355.656	154.004	435.588
-7.5	94.294	266.705	115.486	326.645
-10.0	70.711	200.000	86.603	244.949
-12.5	53.026	149.979	64.943	183.686
-15.0	39.764	112.468	48.700	137.745
-17.5	29.818	84.339	36.520	103.294
-20.0	22.361	63.246	27.386	77.460
-22.5	16.768	47.428	20.537	58.087
-25.0	12.574	35.566	15.400	43.559
-27.5	9.429	26.670	11.549	32.665
-30.0	7.071	20.000	8.660	24.495
-32.5	5.303	14.998	6.494	18.369
-35.0	3.976	11.247	4.870	13.775
-37.5	2.982	8.434	3.652	10.329
-40.0	2.236	6.325	2.739	7.746
-42.5	1.677	4.743	2.054	5.809
-45.0	1.257	3.557	1.540	4.356
-47.5	0.943	2.667	1.155	3.266
-50.0	0.707	2.000	0.866	2.449
-52.5	0.530	1.500	0.649	1.837
-55.0	0.398	1.125	0.487	1.377
-57.5	0.298	0.843	0.365	1.033
-60.0	0.224	0.632	0.274	0.775
-62.5	0.168	0.474	0.205	0.581
-65.0	0.126	0.356	0.154	0.436

continued ...

TABLE 2 dBm/mV CONVERSION (continued)

dBm	(50 Ω)		(75 Ω)	
	Millivolts (r.m.s.)	Millivolts (p-p)	Millivolts (r.m.s.)	Millivolts (p-p)
-67.5	0.094	0.267	0.115	0.327
-70.0	0.071	0.200	0.087	0.245
-72.5	0.053	0.150	0.065	0.184
-75.0	0.040	0.112	0.049	0.138
-77.5	0.030	0.084	0.037	0.103
-80.0	0.022	0.063	0.027	0.077
-82.5	0.017	0.047	0.021	0.058
-85.0	0.013	0.036	0.015	0.044
-87.5	0.009	0.027	0.012	0.033
-90.0	0.007	0.020	0.009	0.024
-92.5	0.005	0.015	0.006	0.018
-95.0	0.004	0.011	0.005	0.014
-97.5	0.003	0.008	0.004	0.010
100.0	0.002	0.006	0.003	0.008

Attenuator and gain settings

85. Attenuator and gain settings depend upon both the mode of operation and the bandwidth selected; those for logarithmic and linear auto operation are shown in Tables 3 and 4 respectively. IF attenuator selection used to set the i.f. gains given in these two tables is shown in Table 5.

TABLE 3 AUTO MODE LOG OPERATION - ATTENUATOR AND GAIN SETTINGS

Recorded ref. level	4304 level of total A-D output	Filter selected									
		3Hz,10Hz,30Hz		100Hz		300Hz,1kHz,3kHz		10kHz,30kHz		0.1MHz.0.3MHz,1MHz	
		RF Atten	IF Gain	RF Atten	IF Gain	RF Atten	IF Gain	RF Atten	IF Gain	RF Atten	IF Gain
+30 dBm	+30 dBm	60 dB	0 dB	60 dB	10 dB	60 dB	10 dB	60 dB	20 dB	50 dB	10 dB
+20 dBm	+20 dBm	60 dB	10 dB	60 dB	20 dB	50 dB	10 dB	50 dB	20 dB	40 dB	10 dB
+10 dBm	+10 dBm	50 dB	10 dB	50 dB	20 dB	40 dB	10 dB	40 dB	20 dB	30 dB	10 db
0 dBm	0 dBm	40 dB	10 dB	40 dB	20 dB	30 dB	10 dB	30 dB	20 dB	20 dB	10 dB
-10 dBm	-10 dBm	30 dB	10 dB	30 dB	20 dB	20 dB	10 dB	20 dB	20 dB	10 dB	10 dB
-20 dBm	-20 dBm	20 dB	10 dB	20 dB	20 dB	10 dB	10 dB	10 dB	20 dB	0 dB	10 db
-30 dBm	-30 dBm	10 dB	10 dB	10 db	20 dB	0 dB	10 dB	0 dB	20 dB	0 dB	20 db
-40 dBm	-40 dBm	0 dB	10 dB	0 dB	20 dB	0 dB	20 dB	0 dB	30 dB	0 dB	30 db
-50→-150	-50 dBm	0 dB	20 dB	0 dB	30 dB	0 dB	30 dB	0 dB	40 dB	0 dB	40 dB

TABLE 4 AUTO MODE LIN OPERATION - ATTENUATOR AND GAIN SETTINGS

Recorded sensitivity	1000 level of A-D output	RF atten	IF gain			Lin select AD1		Filter for 1% f.s.d. noise*
			Wide BW	Med. BW	Nar. BW	1,2(L)	5L	
500 mV/div	10 V	60 dB	0 dB	-10 dB	-20 dB	1	0	
200 mV/div	5 V	60 dB	0 dB	-10 dB	-20 dB	0	1	
100 mV/div	2.5 V	60 dB	0 dB	-10 dB	-20 dB	0	1	
50 mV/div	1 V	40 dB	0 dB	-10 dB	-20 dB	1	0	
20 mV/div	500 mV	40 dB	0 dB	-10 dB	-20 dB	0	1	
10 mV/div	250 mV	40 dB	0 dB	-10 dB	-20 dB	0	1	
5 mV/div	100 mV	20 dB	0 dB	-10 dB	-20 dB	1	0	
2 mV/div	50 mV	20 dB	0 dB	-10 dB	-20 dB	0	1	
1 mV/div	25 mV	20 dB	0 dB	-10 dB	-20 dB	0	1	
500 µV/div	10 mV	0 dB	0 dB	-10 dB	-20 dB	1	0	
200 µV/div	5 mV	0 dB	0 dB	-10 dB	-20 db	0	1	
100 µV/div	2.5 mV	0 dB	0 dB	-10 dB	-20 dB	0	1	
50 µV/div	1 mV	0 dB	20 dB	10 dB	0 dB	1	0	1 MHz
20 µV/div	500 µV	0 dB	20 dB	10 dB	0 dB	0	1	300 kHz
10 µV/div	250 µV	0 dB	20 dB	10 dB	0 dB	0	1	100 kHz
5 µV/div	100 µV	0 dB	40 dB	30 dB	20 dB	1	0	10 kHz
2 µV/div	50 µV	0 dB	40 dB	30 dB	20 dB	0	1	3 kHz
1 µV/div	25 µV	0 dB	40 dB	30 dB	20 dB	0	1	1 kHz
500 nV/div	10 µV	0 dB	60 dB	50 dB	40 dB	1	0	100 Hz
200 nV/div	5 µV	0 dB	60 dB	50 dB	40 dB	0	1	30 Hz
100 nV/div	2.5 µV	0 dB	60 dB	50 dB	40 dB	0	1	10 Hz

* Assuming -150 dBm noise floor for 3 Hz filter

TABLE 5 IF ATTENUATOR SELECTION

IF gain (dB)	Attenuation (dB)		
	3 x 10	0/20	0/30
-20	30	20	30
-10	20	20	30
0	30	0	30
10	20	0	30
20	10	0	30
30	10	0	30
40	0	20	0
50	10	0	0
60	0	0	0

Filter selection

86. The LC filter on board AC3 and the crystal filters on boards AC4 and AC5 (see Fig.s x and 2x are switched into the signal path in accordance with the bandwidth selected. Filter selection is shown in Table 6

TABLE 6 IF FILTER SELECTION

Selected bandwidth	LC filter (AC3)	Crystal filter (AC4)	Crystal filter (AC5)
3 Hz	10 kHz	3 Hz	100 Hz
10 Hz	10 kHz	10 Hz	100 Hz
30 Hz	10 kHz	30 Hz	300 Hz
100 Hz	30 kHz	[30 Hz]	100 Hz
300 Hz	30 kHz	[30 Hz]	300 Hz
1 kHz	30 kHz	[30 Hz]	1 kHz
3 kHz	30 kHz	[30 Hz]	3 kHz
10 kHz	10 kHz	[30 Hz]	[3 kHz]
30 kHz	30 kHz	[30 Hz]	[3 kHz]
100 kHz	100 kHz	[30 Hz]	[3 kHz]
300 kHz	300 kHz	[30 Hz]	[3 kHz]
1 MHz	2 MHz	[30 Hz]	[3 kHz]

Selections shown in square brackets play no part in filter performance

- BOARD CHECK-OUT PROCEDURES -

AA1a - INPUT ATTENUATOR

Test equipment: Voltmeter

87. Proceed as follows:-

(1) If attenuation is incorrect, check each resistor.

(2) If the fault remains, check the microswitches.

AA2a - INPUT FILTER & MIXER

Test equipment: Voltmeter, oscilloscope, signal generator, spectrum analyzer, active probe, v.s.w.r. bridge.

88. (1) Check the following test point voltages:

Test point location	Voltage (V)	If not suspect
TP1	7 ±0.5	TR1,TR2
TP2	6.5 ±0.5	TR3
TR6 collector	5 ±0.25	TR5,TR6,L7
TR8 collector	5 ±0.25	TR7,TR8,L9
TR10 collector	7 ±0.5	TR10,L13

(2) If the d.c. conditions are correct and the fault is observed below 50 MHz, inject a signal into the input of the analyzer under test to check the input amplifier. Using an oscilloscope, check for a gain of 8 dB between tag 1 and TP3. If not, suspect the electrolytic coupling capacitors etc.

(3) Using a high impedance active probe, check that each stage of the l.o. buffer has 5 dB of gain from 500 to 900 MHz, the mixer has about 7 dB of conversion loss and that TR10 has a few dB of gain (this is not a 50 Ω output). Note that for the intermodulation and spurious emission of the mixer to be adequate, the return loss at the three mixer ports must be better than -15 dB.

Mixer matching

88.1 Check as follows:-

(1) Set a second spectrum analyzer to full span (if necessary with an extender to reach 1.25 GHz) and connect the tracking generator output to a v.s.w.r. bridge input. Connect the bridge sense output to the second analyzer's input socket.

(2) Set the analyzer to 10 dB/div, -10 dBm top-of-screen and store the level in Trace A as a reference.

(3) Connect the coupler test port to the required mixer port and read the level into Trace B. Ensure that the test point connection is made as short as possible (<5 cm). Check that the difference between A and B traces is more than -10 dB from 10 MHz to 900 MHz.

(4) Repeat (3) above for the remaining two ports.

(5) If at this point no fault has been found, it will be necessary to replace mixer X1.

AA3 - 502.6 MHz IF FILTER &
AA3a - 2ND MIXER

Test equipment: Voltmeter oscilloscope, spectrum analyzer

89. If the fault involves R5 overheating, it is likely that a voltage surge has destroyed TR1. Proceed as follows:-

(1) Look for shorts around TR1.

(2) If there is a d.c. voltage drop across R3 replace TR1.

90. Check the following d.c. test point voltages:-

Test point (TP)	Voltage (V)	If not suspect
2	3.5 ±1	TR1
3	13.5 ±0.5	TR1
4	10 ±0.5	TR2
5	10 ±0.5	TR3
6	10 ±0.5	TR4

91. If the d.c. conditions are correct, but the intermodulation performance is not, the most likely fault is low local oscillator drive:-

(1) Check that the level of l.o. being injected onto the board is more than -5 dBm at 550 MHz. Also check L11, broadly tuned to 550 MHz, which might have become damaged. Check TR1.

92. Check the gain and filter operation as follows:-

(1) Connect the tracking generator output of a second analyzer to the INPUT socket of the analyzer under test. Connect the 2382 IF output socket to the input of the second analyzer. Set both analyzers to 47.4 MHz centre frequency, with the 2382 on zero span.

(2) Set the second analyzer to 10 MHz/div and check for a symmetrical display at 47.4 MHz at a bandwidth of 7 MHz.

(3) Check the tuning of C8. If there is no noticeable peak in output level as C8 is tuned, check L5. Check also the voltage drop across L5 and L6, which should be very small (less than 0.02 V).

(4) If C8 cannot peak the response carry out the filter setting up procedure.

AA4 - SAMPLING GATE

Test equipment: Voltmeter, oscilloscope

93. Proceed as follows:

Power supplies

(1) Check that the power supplies are as follows:-

70 V	3.6 mA
14.5 V	73 mA
4.8 V	100 mA
-5.2 V	12 mA
-14.5 V	45.3 mA

Isolating amplifier

(2) Check that the d.c. bias at the junctions of R10,R12,R13 and R14, R16,R17 is at +10 V ±1 V.

Pulse generator & sampling gate

(3) Disconnect SKF.

(4) Connect the +5 V rail to PLF pin 6 and, using an oscilloscope, check the following test points:-

(a) TP3 for a 50 MHz square wave with a low of 0 V and a high of >4 V.

(b) TP4 for a 5 MHz square wave of approx. 18 V p-p.

(c) TP5 for a d.c. level of approx. +2 V with a narrow negative-going pulse.

(d) TP6 for a d.c. level of approx. -2 V with a narrow positive-going pulse.

Note ...

All measurements are limited by oscilloscope rise time.

AA5 - MASTER VCO

Test equipment: Voltmeter, spectrum analyzer & probe, counter, power source.

94. Proceed as follows:-

Power supplies

(1) Check that the +10 V line at TP3 and the -10 V line at TP4 are within ±0.25 V.

(2) Check that the power supplied is as follows:-

+15 V	17 mA
+5 V	87 mA
-5.5 V	6 mA

Isolating amplifiers

(3) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R52,54,55	R56,58,59
R72,74,75	R76,78,79
R85,87,88	R89,91,92

Summing amplifier

(4) Connect PLE contacts 3 and 4 and PLJ to ground.

(5) Check TP1 for a d.c. level between 0 V and +0.5 V.

(6) Check TP2 for approximately 0 V.

Outputs

(7) Check that the output to AA8 is -5 dBm ±1 dB. If not, disconnect the signal path to AA8 and check T2 pin 1 for -3 dBm ±1 dB. If not, check T1 pin 1 for 0 dBm.

(8) Check that the output to AA6 ia +5 dBm ±1 dB. If not, disconnect the signal path to AA6 and check T4 pin 3 for -1 dBm. If not, check T2 pin 3 for -3 dBm. If not, check T1 pin 1 for 0 dBm.

(9) Check that the output to AA4 is +5 dBm ±1 dB. If not disconnect the signal path to AA4 and check T4 pin 1 for -1 dBm. If not, check T2 pin 3 for -3 dBm. If not, check T1 pin 1 for 0 dBm.

AA6 - DIVIDER

Test equipment: Voltmeter

Checking board operation

95. Proceed as follows:-

Power supplies

(1) Check that the power supplied is as follows:-

+15 V	17 mA
+5 V	87 mA
-5.5 V	6 mA

Isolating amplifier

(2) Check that the d.c. bias at the junctions of R5,R7,R8 and R9,R11,R12 is at +10 V ±1 V.

Signal path

(3) Check TP1 for a t.t.l. square wave at 1/64 of the input frequency from AA5. Check PLAK for a similar signal at 1 V p-p.

AA7 - SLAVE VCO

Test equipment: Voltmeter

96. Proceed as follows:-

Power supplies

(1) Check that the +10 V line at TP3 and the -10 V line at TP4 are within ±0.25 V.

(2) Check that the power supplied is as follows:-

+70 V	4.3 mA
+14.5 V	105 mA
-5.2 V	8.2 mA
-14.5 V	19.5 mA

Isolating amplifiers

(3) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R57,59,60	R61,63,64
R70,72,73	R74,76,77

Summing amplifier

(4) Connect PLP contacts 3 and 4 and PLAN to ground.

(5) Check TP1 for a d.c. level between 0 V and 0.5 V.

(6) Check TP2 for approximately 0 V.

Outputs

(7) Check that the output to AA8 is +5 dBm ±1 dB. If not, disconnect the signal path to AA8 and check T4 pin 3 for -1 dBm ±1 dB. If not, check T2 pin 3 for -3 dBm ±1 dB. If not, check T1 pin 1 for 0 dBm.

(8) Check that the output to AA2a is +5 dBm ±1 dB. If not, disconnect the signal path to AA2a and check T4 pin 1 for -1 dBm ±1 dB. If not, check T2 pin 3 for -3 dBm ±1 dB. If not, check T1 pin 1 for 0 dBm.

(9) Check that the output to AE4 is -5 dBm ±1 dB. If not, disconnect the signal path to AE4 and check T2 pin 1 for -3 dBm ±1 dB. If not, check T1 pin 1 for 0 dBm.

AA8 - MASTER/SLAVE PHASE DETECTOR

Test equipment: Oscilloscope, voltmeter

97. Proceed as follows:-

Power supplies

(1) Check that the power supplied is as follows:-

+14.5 V	66 mA
+4.8 V	14 mA
-5.2 V	14 mA
-14.5 V	45 mA

Isolating amplifiers

(2) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R56,58,59	R60,62,63
R68,70,71	R72,74,75

Loop operation

(3) Ground SKN by connecting it to PLAS to break the loop.

(4) Check at TP1 for a signal at >1.5 V p-p. Check for a similar signal but shifted by 90^0 at TP2.

(5) Check at TP3 and TP4 for a signal amplitude of approx. 150 mV p-p to check mixer operation.

(6) Check that D2 is lit and TP6 is at -14 V d.c.

(7) Check PLN for a 20 V p-p triangular wave at approx. 5 Hz.

(8) Reconnect SKN.

AA9 - 2ND LO VCO

Test equipment: Oscilloscope, counter, voltmeter

98. Proceed as follows:-

(1) Check all power lines and the two regulated lines.

(2) If loop fails to lock, check level of 550 MHz signal on AA10 using either a sampling oscilloscope or a spectrum analyzer.

(3) If level on AA10 is correct and R6 is able to tune the oscillator to 550 MHz, then fault is on AA10.

(4) If level on AA10 is correct and R6 is unable to tune the oscillator to 550 MHz, then check d.c. level on AA10, TP6.

(5) If d.c. level on TP6 is greater than ±1 V, then fault is on AA10.

(6) If d.c. level on TP6 is less than ±1 V, then fault is in the oscillator.

(7) Check oscillator by checking volts on TP1 and varactor diodes D1 to D3. If these are correct, check values of C3, C6 and C7.

(8) If any of the 550 MHz outputs are below the stated levels then check back through buffers and power splitters until fault is located.

AA10 - SAMPLING GATE

Test equipment: Oscilloscope, counter, voltmeter

99. Proceed as follows:-

(1) Check the power lines by measuring the supply in accordance with the following:-

Component	Supply Voltage	Current
R1	+15 V	69 mA
R2	-5.5 V	1.3 mA
R41	-15 V	13.6 mA

(2) Check TP2 for 50 MHz at approx. 10 V p-p. If not, check the operation of TR2.

(3) Ground SKAD to PLNP, then adjust AA9, R6 for a 550 MHz output.

(4) Check TP4 for a 2 V p-p sinewave at the difference frequency between the 550 MHz output from AA9 and the 50 MHz input multiplied by 11.

(5) If no signal is found at TP4, then check for +1.5 V at the junction of R11,C11 and for -1.5 V at the junction of R12,C12. If not, check the sampling pulse generator.

(6) If no signal is found at TP4 and +1.5 V and -1.5 V are present, then the 550 MHz amplifier TR1 may be at fault. Check that the d.c. bias at the junction of R6, R7 is 10 V ±1 V.

(7) With SKAD still connected to ground, check the search oscillator by checking for a 3.5 V p-p sinewave at TP6.

(8) Check the correct lock detector by checking at TP3 for a square wave of between 0 V and -14 V as the search goes through the detector window.

(9) Connect PLNB to ground to halt the search oscillator operation and check that TP3 remains at -14 V.

(10) Remove ground connections to SKAD and PLNB.

AA11 - LINE CLEANER

Test equipment: Voltmeter

Checking board operation

100. Proceed as follows:-

(1) Check that the +10 V line at PLL contact 8 and the -10 V line at PLL contact 5 are within stated values ±0.4 V.

(2) Check that the power supplied under no load conditions is as follows:-

+15 V	18 mA
+5 V	62 mA
-5.5 V	56 mA
-15 V	18 mA

(3) Check the line cleaner operating current by measuring the voltages at the following test points:-

TP1	+1 V ±0.2 V
TP2	+2 V ±0.5 V
TP3	-2 V ±0.5 V
TP4	-1 V ±0.2 V

Ripple rejection

(4) Modulate each of the incoming power lines with a 10 mV r.m.s. signal at 1 kHz.

(5) Check that the rejection of the 14.5 V lines is greater than 35 dB.

(6) Check that the rejection of the other power lines is greater than 23 dB.

AB1 - D TO A BOARD

Test equipment: Oscilloscope and probes, voltmeter

101. Proceed as follows:-

Power supplies

(1) Check that TP22 is at 15 V ±0.05 V.

(2) Check that the power supplied is as follows:

Line	Current
+70 V	24 mA
+20 V	630 mA
+15 V	540 mA
+ 5 V	340 mA
-55 V	87 mA
-15 V	185 mA

Sweep gain D to A

(1) Select PRESET and then SWEEP MODE SINGLE ARM.

Enter Self-test mode 4(b) - see para. 50 and select Sweep gain D to A.

Set the Sweep gain D to A value to 200.

Check that AB1 is at 6.3 V ±

(2) Set the Sweep gain D to A value to 190.

Check that AB1 TP3 drops 0.32 V (i.e. 32 mV/bit).

(3) Select SWEEP MODE NORM.

Vary Sweep gain D to A between 170 and 230 to illustrate its effect on the sweep.

(4) Leave the test via PRESET.

Sweep D to A

(1) Select PRESENT and then METER.

Select MARKERS 1 2 MOVE.

Turn MARKERS MOVE anti-clockwise to set meter to minimum frequency.

Check that AB1 TP4 is at 0 V ±0.05 V.

(2) Using I/O port access (see para. 72) WRITE 00000000B to ports 602 and 612.

Check that AB1 TP4 is at 12.5 V ±0.25 V.

Step D to A, sweep integrator and rate limiter

(1) Select PRESET and then 200 kHz/DIV.

Enter Self-test mode 4(b) - see para. 50 - and select Step D to A.

Trigger the oscilloscope (on Ext. Trig) to the falling edge of AD3 TP3.

Check that the waveforms at TP4, TP5, TP6 and TP7 are correct.

(2) Set the Step D to A value to 255.

Check that the step size is 750 mV ±50 mV.

Rotate MARKERS MOVE fully anti-clockwise.

(3) Leave the test via PRESET.

Step attenuator, sweep select, x1x5 amplifier and AB2 remote attenuator.

(1) Select PRESET and then METER.

Set a convenient voltage at TP4 using MARKERS MOVE control.

Check division ratios on resistors R30-37

Switch closed	Selected SPAN/DIV				
IC21(a)	40 Mhz		200 kHz	2 kHz	200 Hz
IC21(b)	20 MHz		100 kHz	1 kHz	100 Hz
IC21(c)	10 MHz	2 MHz	50 kHz	500 Hz	50 Hz
IC21(d)	5 MHz	1 MHz			
IC22(a)			20 kHz		20 Hz
IC22(b)		500 kHz			
IC22(c)			10 kHz		10 Hz
IC22(d)			5 kHz		

(2) Select some of the following spans in order to check the sweep selector, x1x5 amplifier, and rotate attenuation on AB2.

SPAN/DIV	x1x5 amp. state	AB2 atten. state	Sweep select drive to oscillator
40 MHz	x5	÷5	
20 MHz	x5	÷5	
10 MHz	x5	÷5	
5 MHz	x5	÷5	AA5
2 MHz	x1	÷5	
1 MHz	x1	÷5	
500 kHz	x1	÷5	
200 kHz	x1	÷5	
100 kHz	x1	÷5	
50 kHz	x1	÷5	
20 kHz	x1	÷5	
10 kHz	x1	÷5	AB3
5 kHz	x1	÷5	
2 kHz	x1	÷5	
1 kHz	x1	÷5	
500 Hz	x1	÷5	
200 Hz	x1	÷50	
100 Hz	x1	÷50	
50 Hz	x1	÷50	AB2
20 Hz	x1	÷50	
10 Hz	x1	÷50	

Reference voltage generator

(1) Select PRESENT.

Enter Self-test mode 3 - see para. 35.

Select 2ND FUNCT:MARKERS A B SELECT.

Check that AB1 TP15 is at 12.5 V ±100 mV.

(2) Select 2nd FUNCT:MKR2 and using the MARKERS MOVE control set the fine D to A to zero.

Check that AB1 TP15 is at 0 V ±20 mV.

Check that AB1 TP16 is at 0 V ±10 mV.

Check that AB1 TP17 is at 12.5 V ±100 mV.

(3) Select 2nd FUNCT:MKR1 and set the Coarse D to A to zero.

Check that AB1 TP17 is at 0 V ±10 mV.

(4) Select 2nd FUNCT:MKR1 2 MOVE and set the Medium D to A to zero.

Check that AB1 TP16 is at 12.5 V ±100 mV.

(5) Check that the voltage at TP16 changes by the same amount by either changing the Fine D to A by 255 bits or the Medium D to A by 4 bits. This 64 to 1 relationship should also exist between the Medium D to A and the Coarse D to A.

(6) Check that the D to A's are monotonic. (IE increasing codes always produce an increasing/decreasing output voltage.)

Output level D to A Tracking generator

(1) Select PRESET.

Enter Self-test mode 4(b) - see para. 50 - and select TG level D to A.

Check that AB1 TP19 is at 0 V ±20 mV at D to A value zero.

(2) Leave the test via PRESET.

Set IF gain D to A

(1) Select PRESET.

Enter Self-test mode 4(a) - see para. 46.

Check that AB1 TP20 is at 0 V ±20 mV at D to A value zero.

Check that AB1 TP20 is at 10 V ±100 mV at D to A value 255.

(2) Leave the test via PRESET.

Centre freq. adjust D to A (IC1 and 2)

(1) Select PRESET.

Enter Self-test mode 4(a) - see para. 46.

Check that AB1 TP21 is at 1.0 V ±100 mV at D to A value zero.

Check that AB1 TP21 is at 11.0 V ±200 mV at D to A value 255.

(2) Leave the test via PRESET.

Latches

(1) Select PRESET.

Enter I/O port access, - see para. 73 - write a bit pattern into any specified port and check that the corresponding latch is set correctly.

AB2 - INTERPOLATION OSCILLATOR

Test equipment: Oscilloscope & probe, frequency meter

102. Proceed, with the board in place, as follows:-

(1) Disconnect PLN.

(2) Check that the regulator is operating correctly by measuring the voltage on TP6 for -11.8 V ±10%.

(3) Monitor the waveforms at TP3 and TP5 and check for 2 V ±0.5 V p-p and frequency 29 MHz ±2 MHz.

(4) Replace PLN.

AB3 - MASTER HF VCO

Test equipment: Oscilloscope & probe, frequency meter

103. Proceed, with the board in place, as follows:-

(1) Disconnect PLX and PLAL.

(2) Check that the regulator is operating correctly by measuring the voltage on TP6 for -11.8 V ±10%.

(3) Connect +6 V to PLX 3 and ground PLX 5.

(4) Monitor the waveforms at TP3, PLZ, PLV and check for 2 V ±0.5 V p-p and frequency 31 MHz ±2 MHz.

(5) Replace PLX and PLAL.

AB4 - SAMPLING GATE

Test equipment: Oscilloscope & probe and generator

104. Proceed, with the board in place, as follows:-

Sampling pulses

(1) Select a sweep span of 5 MHz to take PLAM 5 low to enable phase lock operation.

(2) Check that IC4, pin 9 is below -2 V, if not then IC3 or IC4 is faulty.

(3) Check on TP11 for a 100 kHz signal with a 1:4 mark/space ratio at e.c.l. levels.

(4) Check TP4 for a 50 ns, 1 V positive pulse corresponding to the rising edge of the waveform at TP11, and for a similar, negative pulse at the trailing edge.

(5) Check that the pulse at TP2 is negative-going, and that the pulse at TP3 is positive-going.

(6) Check for negative and positive pulses at TP6 and TP7 respectively.

(7) Select a sweep span of 2 MHz to take PLAM 5 high to disable phase lock operation.

(8) Check that the pulses are no longer present on the test points, and that TP9 is at 0 V.

Signal path

(9) Reselect a sweep span of 5 MHz to take PLAM 5 low.

(10) Disconnect PLAL. Input 32.004 MHz at 2 V p-p to SKY.

(11) Check that the output of the first gate at TP5 is a stepped approximation of a sinewave of 1.5 V p-p and 4 kHz. The waveform between sampling pulses should be flat, with no noticeable droop. Faults here are likely to be caused by diodes.

(12) Check at TP8 for a similar waveform to that in (11) but of 1.2 V p-p.

(13) Check at TP9 for a smoothed sinusoid of 0.3 V p-p.

(14) Reconnect PLAL and SKY.

AB5 - SLAVE VCO

Test equipment: Oscilloscope & probe, frequency meter, d.c. source

105. Proceed, with the board in place, as follows:-

(1) Disconnect PLAE and PLAK.

(2) Connect 6 V to PLAK and ground PLAE 3,4.

(3) Monitor the waveform at TP1 and check for 2 V ± 0.5 V p-p and frequency 32 MHz ±2 MHz.

(4) Replace PLAE and PLAK.

AB6 - PHASE DETECTOR

Test equipment: Oscilloscope & probe, frequency meter

106. Proceed with the board in place as follows:-

(1) Select /DIV and reference frequency 10.005 MHz.

(2) Make a note of the approx. 32 MHz input frequency (f) on SKR.

(3) Check at IC1 pin 11 for f/16.

(4) Check on TP2 and IC4 pins 3,6 and 11 that the four phases of the output signal from IC3 are at t.t.l. levels and at f/32.

(5) Check at TP3 for a signal of approximately 1 MHz at 300 mV p-p to check mixer operation.

(6) Ground TP7 to break the loop and check at TP6 for a triangular waveform of 0.5 V p-p.

AB7 - OSCILLATOR SELECT

Test equipment: Oscilloscope & probe

107. Proceed with the board in place as follows:-

(1) Check for t.t.l. levels at TP1,2 and 3.

(2) Ground PLAA contacts 4,5 and 6 in turn and check that the signals from AA6, AB2 and AB3 are respectively routed to TP4 as shown below:-

PLAA contacts			TP4
4	5	6	signal
H	H	H	none
L	H	H	AA6 input
H	L	H	AB2 input
H	H	L	AB3 input

AB8 - OVERLOAD DETECTOR

Test equipment: DC source, oscilloscope, pulse generator

Control signals

108. Input/output control signals are as follows:-

(1) Output solenoid controls:-

TTL; high to energize

(2) Input logic CHANGE:-

TTL; falling edge initiates a solenoid voltage pulse

(3) Input logic CLEAR:-

TTL; when asserted low -

(a) Returns logic from tripped to normal state provided that no overload is detected.

(b) Prevents transition from normal to tripped state.

Checking board operation

108/1 Board operation may be checked as follows:-

(1) Connect a Schottky diode detector circuit like that on board AA1a to PLAU 1,4 and 5, a 600 Ω load on each solenoid output (PLAT 1,2,3,8,9,10, common line PLAT 7) and a suitable latch or switches to the control inputs (PLAS 1-4, 7-10).

(2) Connect a d.c. source to the positive detector diode and check that the overload detector output at TP1 goes low when the input voltage rises through 5 V and high again when it falls through about 3.5 V. Check the negative detector similarly for switching at -5 V and -3.5 V.

(3) Check that in the normal state, i.e. no overload, TP2 is t.t.l. high and goes low when TP1 does, provided OVERLOAD CLEAR (TP4) is high. Check that INPUT OVERLOAD (TP3) is the inverse of TP2.

(4) Check that application and removal of an overload leaves the circuit in the tripped state (TP2 low) and that taking OVERLOAD CLEAR low restores the normal state only if TP1 is high.

(5) Check that applying a t.t.l. high level to any of PLAS 1-4, 7-10 causes the corresponding solenoid output to be pulled to ground, and that when PLAS 3 and 8 and TP2 are all high, TP7 goes from about 0 V to 5 V. Check that TR2 and TR3 are always off in the tripped state.

(6) Connect a pulse generator set to produce about 5 t.t.l. low pulses per second to TP5 (CHANGE). Trigger an oscilloscope from the pulses and check that each falling edge causes the voltage at PLAT 4 to fall from -9.5 V to -20 V for about 30 ms.

(7) The board will fail many of these tests if the 1.5 V reference voltage produced at the junction of R18 and R19 (TP6) is in error by more than about ±1 V. This may be caused by a short circuit comparator input in IC6 or IC7.

AC1 - 50 MHz CRYSTAL OSCILLATOR

Test equipment: Oscilloscope & probe, counter

109. Proceed as follows:-

(1) If loop fails to lock, connect oscilloscope via probe to AC6, TP4 and continue as follows:-

(a) If low frequency error signal of ±6 V is not present check back through the phase detector and the divider chains until fault located.

(b) If error signal present, check frequency of 10 MHz is within 1 p.p.m. and frequency of 50 MHz is within 10 p.p.m.

(2) If no 50 MHz signal at any of the AC1 outputs, check back through the buffers with the oscilloscope probe.

AC2 - 47.4 MHz IF AMP

Test equipment: Oscilloscope and probe, signal generator

110. After checking the power supplies proceed as follows:-

(1) If the signal is being displayed, but the 10 dB i.f. gain steps are not producing 10 dB shifts in the screen level go to para. 114.

(2) If there is no output from the rear panel i.f. output socket go to para. 113.

(3) If the overall level is too low, carry out para. 112 and if no fault is found then continue this sequence.

111. After checking AC1, PLM to ensure that the l.o. signal is present, check TP2 for a 50 MHz sinewave. If not check TR3.

112. Check the 47.4 MHz signal as follows:-

(1) Set the 2382 to 10 MHz centre frequency, zero span and 10 dB input attenuation.

(2) Connect the STD 10 MHz OUTPUT socket to the INPUT socket (or connect a 47.4 MHz, 0 dBm signal to PLA).

(3) Connect an oscilloscope via a probe to TP3 and check for a similar 47.4 MHz, 0 dBm signal. If not, check TR5 and that the filter/notch are set up properly.

113. Connect the oscilloscope and probe to TP5 and check for a 2.6 MHz signal about 6 dB higher than the input 47.4 MHz signal. If not, the fault lies in the mixer TR5-8 or in TR11.

114. Check attenuator operation as follows:-

(1) Set r.f. attenuation to 50 dB. Set top of screen reference level to -20 dBm and adjust span control to obtain a resolution bandwidth of >30 kHz.

(2) Input a signal and display near the top of screen.

(3) Check that TP10, 11 and 12 are all high (see Table 7 entries against 60 dB i.f. gain).

(4) Increment r.f. attenuation in 10 dB steps and check that the logic levels on TP10,11 and 12 change in accordance with Table 7.

(5) If the logic levels (H = +3.5 V, L = 0 V) are incorrect, check back to AD3.

(6) If the logic levels are correct but the displayed level changes, then check that the drive voltages (H>10 V, L<-10 V) of level shifters IC2,4 agree with Table 7.

115. Check that the d.c. on TP5,6 and 7 is -0.7 V. If not, there is a fault with TR11 or TR12.

116. Check that the signal level at TP7 is 30 dB lower than that at TP8. If not, amplifier TR15,16 is faulty. If so go back to the beginning or suspect another board.

117. Check that i.f. output amplifier TR2 has 0 dB gain to 47.4 MHz signals when terminated with 50 Ω.

TABLE 7 IF ATTENUATOR SELECTION LOGIC -AC2

IF gain (dB)	Test point			IC2 pin		IC4 pin			
	10	11	12	7	1	8	14	1	7
+60	H	H	H	H	L	H	L	H	L
+50	L	H	H	H	L	H	L	[L	H]
+40	H	L	H	H	L	[L	H]	H	L
+30	H	H	L	[L	H]	H	L	H	L

Ringed levels are transitory

AC3 - 2.6 MHz LC FILTER

Test equipment: Oscilloscope & probe, signal generator

118. This is carried out with the board in place in the instrument. Note that there is a relationship between the PLH numbers and the TP numbers: add 10 to the PLH number to obtain the relevant TP number. A connection made to any of these test points can be used to set a required logic state.

(1) If the board works properly only when the instrument is set to bandwidths other than 10 kHz, 30 kHz, 100 kHz, 300 kHz or 1 MHz, start at (7).

(2) If the autocal tune function is not working, check that TP19 goes to about +6 V for system i.f. bandwidths of <10 kHz independent of autocal volts; and that TP19 tracks the autocal volts for i.f's >3 kHz. If not suspect TR17.

(3) With power connected to PLH, check that the t.t.l. inputs and the level shifter outputs conform to those given below:-

PLH	Test point	Level shifter	Approx. level shifter output for t.t.l. input "low"	"high"
3	TP13	IC8a	+12 V	-12 V
4	TP14	IC8c	+12 V	-12 V
5	TP15	IC10a	-12 V	+12 V
5	TP15	IC10b	+12 V	-12 V
10	TP20	IC2a	-12 V	+12 V
10	TP20	IC2b	+12 V	-12 V
11	TP21	IC8d	+12 V	-12 V
12	TP22	IC8b	+12 V	-12 V

(4) Connect a 2.6 MHz, 1 V p-p signal to PLE and connect an oscilloscope probe to TP1. Toggling PLH 10 should produce either 1 V p-p or 30 dB down on 1 V i.e. 31.6 mV p-p.

(a) If true, set PLH 10 low and go to (5).

(b) If false, fault is in IC1 (or possibly TR1).

(5) Connect probe to TP2 and check for 1 V p-p sinewave.

(a) If true, check that a control voltage of between 0 and 10 V on PLH 6 varies the level at TP2 by +2 to -10 dB.

(i) If true, go to (6).

(ii) If false, fault is in D1, D2.

(b) If false, fault is in gain block TR1, TR2.

(6) Connect probe in turn to TPs 3,4,5,6,7 and 8 and check for a similar amplitude sinewave.

(a) If true, go to (7).

(b) If false, fault in region of test point.

(7) Set PLH 5 low and check that the signal is present on TP9, and that there is no signal on PLJ. Then set PLH high and check that the situation is reversed, i.e. signal on PLJ and none on TP9.

(a) If true, fault is in TR17, TR18.

(b) If false, fault is in IC9.

AC4 - 100 kHz IF XTAL FILTER

Test equipment: Oscilloscope & probe

119. Proceed with the board in place as follows:-

(1) Connect the STD 10 MHz OUTPUT socket to the INPUT socket.

(2) Take PLX 9 low and check for a broadband, low-loss connection to i.f. signals between the input at SKJ and the output at PLW.

(a) If true, take PLX 9 high - or allow it to float high - and proceed to (3).

(b) If false, check that IC11a output is less than -10 V and IC11b output is more than +12 V.

(i) If true, check IC1,IC7 and paths from IC11 to IC1 and IC7.

(ii) If false, check IC11 and path from PLX 9 to IC11.

(3) Check for presence of t.t.l. square wave on the gates of IC1a,b and IC7a,b.

(a) If true, proceed to (4).

(b) If false, check IC2 etc.

(4) Connect probe to TP1 and check for a symmetrical, chopped sinewave.

(a) If true, proceed to (5).

(b) If false, check d.c. conditions in amplifier TR1,6,7.

(i) If no symmetrical chopped sinewave is present, check T1, IC1a, IC1b.

(5) Set PLX 7 and PLX 8 high and connect probe to TP4,6,8,10,11 in turn and check for a similar amplitude 100 kHz sinewave.

(a) If true, fault in IC7.

(b) If false, check that the d.c. component at the test point in question is about -0.7 V.

(i) If true, check the feed forward transistor (TR8,10,14,16,20) etc.

(ii) If false check the emitter follower (TR7,9,13,15,19,21).

Note ...

Further faults may be exposed by the calibration procedure.

AC5 - 2.6 MHz XTAL FILTERS

Test equipment: Signal generator, oscilloscope & probe

120. Proceed with the board in place as follows:-

(1) Select 3 kHz bandwidth (PLL 2,3,9 are high) and check that the outputs of IC1a,b and c are all greater than +10 V.

(a) If true, proceed to (2).

(b) If false, check for shorts on IC1 outputs and for 1.2 V at the junction of R23,R24.

(2) Select each of the bandwidths in turn, either using the front panel or by grounding TP13,14,15 as required, and verify that the respective diode lines go to less than -10 V.

(a) If true, check for each diode bandwidth switch, that when selected it drops 0.7 V and when not it drops greater than 10 V.

(i) If true, apply a 2.6 MHz signal at about 100 mV p-p to SKW and proceed to (3).

(ii) If false, check the diode involved, and possibly the inductor (L2 to L6).

(b) If false, check the load resistors etc. associated with the diode in question.

(3) Connect oscilloscope probe to TP2 and check for a 2.6 MHz sinewave centred at about +4.3 V and about 250 mV p-p.

(a) If true, go through the bandwidths and check that R7,R11 control the gain when selected.

(i) If true, proceed to (4).

(ii) If false, check TR2,TR3.

(b) If false, check d.c. conditions of TR1,TR4,TR5.

(4) Connect probe to TP4 and check for approx. 250 mV p-p 2.6 MHz sinewave. Transfer to TPs 6 and 8 and check for approx. 625 mV p-p 2.6 MHz sinewave. Transfer to TPs 10 and 11 and check for approx. 1.55 V p-p 2.6 MHz sinewave.

(a) If true, the problem occurs after the test point probed.

(b) If false, check the preceding stage.

Note ...

Further faults may be exposed by the calibration procedure.

AC6 - PHASE DETECTOR

Test equipment: None

121. The procedures for checking the p.l.l. operation and for fault finding are included in those for AC1.

AD1 - LOG AMP

Test equipment: Oscilloscope & probe, step attenuator

122. Proceed with the board in place as follows:-

Gain stages

(1) Connect TRACKING GENERATOR socket via step attenuator to INPUT socket.

(2) Select LOG.

(3) With all attenuation out, display a level at top of screen.

(4) Increase attenuation in steps to 80 dB down and check that the G outputs go high and low in the following sequence:

	SIGNAL LEVEL DECREASING ⟶							
G1	H	H	L	L	L	L	L	L
G2	H	H	H	H	L	L	L	L
G3	H	H	H	H	H	H	L	L
G4	H	L	H	L	H	L	H	L

Note that feedforward will influence the situation; if one latch has jammed high it will lock the following 25.6 dB stages high. If this test is successful then the fault probably lies in the final detector.

(5) If a particular gain stage is suspected, check that it has the correct gain, then check the attenuator. The gates of level shifters IC2c and 2d should be at +15 V for the off state and -5 V for the on state. The detector outputs are available on test points TP3,6,9,12. In the absence of signals, the TPs should be at about 0.7 V. The comparator should change state for levels at this point of about 0 V.

(6) Check for video trigger output. If not, check TR39,40,41.

Final detector

(7) With a normal input signal level, the voltage swing at the input to the detector (TP12) should be between 4 V and 0.7 V p-p.

(a) If true, proceed to (8).

(b) If false, suspect the 12.8 dB gain block and attenuator.

(8) Connect oscilloscope probe to TP13. Check that this carries a signal which is sinusoidal at the top and bottom of its swing and slews very rapidly across the zero point.

(a) If true, proceed to (9).

(b) If false, check the d.c. conditions of TR36,37,38 and also D24,25.

(9) Probe through to IC14,15 to check continuity; there should be no change in d.c. level from L1,L2 to the outputs of ICs 14b and 14a respectively. Also, check that the two inputs to IC15 are at the same d.c. voltage.

(10) Check that TP14 voltage is the same as the level at PLU.

(11) Check for presence of i.f. counter output. If not, check IC13.

AD2 - LOG AMP INTERFACE

Test equipment: Oscilloscope & probes, a.m. signal generator

Checking board operation

123. Proceed as follows:

Power supplies

(1) Check the power supplied is as follows:

LINE VOLTAGE	CURRENT
+15	23 mA
+5	860 mA
-15	45 mA

124. The board divides into three different sections - data conversions, triggering and sweep handling - which are dealt with separately.

Data conversions (Circuit diagram : Chap. 7, Fig. 31)

(1) Select PRESET

REF FREQ = 10 MHz
REV LEV = 10 dBm
SPAN/DIV = 200 Hz
METER

(2) Trigger oscilloscope to TP3 and check waveforms shown in Fig. 31.

(3) Remove PLG (Sampled data), select SWEEP MODE START to refresh the display and reveal the switching points of G1 to G4. Using the MARKERS MOVE control set the meter on each of the different levels to confirm binary conversion is taking place and the IC17 and IC23 are functioning correctly. Refer to AD2 description for conversion data.

(4) Replace PLG and select AUTO RF ATTEN.

(5) Monitor IC55(d) pin 6 to see active high 1 µs pulse. Overload the 12 bit A-D by selecting ↓ REF LEVEL to make the pulse at IC55 pin 6 2 µs wide. This change in pulse width forces the A-D outputs, A0-A10 high which is then latched into the Piso´s on the rising edge of SEQUENCE OND.

In this forced condition the outputs of IC14 and 15 are fixed which make it possible to check the digital summer. The data on the outputs of the summer must be stored on the rising edge of SEQUENCE OND.

(6) Select RF ATTEN AUTO, VOLTS/DIV and a sensible sensitivity (5 mV/div) to check the LOG LAW/LIN look-up table. In VOLTS/DIV IC´s 14 and 15 are programmed such that D0 to D10 = A0 to A10. These conditions must be true on the rising edge of TP3 and hold for 200 ns. Rotation of the MARKERS MOVE control sets the values A0 to A10.

Triggering (Circuit diagram : Chap. 7, Fig. 32)

(1) Check the waveforms in Fig. 32 to test the analogue sections of the trigger circuit.

(2) Check the trigger mode latch using the I/O port access diagnostics - see para. 77.

(3) Refer to AD2 board description, triggering section, for IC2 logic selection.

Sweep handling

(1) It is likely that a fault on either Fig. 33 or 34 of the circuit diagrams will result in the instrument looking up and and refusing to sweep. If this is the case power up into diagnostics and increase the delay to allow sufficient time to perform the following:

Select PRESET

SWEEP TIME = 10 s/DIV
SWEEP MODE SINGLE ARM
STORE 1

(2) Power down and up and check that the following conditions exist.

LOW		HIGH	
IC30(a)	pin 5	IC36	pin 2
IC31(b)	pin 9	IC36	pin 5
IC31(a)	pin 6	IC36	pin 15
IC54(b)	pin 5		
IC32(b)	pin 9		
IC46(b)	pin 9		
IC36	pin 9		

(3) Trigger pulses on IC54 pin 1. Select SWEEP MODE SINGLE ARM and check that IC36 pin 2 goes low. Failure to go too low may be due to faulty decoding on AD3 or a faulty latch IC36.

(4) Check the decoding and the latch by using the I/O port access diagnostics - see para. 77. If IC36 is functioning correctly it may be that the 2380 is refusing to grant permission to sweep. Permission to sweep is granted by sending ´KS CR LF´ from the 2380 to the 2382 after each press of the SINGLE ARM key which it self sends ´KS CR LF´ to the 2380. These messages appear on Rx and Tx of AD3 IC11 in ASCII format. The Hex-ASCII format of this message is as follows:-

´K´	4BH
´S´	53H
´CR´	ODH
´LF´	OAH

Absence of a message on the Tx line implies a lower unit fault whereas no reply on the Rx line implies an upper unit fault.

(5) IC36 pin 2, when taken low arms the data conversion sequence which is programmed to last for 100 s. During this period check that the trigger pulse clocked its way through IC30(a), IC31(b) causing a sampling period clock which after changing IC40(a) generated a low on IC56(b) which started the Log amp measurement cycle sequence generator. Check the 10 µs clock on TP3 is divided in IC47 counters 3 and 4 to give 20 ms and 200 ms clocks at their respective outputs.

After 100 s IC47 counter 4 output goes low for 200 ms and generates an end of sweep sequence on its rising edge. Check that this rising edge clocks IC32(b) which feeds back to the trigger controls on sheet 3 and sets the sweep start conditions which were checked immediately after power up.

A faulty sampling interval programmable counter or sampling incremental delay generator may have stopped the sweep handling but it is more likely to cause problems on zero span time bases which are faster than 10 ms/div. Check the waveforms in Figs. 33 and 34 using the division ratio information available in the AD2 board description.

AD3 - MICROPROCESSOR BOARD

Test equipment: Oscilloscope and probes.

125. This board can be divided into two areas. One area which can be referred to as the microprocessor, includes all the hardware which enables the decoding and running of a program which is stored in memory. This hardware is shown on circuit diagrams Figs. 36,37 and 38 with the exception of IC4,5,11,12 and 13. The only other requirements is that the 5 V power supply is available and IC32 pin 1 is clocked at 5 MHz.

126. The other area includes the hardware which allows the processor to communicate with the operator and Display Unit, using the UART(IC11) and INTERRUPT CONTROLLERS (IC12 and IC13). It also includes a frequency counter, various dividers for setting up interrupt timing intervals and latches for programming fixed conditions.

Checking board operation

(1) Disconnect one end of the rear panel data lead and power the instrument up. If the front panel l.e.d´s are flashing at 0.5 Hz rate it can be assumed that the processor is functioning as well as the interrupt controllers which govern the flash rate.

(2) If the l.e.d´s flash then proceed as follows otherwise go to 20 bit frequency counter check - para. 132.

Power supply

127. Check the power supplied is as follows:

LINE	CURRENT
5 V	1.2 A

(5 V fuse may have blown on AR2)

128. Check that the 10 MHz t.t.l. clock on IC8 pin 1 is divided down to 2 MHz on IC8 pin 8 and 5 MHz on IC8 pin 12. Check that IC10 pin 11 has a 150.625 kHz clock (6.4 µs) and IC32 pin 37 has a 2.5 MHz clock which is derived from its 5 MHz clock on pin 1.

129. Check that IC1 pin 19 is pulsed active low at approximately 200 µs repetitive rate.

130. If a pulse is present on IC1 pin 19 the microprocessor system is running but failing to flash the l.e.d´s. This may be due to a front panel fault, i.e. missing power supply or a faulty CLK TIK INTERRUPT. Check for a 10 ms clock on IC30 pin 7 and a coincident interrupt on IC12 pin 12 (active high pulse). This interrupt should pulse the master which in turn should pulse IC32 pin 10 which should reply with an interrupt acknowledge on IC32 pin 11 which is three active low 1 µs pulses which are separated by approximately 2 µs each. If IC12 pin 17 is permanently high the slave will have interrupted the master but master will not have interrupted the processor unless its pin 17 is high. A reply from the processor clears both these requests.

131. If the pulse is not present on IC1 pin 19 then the processor has crashed. This may be due to a faulty quiet data bus which is used during the flash l.e.d. routines. To eliminate this possibility power down and remove plugs PLN,PLK,PLH and PLT. Connect PLT pin 8 to AD2 PLD pin 8 to maintain the 10 MHz drive and power up again. If the processor is now running replace the leads one by one and trace the fault.

20 bit frequency counter

132. With the rear panel data lead connected power up into diagnostics and select 2nd FUNCT:MKR1 SETS REF LEVEL, and 2nd FUNCT:MKR1 SETS INC FREQ. Connect PLFT pins 2 and 3 and select MKR1, MARKERS 1 2 MOVE and MKR2 checking that the following conditions are true.

			TP active high period
OSC 0	=	640 MHz ±8.192 kHz	7.8125 ms
OSC 1	=	10 MHz ±128 Hz	7.8125 ms
OSC 2	=	10 MHz ±32 Hz	31.25 ms

Exit via 2nd FUNCT:MKR1 SETS INC FREQ.

Latches

133. Check the latches using the I/O port access diagnostics - see para. 77.

Freq count and linearizor interrupts

134. Set the conditions shown for Figs. 35 and 36 and check the resulting wavefroms.

AD4 - 10 MHZ CALIBRATOR

Test equipment: Oscilloscope, spectrum analyzer

135. Internal and external standard generation is checked with the board installed in the instrument as follows:-

(1) Check that the TCXO output at TP2 is roughly sinusoidal with frequency 10 MHz and amplitude at least 400 mV p-p.

(2) Operate R2 over its full range and check that a total frequency shift of at least 100 Hz is produced. Operate the back panel adjuster and check for a similar frequency shift.

(3) Apply a 5 MHz source to the external standard input and check at TP3 that increasing this from zero level causes the external standard detector to trigger at a level less than 50 mV p-p: on triggering, TP3 should fall from about 4 V to 0 V and the signal at TP4 should change in frequency from 10 MHz to 5 MHz. Repeat for external standard frequencies of 1 MHz, 2 MHz and 10 MHz.

(4) With SWITCH CONTROL (TP5) low check that the output at TP9 is sinusoidal with amplitude variable by R25 through 200 mV p-p (-10 dBm).

(5) The 10 MHz standard output at TP8 should be roughly square with rise/fall times of about 4 ns. Check that operation of R22 will vary its amplitude through 160 mV p-p (-10 dBm).

(6) Set SWITCH CONTROL high (5 V) and check that TP6 and TP7 go to about -13 V and +13 V respectively. Check that this polarity reverses when SWITCH CONTROL is taken to 0 V.

(7) Fit the cover that screens AD1 and AD4. Using another analyzer set to -40 dBm top-of-screen, check that when SWITCH CONTROL is high the output at PLAC is below the following levels:-

HARMONIC No.	LEAKAGE (-dBm)
1	100
2-3	110
4-11	120
12-20	125
21-40	130

(8) If the frequency of the TCXO cannot be adjusted through 10 MHz, check that operation of R2 changes the voltage at TP1 from 0 V to about 12 V; if it does, then suspect varactor D1 or the oscillator module itself.

(9) If the external standard detector fails to trigger at the correct level, first check that the signal at TP10 is switching between about 0 V and 4 V; if not, suspect IC1. Otherwise, check that a steady voltage of at least 1.9 V is present at TP11; if not, suspect IC2 or possibly D2 or D3.

(10) Complete failure of the output switch may be caused by a fault in IC3, while inadequate isolation can be caused by a failure of one or more diodes or an open circuit at decoupling capacitor C16.

AE1 - 47.4 MHz CRYSTAL OSCILLATOR

Test equipment: Oscilloscope & probe

136. Proceed as follows:-

(1) If after setting up the p.l.l. there is no 47.4 MHz signal on TP9, check the oscillator. TP8 should be between 6 and 10 V.

(2) If the oscillator fails to lock, check the output from the sampling gate. TP4 should be 1 V p-p, TP7 should be 4 V p-p about +7.5 V, with frequency <1 kHz. Check that the cathode of D2 is at +1.3 V, the anode of D4 is at -1.3 V and the anode of D3 is at 0 V for correct operation. If any of these is incorrect, check the diodes and then the pulse generator.

(3) If there is no signal at PLF, check the gain-controlled amplifier. TP11 should be between -2 V (-19 dBm) and -11 V (-1 dBm).

AE2 - BUFFER

Test equipment: Voltmeter, spectrum analyzer

137. Proceed as follows:-

(1) Check that the power supplied is as follows:-

+15 V	17 mA
-5.5 V	3.4 mA

(2) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R2,R4,R5	R6,R8,R9

(3) Check the a.c. operation from the +2 dBm input to the -8 dBm output.

AE3a - NARROW BAND MIXER/BUFFER

Test equipment: Voltmeter & spectrum analyzer

138. Proceed as follows:-

(1) Check that the power supplied is as follows:-

+15 V	41 mA
-5.5 V	3 mA

(2) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R2,R4,R5	R6,R8,R9

(3) Check that TR3 gate bias is 2 V ±0.25 V on both gates.

(4) Check the mixer output at tag 1 for a 502.6 MHz signal at -9 dBm.

AE4 - TG BUFFER

Test equipment: Voltmeter, spectrum analyzer

139. Proceed as follows:-

(1) Check that the power supplied is as follows:-

+15 V	17 mA
-5.5 V	3.4 mA

(2) Check that the d.c. bias is 10 V ±1 V at the junctions of the following:-

R2,R4,R5	R6,R8,R9

(3) Check the a.c. operation from the -10 dBm input to the 0 dBm output.

AE5a - WIDEBAND MIXER BUFFER

Test equipment: Items, Multimeter

Checking board operation

140. Proceed as follows:-

(1) Check that the power supplied is as follows:-

+15 V	122 mA
-5.5 V	5 mA

(2) Check that the d.c. low is 10 V ±1 V at the junctions of the following:-

R2,R4,R5 R6,R8,L3
R20,R22,R23

(3) Check that the d.c. bias is 5 V ±0.25 V at the junction of the following:-

R13,R14,L5

AE6 - AMPLIFIER LEVELLER

Test equipment: Oscilloscope & probe, power meter, power source

LF response check

141. To trace levelling faults, it will be found convenient to break the loop by connecting AE1, PLE to a -2 to -5 V d.c. power supply. Nominal output level can then be varied between -20 dBm and -10 dBm.

(1) If the output level is incorrect in both the TG and CAL modes:

(a) Set the power source to -5 V and trace signal levels in AE1,AE3,AE5,AE6 and AE7 corresponding to -10 dBm nominal output level.

(b) Check the operation of the 21 dB amplifier in AE6.

(c) Check the operation of the output switches in AE6 and AE7.

(2) If not levelling in both the TG and CAL modes:

(a) Check the logic and operation of AE6 sampling gates and sampling amplifier.

(3) If not levelling in TG mode only:

(a) Check the TG output switch, TG levelling detector, TP3 (see under 'Test points' below), TG LEVEL CONTROL volts, TG levelling comparator and TG sampling gates.

(4) If not levelling in CAL mode only:

(a) On AE6 and AE7: Check CAL output switches, CAL levelling detector, TP10 (see under ´Test points´ below), CAL levelling comparator and CAL sampling gates.

(5) If not levelling at high frequencies:

(a) Trace signal levels from AE1 through to AE7 corresponding to -10 dBm nominal output level.

(b) On AE6 check the frequency conscious switch, TP17, TP19 (see under ´Test points´ below) and detectors.

(6) If not levelling at low frequencies:

(a) Check 21 dB amplifier, TP16,TP17,TP19,TP2,TP3,TP10 (see under ´Test points´ below), and sampling gate logic and operation.

(7) If low frequency distortion present:

(a) Check 21 dB amplifier, TP16,TP17,TP19,TP2 (see under ´Test points´ below), and sampling gate logic and operation.

Test points

142. As an aid to fault finding, the signals present at the various test points are summarized below:-

TP2 - Detector bias: Mean voltage +5 V for signal frequency >1 kHz, varying linearly down to +0.5 V at 100 Hz.

TP3 - TG detector output: Voltage offset (TG off) within ±10 mV. Allowing for offset, output varies from -25 mV to -150 mV approx. as the TG output level varies from -20.5 dBm to -9.5 dBm.

TP5 - Gain control volts: Varies -2 to -5 V approx. as TG output level varies -20.5 dBm to -9.5 dBm. -1.4 V approx. with TG off.

TP7 - Phase shift waveform: Sawtooth with positive slope +1.67 V/ms nominal, negative slope -3.34 V/ms nominal and base voltage -40 mV approx. Amplitude 8 V approx. at 100 Hz decreasing to 80 mV approx. at 10 kHz.

TP10 - CAL detector output: Voltage offset (AE7 tag 1 short-circuited to ground) within ±10 mV. Allowing for offset, output is -145 mV approx.

TP16 - Squarer output: TTL square wave at signal frequencies up to 5 MHz. At 100 Hz, mark/space ratio within 0.75:1 to 1.3:1.

TP17 - Detector bias pulse: TTL 1 ms positive pulse per cycle for signal <1 kHz. +5 V for signal >1 kHz.

TP19 - Sampling pulse: TTL 20 µs negative pulse per cycle for signal <50 kHz, 90^0 phase shifted w.r.t. TP16 waveform. 0 V for signal >50 kHz.

AE7 - SWITCH

Test equipment: None

143. The procedures for checking the operation of this board and for fault finding, are included in those for AE6.

AR2 - POWER SUPPLY INTERFACE

Test equipment: Voltmeter

144. Proceed as follows:-

(1) Check that the power supplied under no load conditions is as follows:-

+15 V	10 mA
+5 V	80 mA
-5.5 V	4 mA
-15 V	8 mA

(2) Check for the following voltages, preferably at full load, at the specified test points:

TP1	-5 V ±0.05 V
TP2	+5 V ±0.1 V
TP3	-15 V ±0.05 V
TP4	+15 V ±0.05 V
TP5	0 V ±1 V at 25^{0}C
TP6	0 V ±0.25 V at 25^{0}C
FS1	+5.15 V ±0.15 V

Chapter 5-3, Annex A

FAULT DIAGNOSIS
- SYNTHESIZER FAULT LOCATION -

CONTENTS

Para.
1 Introduction
6 UHF synthesizer faults
Symptoms
7 2nd local oscillator faults
Symptoms
8 HF synthesizer faults
Symptoms

- Fault location charts -

Fig. Page
1 UHF master slave phase lock 4
2 No signal displayed 6
3 UHF master oscillator failing to lock 7
4 2nd local oscillator 9
5 HF synthesizer 12

INTRODUCTION

1. The synthesizer is a major sub-system of the analyzer which comprises, for fault location purposes, a u.h.f. synthesizer, a 2nd local oscillator and an h.f. synthesizer. A set of fault location procedures is included for each of these sections. This is preceded by information on the master oscillator system and diagnostic routines which may help to localize the fault.

2. Since failure to set an oscillator can be the result of many fault conditions it is an advantage if the frequency setting procedure is understood. This procedure is iterative and involves the boards AA4,AA5,AA6,AB1,AB2,AB3, AB4,AB7 and AD3. The three master oscillators, AA5,AB2 and AB3, receive analogue drive signals from the analogue control board AB1 which in turn receives commands from the micro-processor board AD3. The frequency of any of the master oscillators is measured on AD3 by selecting the required oscillator output from AB7. The frequency of AA5 is too high to count directly so it is divided by 64 on AA6 before reaching AB7. The other two boards, AA4 and AB4, are involved when phase locking either AA5 or AB3.

3. At the start of the procedure the Ref and Sweep D to A drives are switched through from AB1 to the oscillator which is about to be shifted in frequency. The Sweep D to A is set to zero and a voltage is selected by the Ref D to A's which corresponds to the required frequency. The resulting frequency is switched through AB7 and measured on AD3 while TP2 is high. The

error in frequency is calculated, the necessary adjustments are made to the Ref D to A's and the measurement process is repeated. It normally takes less than five measurements to set the oscillator but will take as many as twenty before issuing an error 40,41 or 42, depending on whether it is OSC0, OSC1 or OSC2 that it has failed to set up.

4. The Span/div and Reference frequency conditions dictate the master oscillator frequencies. By changing these conditions it is possible to determine whether the fault is present on one or all three oscillators. Having decided the fault applies to all three oscillators it may be found on AB1,AB7 or AD3. If the fault appears to be only on one oscillator it may still be found on any of the previous three boards as well as AA4,AA5 and AA6 for OSC0, AB3 and AB4 for OSC1 and AB2 for OSC2.

5. The functions described under Modes 1 to 3 of the diagnostic routines allow the following range of tests to be carried out:-

(a) Check the oscillator frequency ranges
(b) Check the oscillator response to a step voltage change
(c) Manually tune each oscillator through its range
(d) Measure the frequency of phase locked oscillators
(e) Look at oscillator drift and phase noise
(f) Check Ref D to A outputs
(g) Check AD3 oscillator measurement operation
(h) Monitor the number of measurements per oscillator setting
(i) Monitor oscillator set-ups with and without delays
(j) Monitor the Ref D to A's during oscillator set-ups
(k) Check out oscillators which refuse to phase lock
(l) Test measurement loop

UHF SYNTHESIZER FAULTS

Symptoms

6. (1) With the STD 10 MHz OUTPUT connected to INPUT, select PRESET, SPAN/DIV 40 MHz and REF LEVEL 10 dB.

SYMPTOM	FAULT	See Fig. No.
Signal pulsating back and forth across screen.	UHF master/slave phaselock broken.	1
Signal displaced by about 60 MHz from indicated position i.e.: DC marker appears at about 60 MHz.	Incorrect master/slave phaselock.	1
No signal displayed on screen, no tracking generator signal.	Slave oscillator failed. 2nd LO at incorrect frequency.	2
No tracking generator signal, standard signal displayed correctly.	Slave oscillator fault or tracking generator fault. 2nd LO at incorrect frequency.	2
Ref. frequency incorrect, tracking generator signal in excess of 400 MHz.	AA6/AB7 fault.	2

(2) Select SPAN/DIV 500 kHz, REF FREQ 10 MHz and REF LEVEL -10 dBm.

SYMPTOM	FAULT	See Fig. No.
Signal displaced from centre of screen.	HF master oscillator incorrectly phase locked. 2nd LO not phase locked.	5
Switching span to 200 kHz/div causes signal to disappear or incorrect signal to be displayed.	UHF master oscillator failing to lock on correct frequency.	3

(3) Select SPAN/DIV 5 kHz, REF FREQ 10 MHz, REF LEVEL -10 dBm and HORIZ POSN centre ref.

SYMPTOM	FAULT	See Fig. No.
Switching span to 2 kHz/div causes loss of signal or produces large sidebands.	HF master incorrectly locked.	5

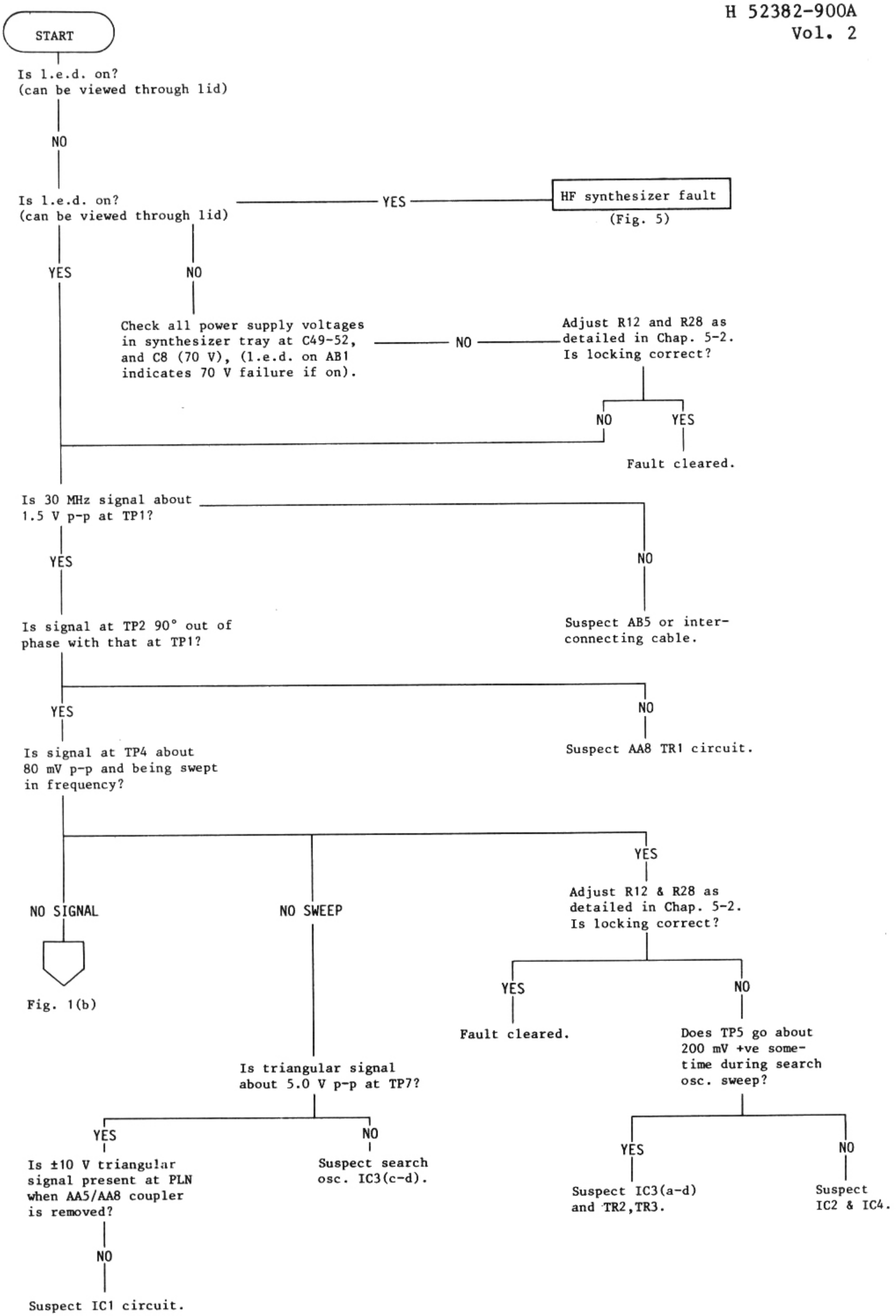


Fig. 1(a) - Fault location chart - UHF master/slave phase lock

Fig. 1(a)

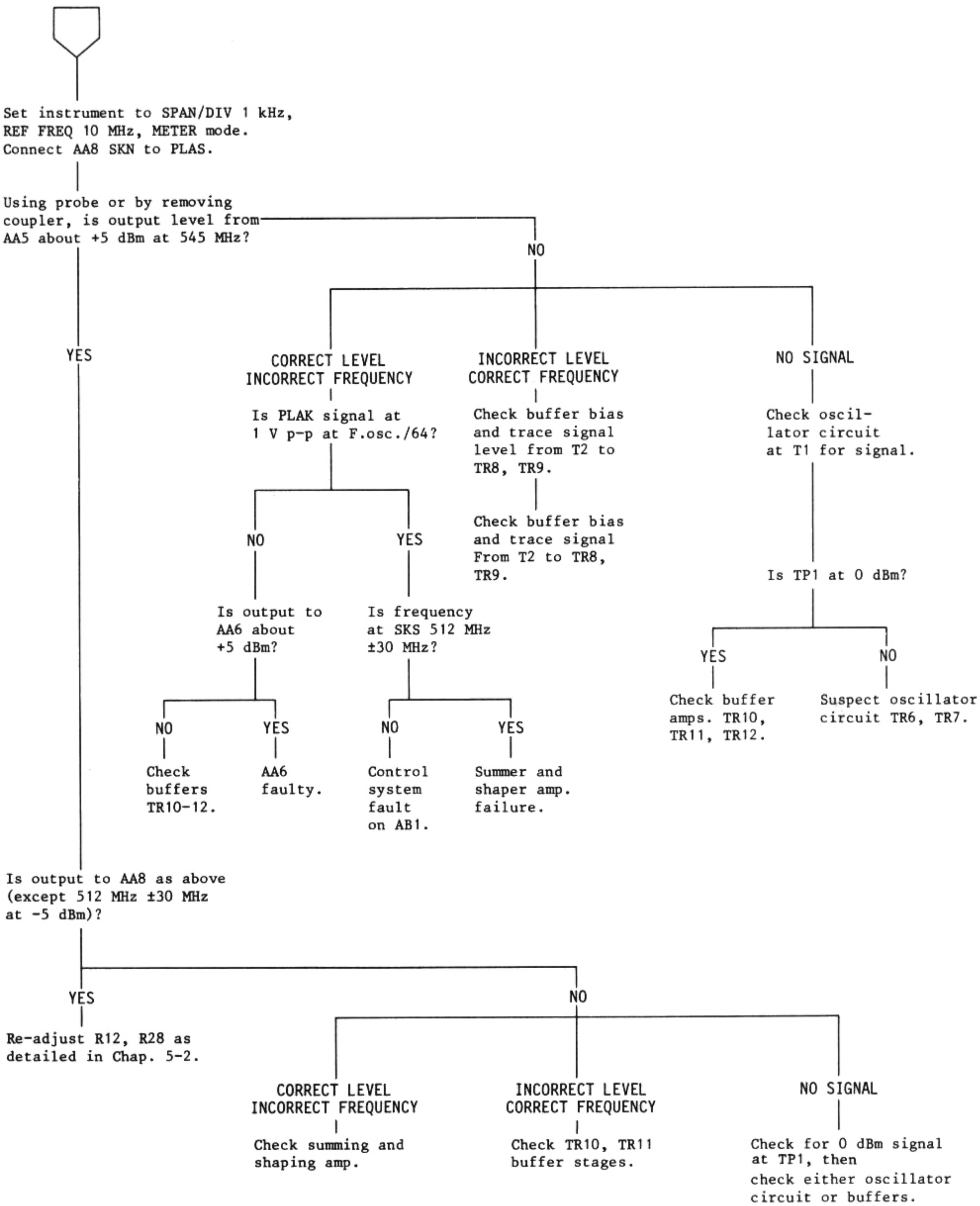


Fig. 1(b) - Fault location chart - UHF master/slave phase lock

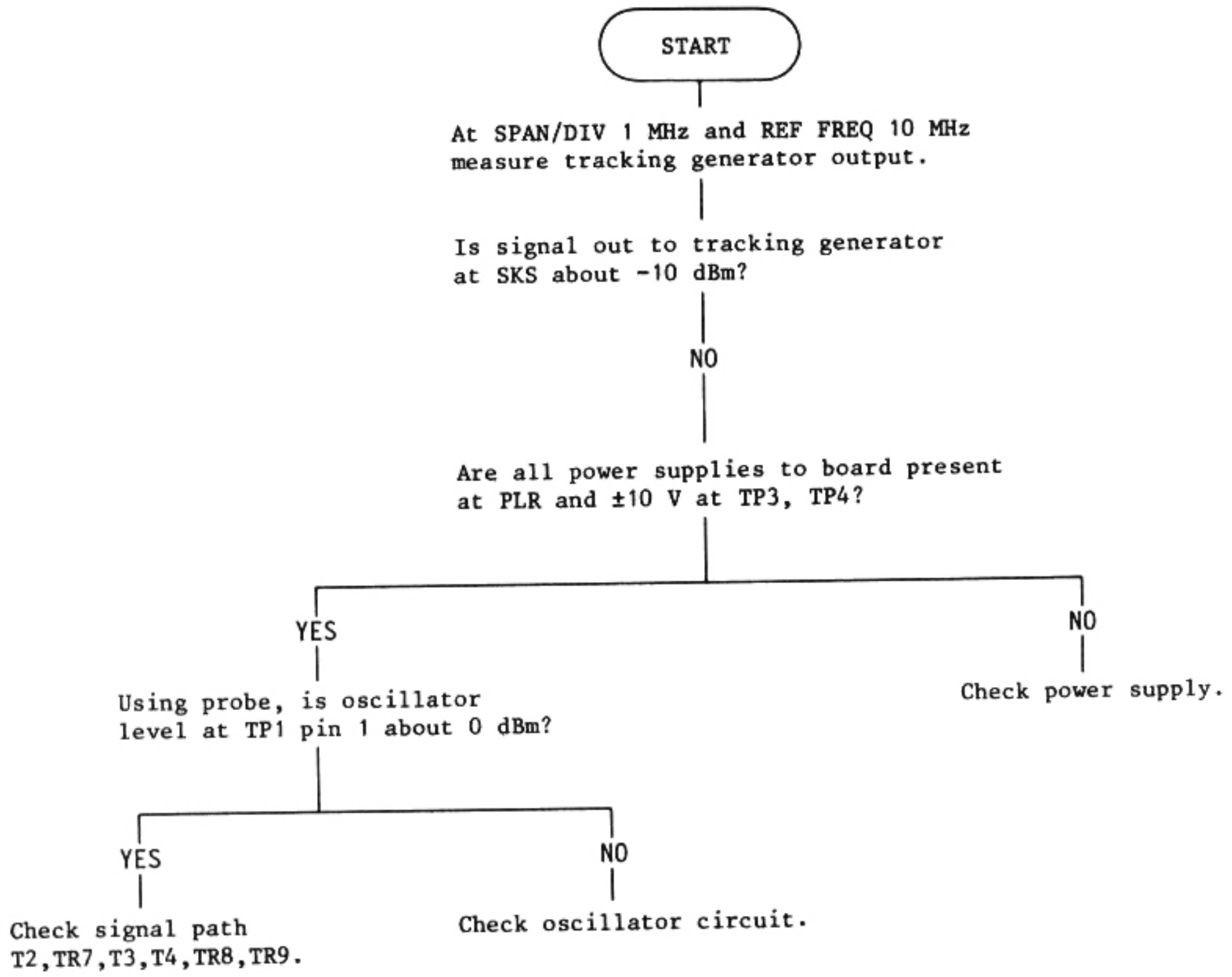


Fig. 2 - Fault location chart - No signal displayed

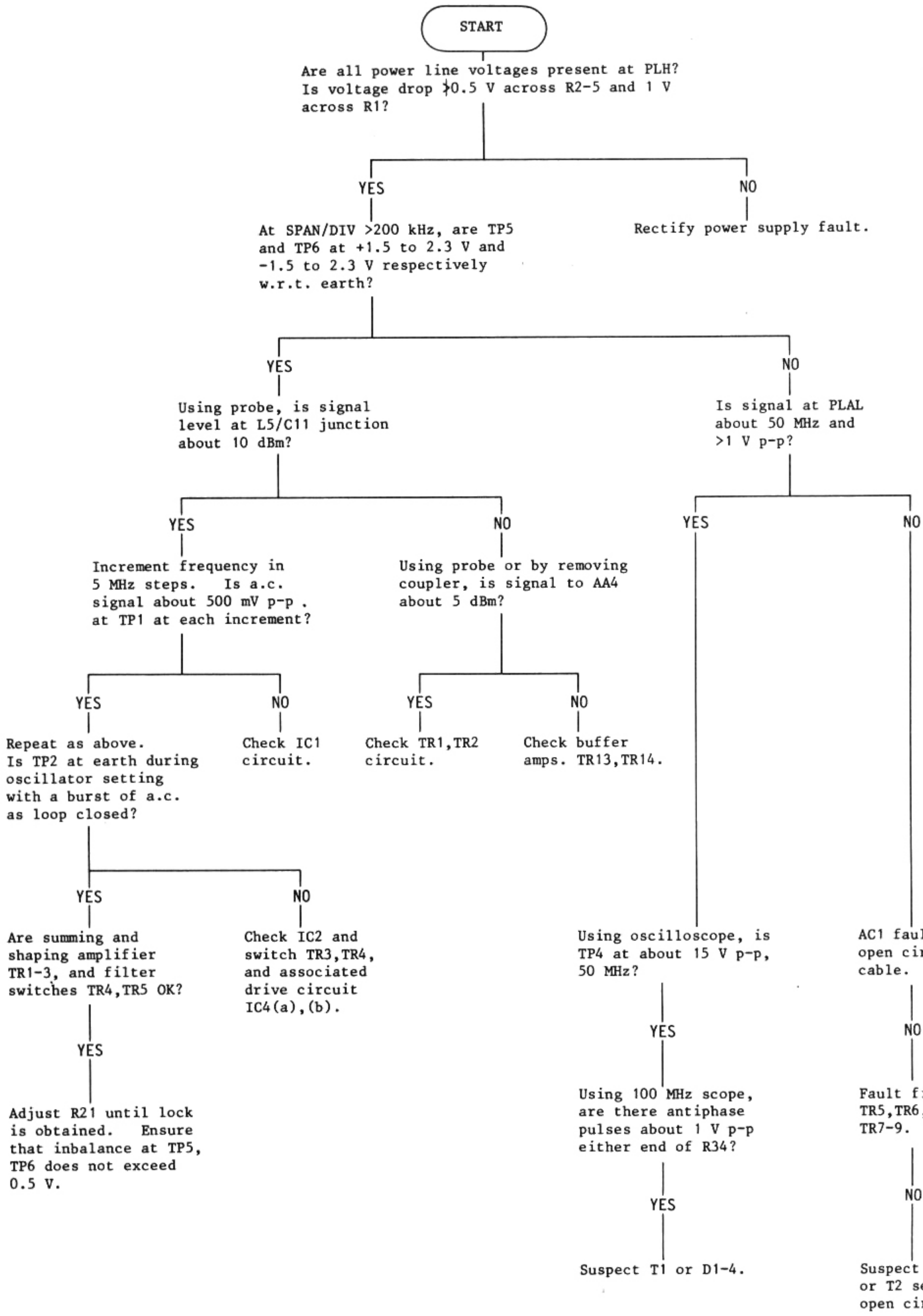


Fig. 3 - Fault location chart - UHF master oscillator failing to lock

2nd LOCAL OSCILLATOR FAULTS

Symptoms

7. Measure the 2nd LO output to the tracking generator and check that it is 550 MHz at +2 dBm

SYMPTOM	See Fig. No.
Correct amplitude, incorrect frequency	4(a)
Correct amplitude, correct frequency	4(b)
Incorrect amplitude, correct frequency	4(c)
No signal	4(d)

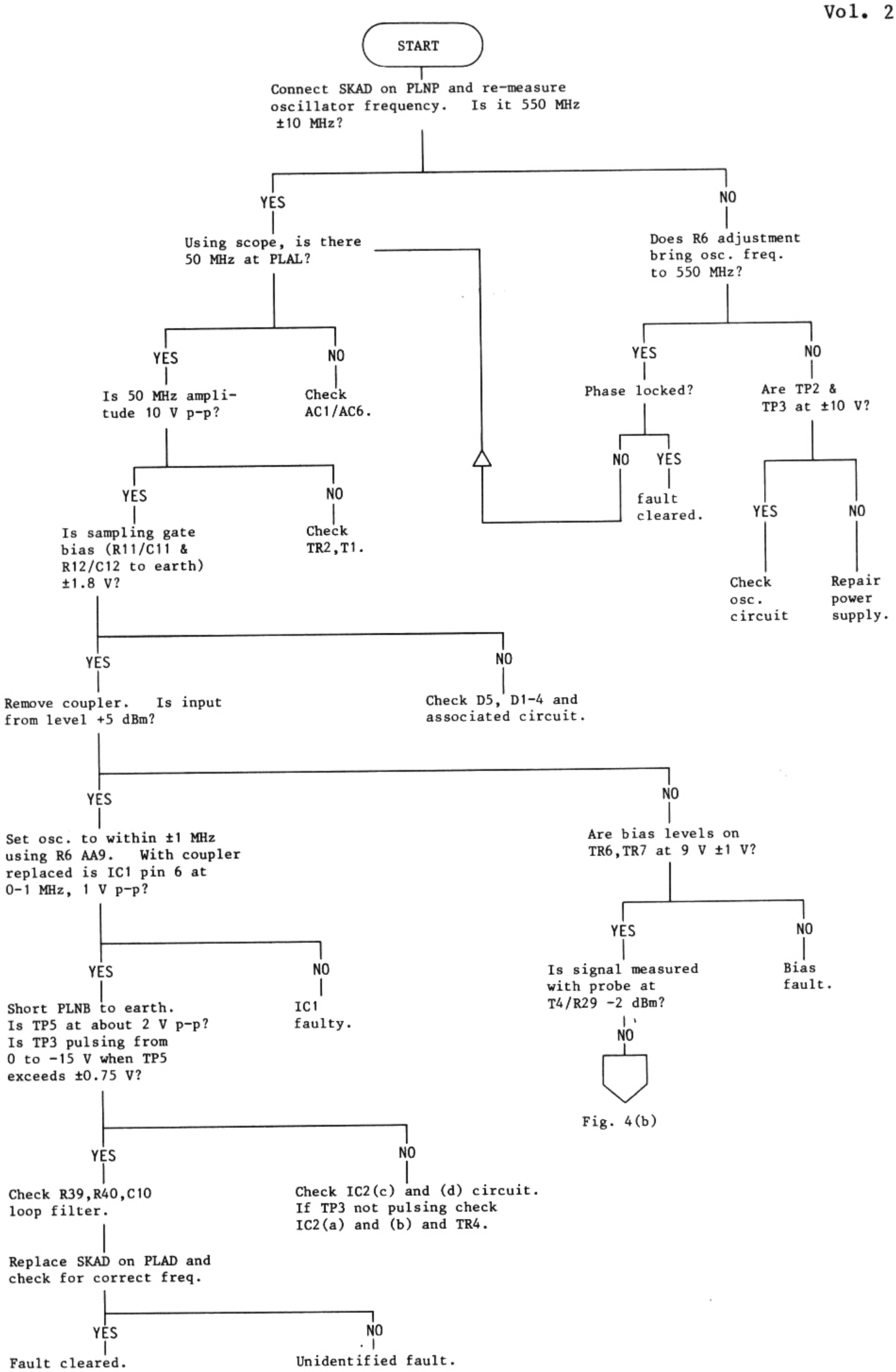


Fig. 4(a) - Fault location chart - 2nd LO

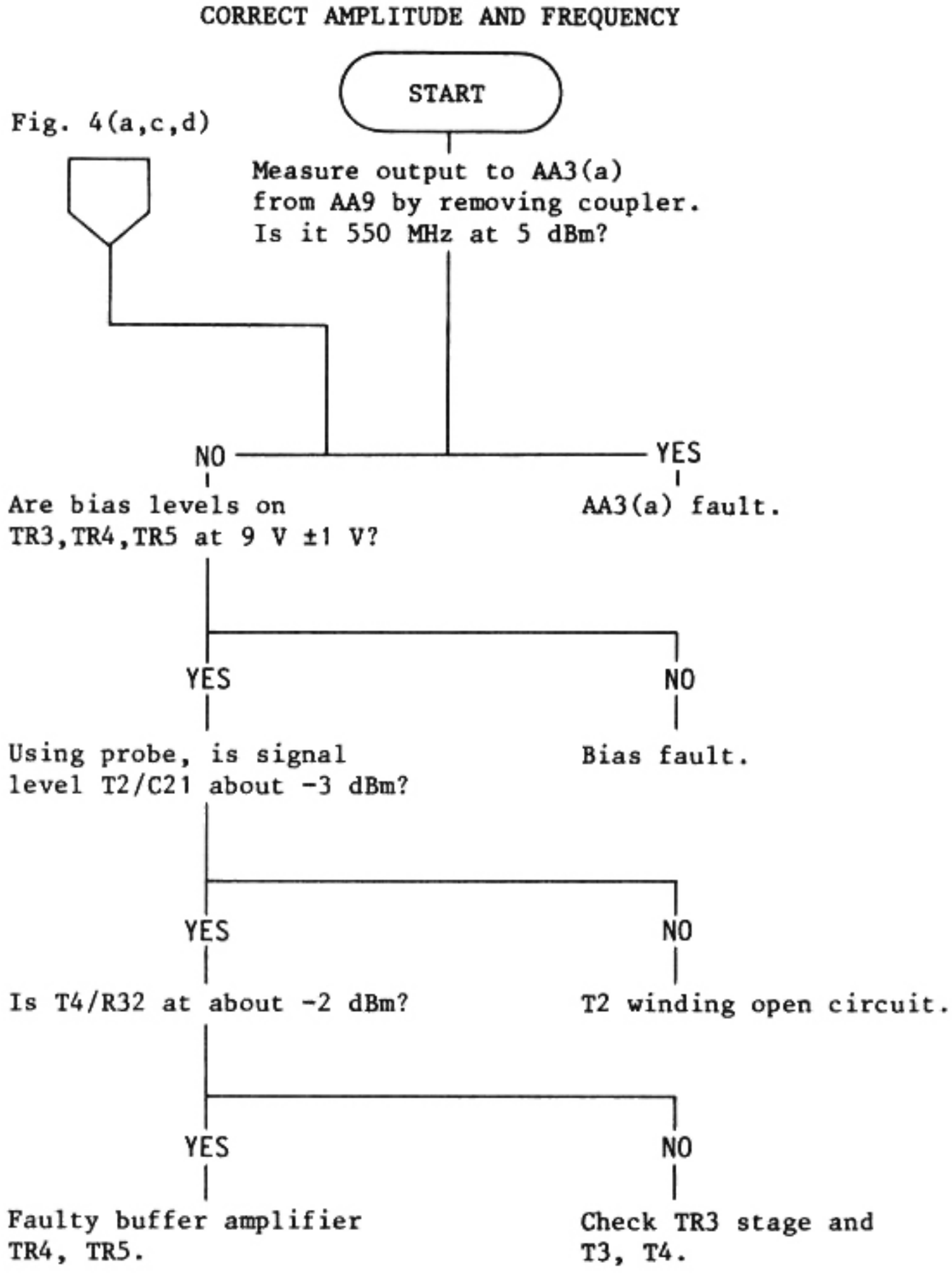


Fig. 4(a,c,d)

Fig. 4(b) - Fault location chart - 2nd LO

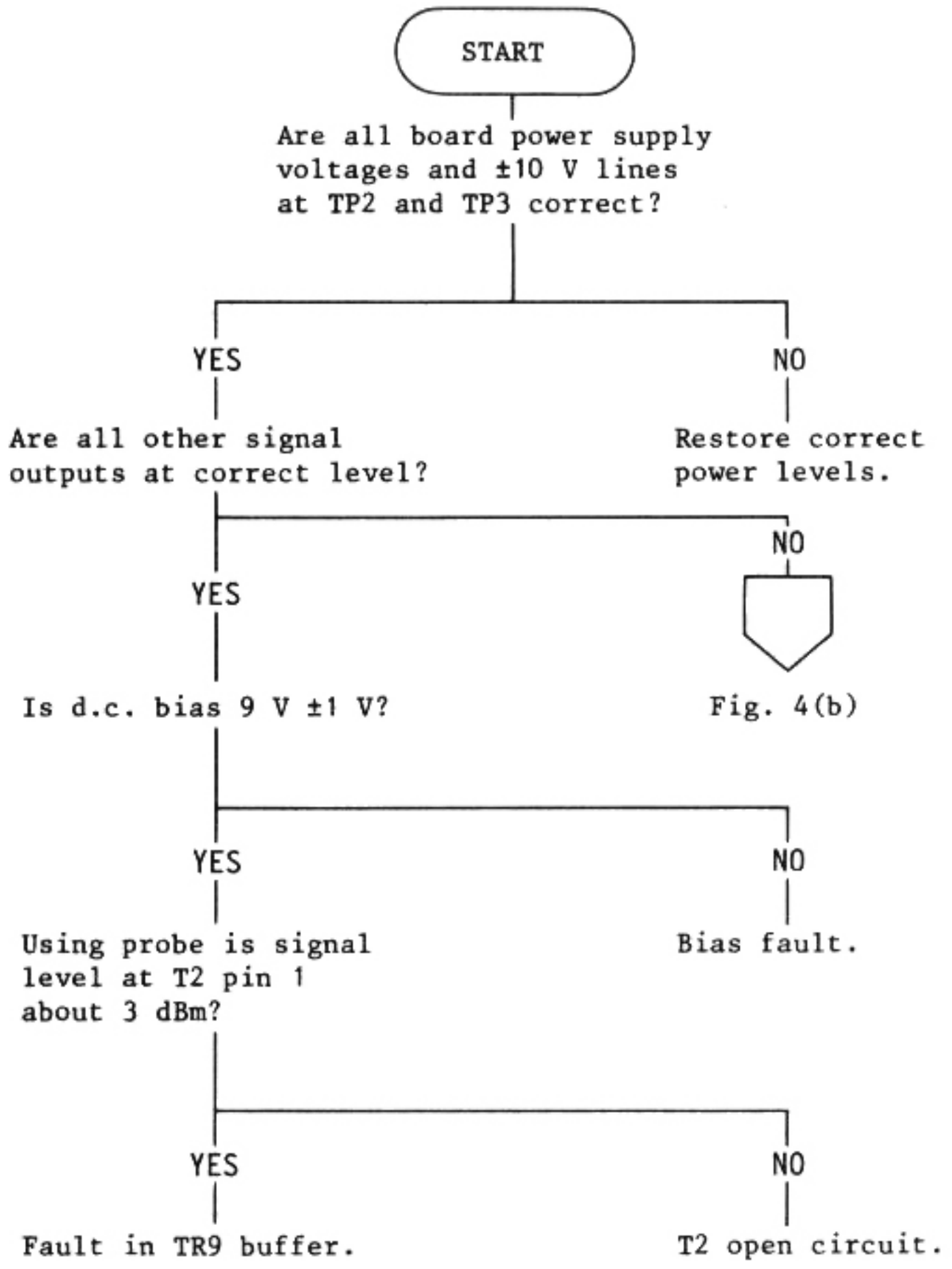


Fig. 4(c) - Fault location chart - 2nd LO

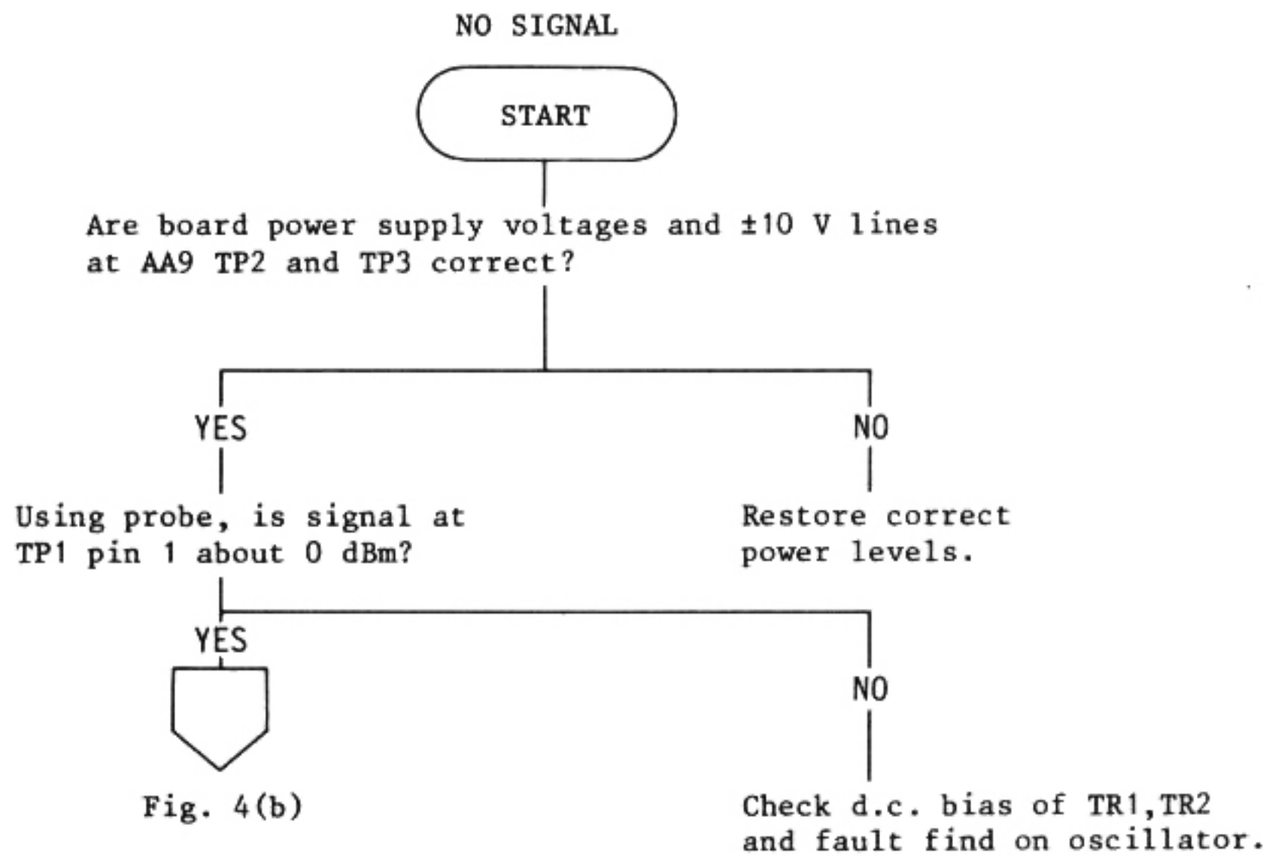


Fig. 4(d) - Fault location chart - 2nd LO

HF SYNTHESIZER FAULTS

Symptoms

8. Check for the occurrence of any of the following fault conditions within the indicated SPAN/DIV range.

SPAN/DIV	SYMPTOM	See Fig.
10 Hz to 40 MHz	Low or zero level	5(a)
500 kHz to 40 MHz or 10 Hz to 2 kHz	Centre frequency stable but wrong	5(b)
	Centre frequency unstable	5(c)
5 kHz to 200 kHz	Frequency error > 1 kHz	5(d)
	Frequency jitter > 1 kHz	5(e)
	No sweep	5(f)
10 Hz to 2 kHz	No sweep	5(g)

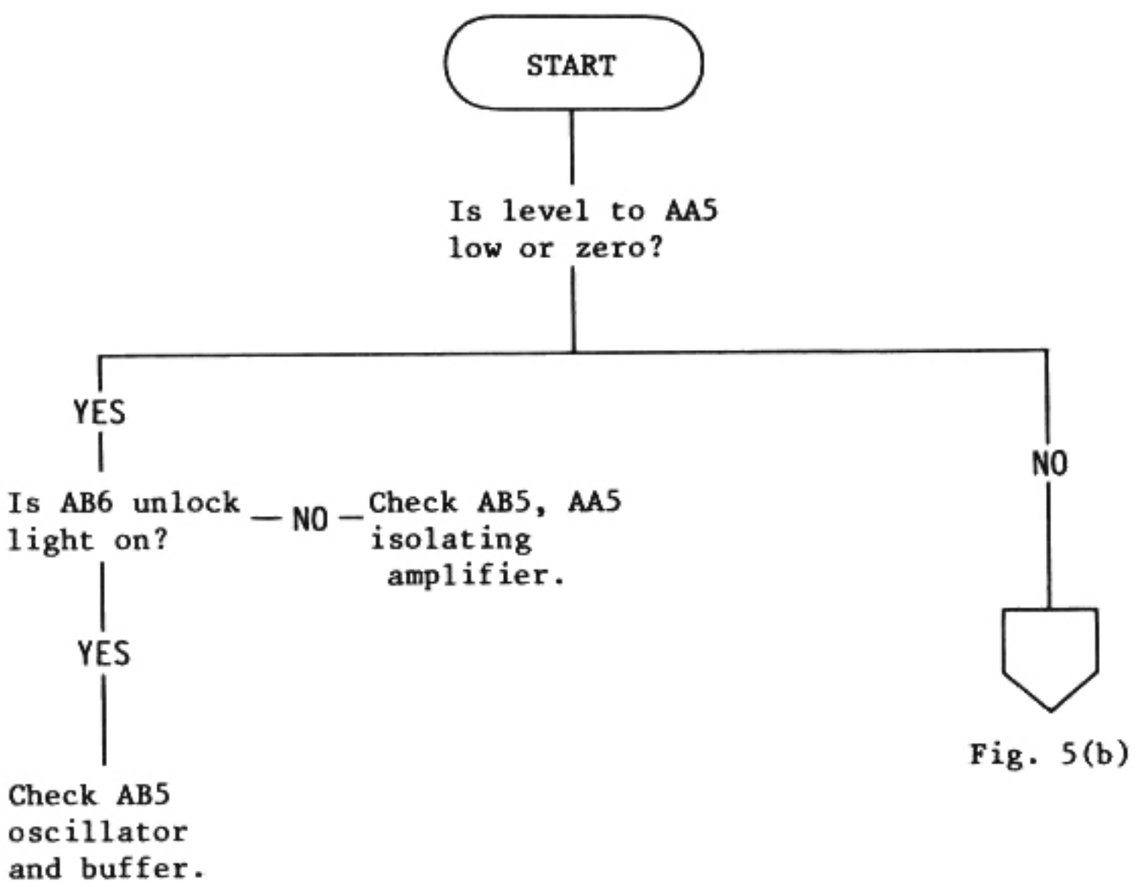


Fig. 5(b)

Fig. 5(a) - Fault location chart - HF synthesizer

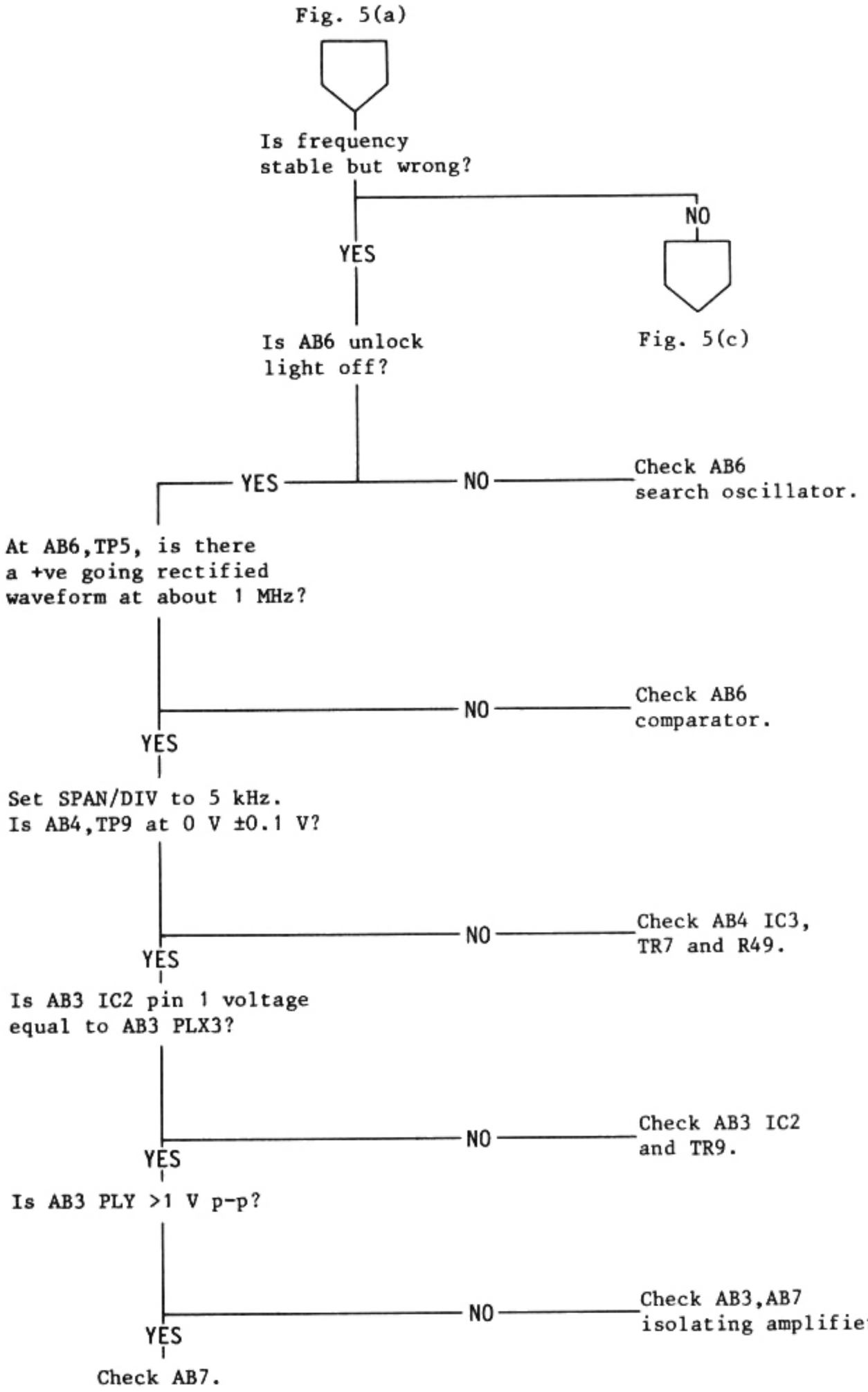


Fig. 5(b) - Fault location chart - HF synthesizer

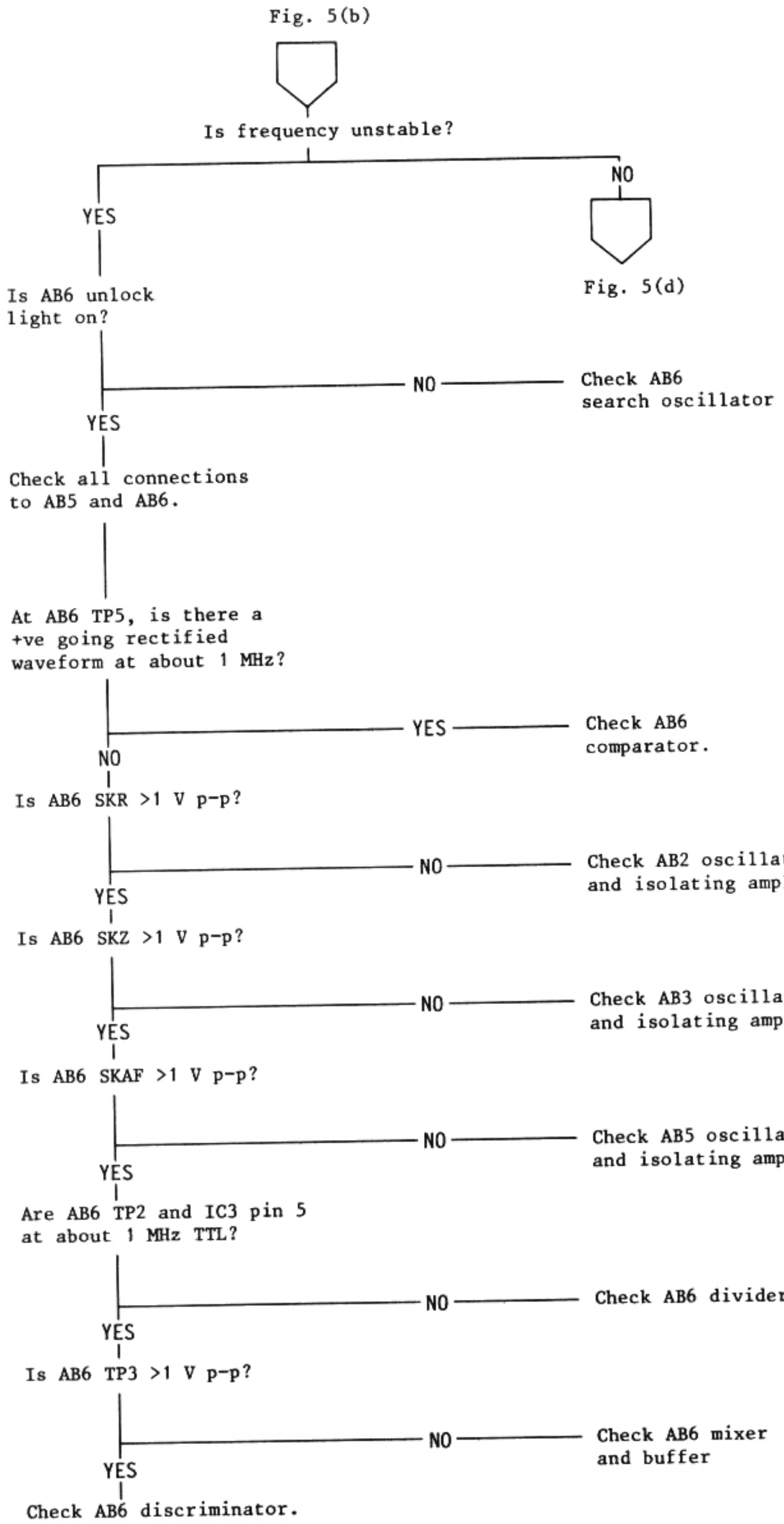


Fig. 5(c) - Fault location chart - HF synthesizer

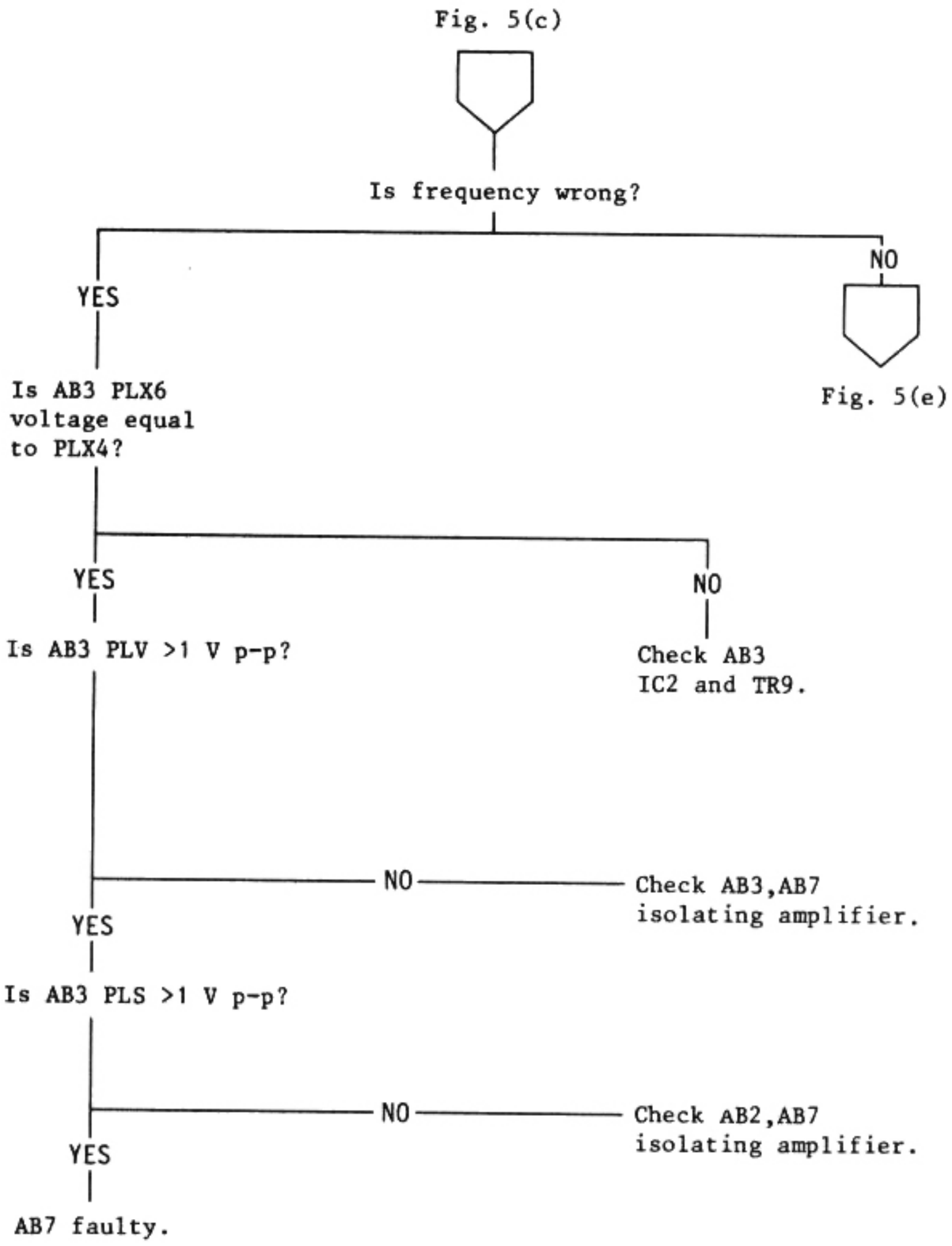


Fig. 5(d) - Fault location chart - HF synthesizer

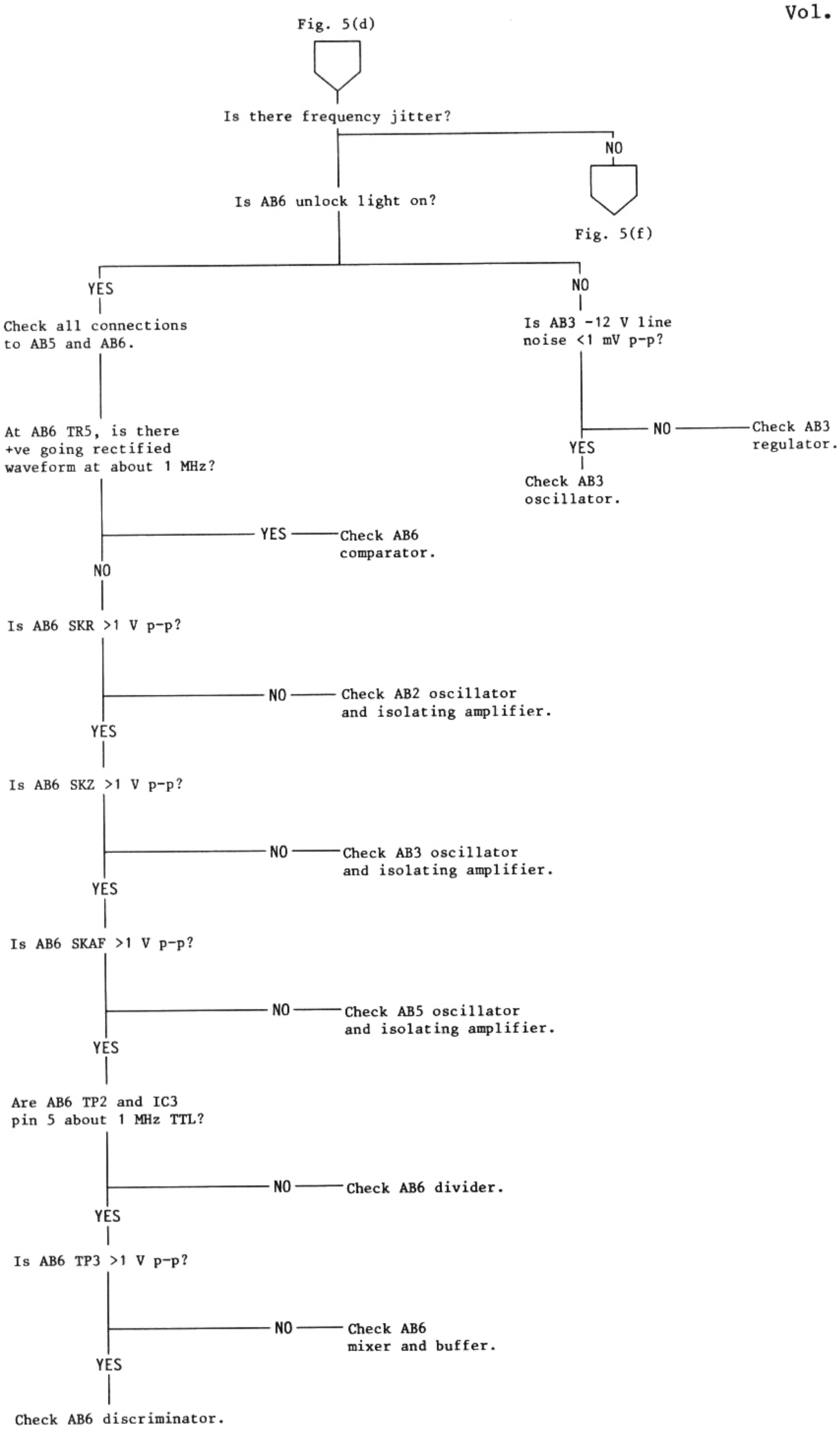


Fig. 5(e) - Fault location chart - HF synthesizer

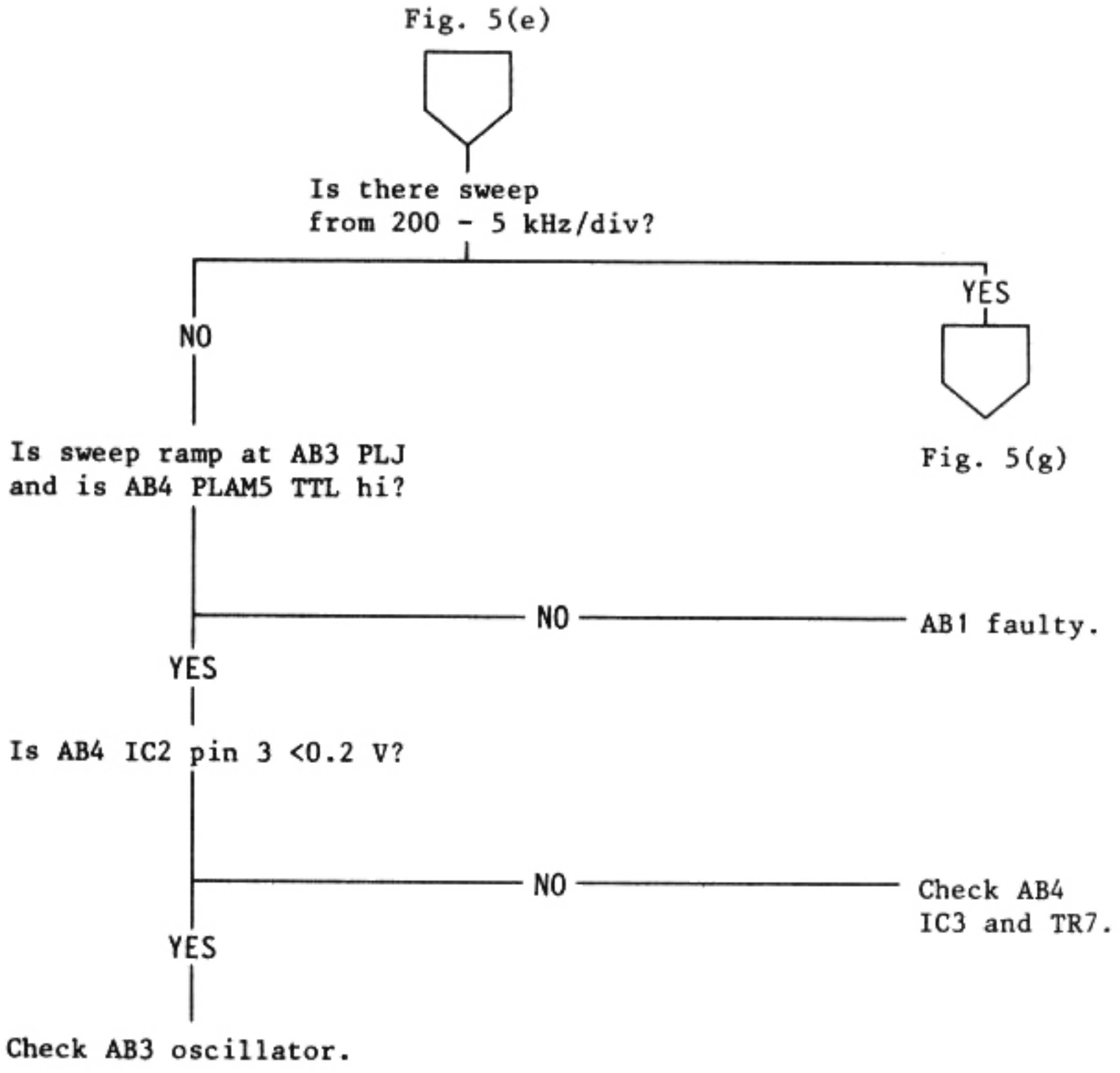


Fig. 5(f) - Fault location chart - HF synthesizer

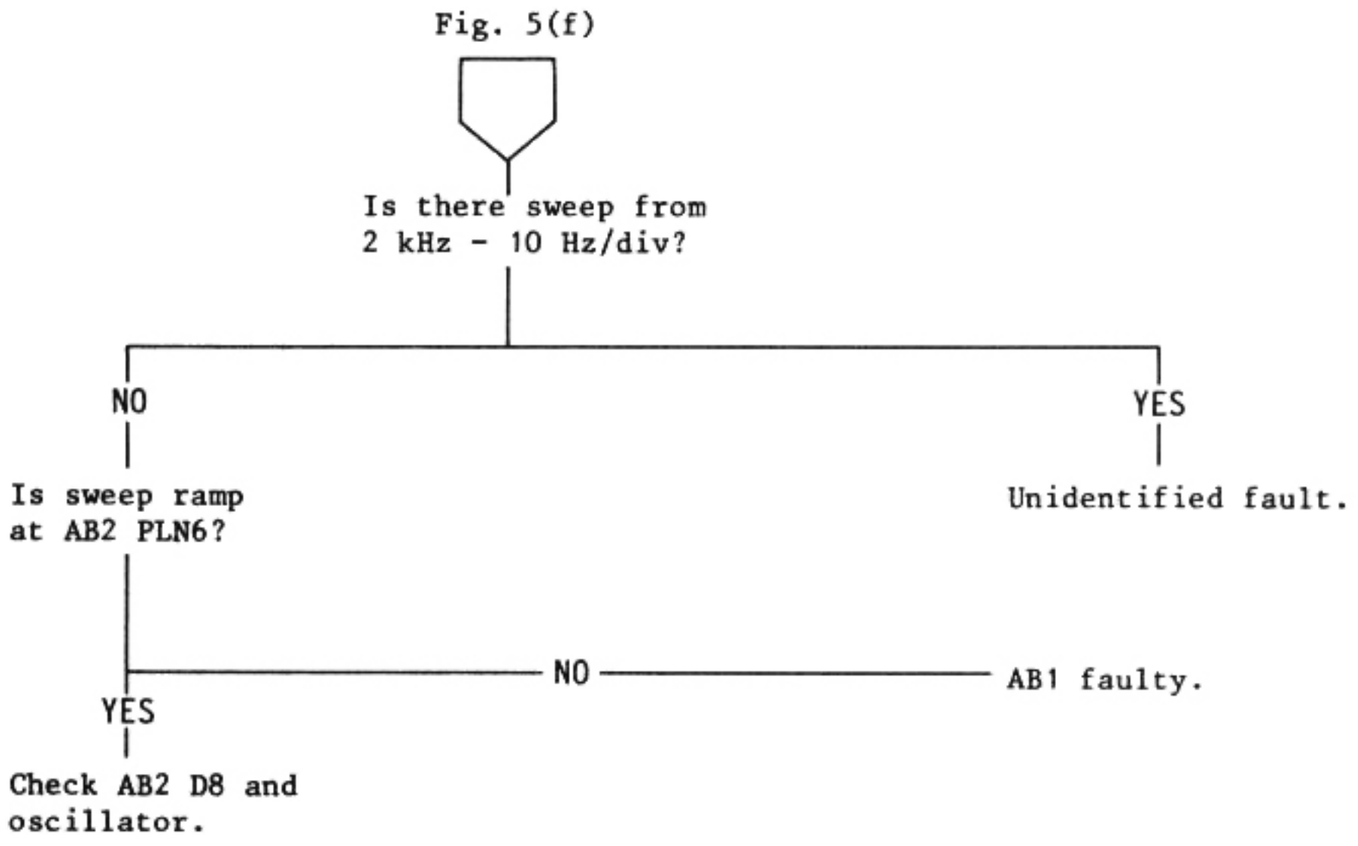


Fig. 5(g) - Fault location chart - HF synthesizer

Chapter 5-3, Annex B

FAULT DIAGNOSIS
- AUXILIARY INFORMATION -

CONTENTS

Para.
1 Introduction
2 Linearization
7 Frequency count

Fig. Page
1 Intermediate frequency configuration 3
2 Relationship between LO and IF at different marker frequencies . 3

INTRODUCTION

1. This Annex contains supplementary information to support certain branches of the fault location charts.

LINEARIZATION

2. In order to get a linear display an oscillator must sweep through a given frequency in a given period of time. For example, with a 10 MHz/div span and a 10 ms/div sweep time the sweep oscillator's rate of change of frequency with time is 1 MHz/ms. Assuming that a change of 10 MHz is brought about by a 10 V change in the oscillators reference voltage, it follows that in order to get a frequency change of 1 MHz/ms the oscillator's reference voltage must be changed by 1 V/ms. If the relationship between voltage and frequency is constant, a sweep rate of 1 V/ms will produce a linear sweep ramp.

3. The span and reference frequency combinations available in the 2380/82 are achieved by sweeping one of the three master oscillators knowing that the other two are at fixed frequencies. The voltage/frequency characteristics of the master oscillators are not constant over their total range. However a small frequency increment can be assumed to be constant but having slightly different values to its neighbours. If a frequency increment of 10 MHz is adopted, the previous example may be rearranged such that it still requires 100 V to sweep 100 MHz but the voltage frequency characteristic is no longer constant. This is shown as follows:

ZONE	FREQUENCY RANGE (MHz)	SWEEP VOLTAGE (V)	VOLTAGE CHANGE (V)
1	600-610	6	6
2	610-620	13	7
3	620-630	21	8
4	630-640	30	9
5	640-650	40	10
6	650-666	51	11
7	660-670	63	12
8	670-680	76	13
9	680-690	88	12
10	690-700	100	12

If a 100 V change on the output of the Sweep D to A corresponds to 1000 sweep clocks it can be assumed that clocking the Sweep D to A from 0 to 60 in 10 ms will linearly sweep the oscillator over the first 10 MHz. If at this moment an interrupt is generated which changes the period of the sweep clock, such that in the next 10 ms a total of 70 clocks occur, the second portion of the sweep will be linear. This routine is repeated at each frequency zone boundary until the sweep is completed.

4. The above example is somewhat simplified, but by calibrating the synthesizer, as described in Mode 5 of the diagnostic routines, it is possible to apply this technique to all three master oscillators. Changing the synthesizer recalculates the frequency zones and sweep rates as well as generating an interrupt structure which indicates the position of the frequency zone boundaries or break points during the sweep.

5. The size of the frequency zone determines how near the straight line approximation fits the voltage/frequency characteristic. Another source of error is due to the counter/dividers on AD3 which only allow 1% adjustment of the sweep rate. These errors are reduced by using the Sweep gain D to A which allows this technique to meet the 2% non-linearity specification.

6. Bad linearity can be the result of many things ranging from corrupted calibration data in AD3 IC22, faulty counter/timers AD3 IC30, faulty interrupts 6.5, faults on any of the analogue sweep generation circuits on AB1 and possible changes to the oscillators AA5, AB2 and AB3. The waveforms shown alongside AB1 and AD3 show the sweep and interrupt waveforms which may indicate the troublesome area. Changing the span/div, hence the sweep oscillator, may confirm or lead to the fault.

FREQUENCY COUNT

7. On a super-heterodyne system the relationship between three ports is as follows:

Intermediate frequency = Local oscillator frequency ± Input frequency

Knowing the intermediate frequency (IF) is band limited, simultaneous measurement of this and the local oscillator frequency (LO) gives the input frequency. The IF configuration of the 2382 is as follows:

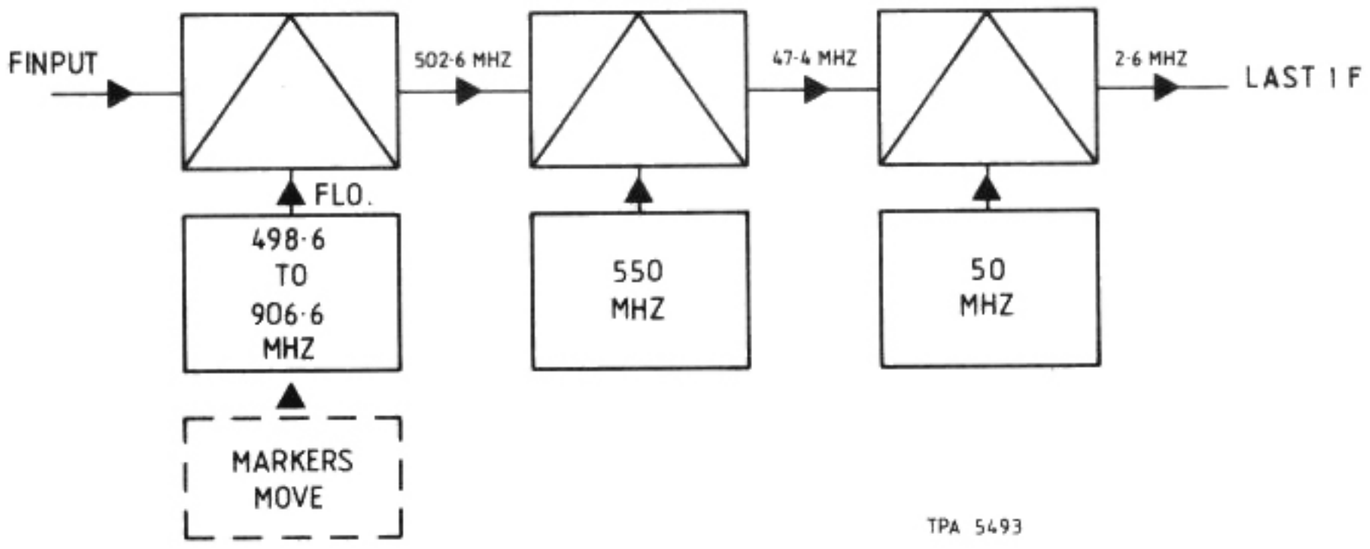


Fig. 1 Intermediate frequency configuration

$$F_{INPUT} = F_{LO} - 500 - \text{LAST IF}$$

8. The last IC is translated to t.t.l. levels on AD1 before being counted in AD2 IC47 counters 1 and 2. This count process takes place in flyback and is gated by AD3 which is simultaneously measuring the sweep oscillator. The position of the marker on the forward sweep determines the sweep voltage which is applied during this measurement.

9. During the sweep AD2 IC47 counter 2, counts the sweep clock. When freq. count is on, an INT7.5 is generated at the marker ordinate. This interrupts the processor which reads the value in counter 2 and is then loaded into the Sweep D to A in flyback prior to a frequency count.

10. The example in Fig. 2 illustrates how the result of a frequency count is independent of marker position.

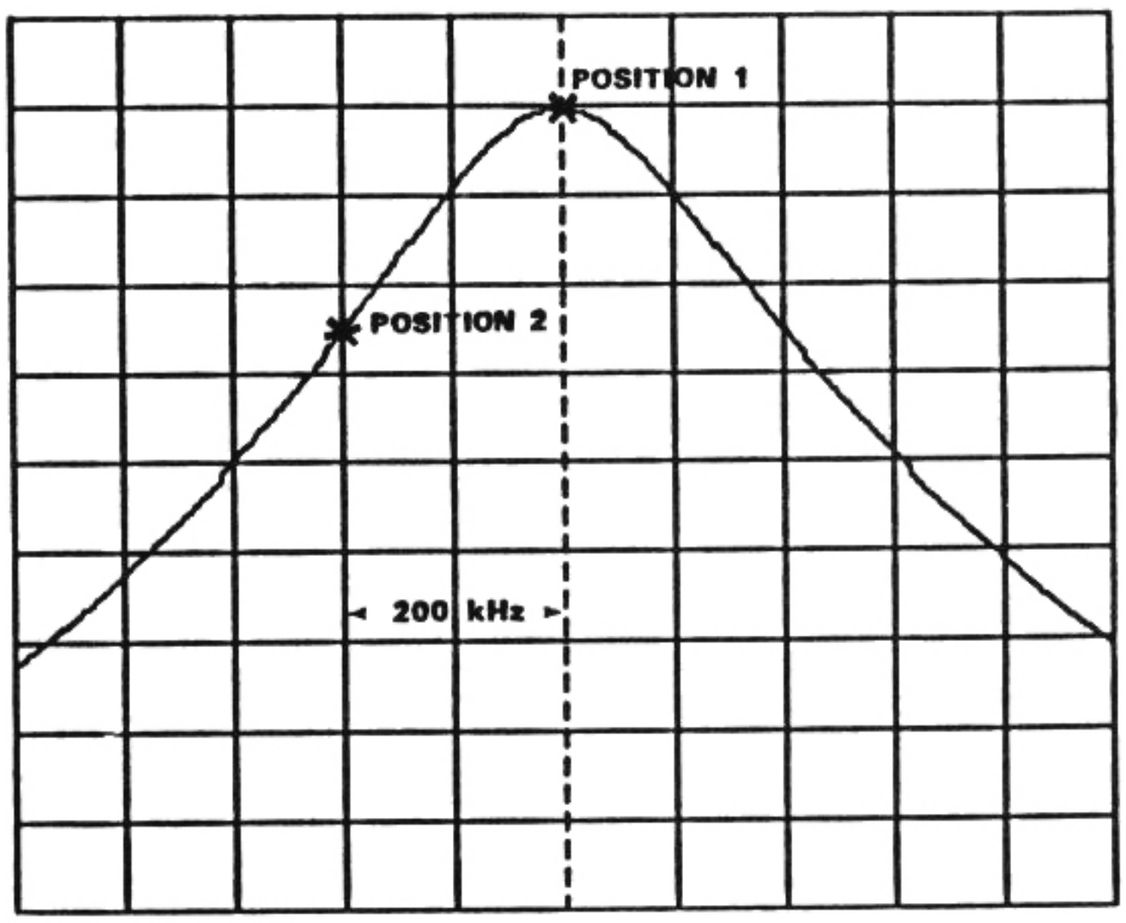


Fig. 2 Relationship between LO and IF at different marker frequencies

Display shows a 100 MHz signal at SPAN/DIV = 100 kHz

In position 1: $F_{INPUT} = 602.6 - 500 - 2.6 = 100$ MHz

In position 2: $F_{INPUT} = 602.4 - 500 - 2.4 = 100$ MHz

11. A series of waveforms in Chap. 7 for both AD3 and AB1 show the relationship between the marker positions, the sweep flyback, the gate periods and INT7.5 which should enable a fault to be traced.

Chapter 6

REPLACEABLE PARTS

CONTENTS

Para.
1 Introduction
3 Abbreviations
4 Component values
6 Ordering
7 Components
7 Unit A0 - 400 MHz Spectrum Analyzer RF unit
8 Unit AA0/AB0 - RF box assembly (AA/AB)
9 Unit AA1 - Input attenuator assembly
10 Board AA1a - Input attenuator
11 Unit AA2 - 400 MHz input filter assembly
12 Board AA2a - Input mixer
13 Unit AA3 - 502.6 MHz BPF
14 Board AA3a - Second mixer
15 Board AA4 - Sampling gate
16 Board AA5 - Master VCO
17 Board AA6 - Divider
18 Board AA7 - Slave VCO
19 Board AA8 - Phase detector
20 Board AA9 - Second LO VCO
21 Board AA10 - Sampling gate
22 Board AA11 - Line cleaner
23 Unit AB0 - AB tray assembly
24 Board AB1 - D to A converter
25 Board AB2 - Interpolation oscillator
26 Board AB3 - Master VCO
27 Board AB4 - Sampling gate
28 Board AB5 - Slave VCO
29 Board AB6 - Phase detector
30 Board AB7 - Oscillator select
31 Board AB8 - Attenuator control
32 Unit AC0/AD0 - IF box assembly (AC/AD)
33 Board AC1 - 50 MHz crystal oscillator
34 Board AC2 - 47.4 MHz i.f. amplifier
35 Board AC3 - 2.6 MHz LC filter
36 Board AC4 - 100 kHz i.f. crystal filter
37 Board AC5 - 2.6 MHz crystal filter
38 Board AC6 - Phase detector
39 Unit AD0 - AD tray
40 Board AD1 - Logarithmic amplifier
41 Board AD2 - Logarithmic amplifier interface
42 Board AD3 - Microprocessor
43 Board AD4 - 10 MHz calibrator
44 Unit AE0 - Tracking generator tray
45 Board AE1 - 47.4 MHz crystal oscillator

continued ...

CONTENTS (continued)

Para.
46 Board AE2 - Buffer
47 Unit AE3 - 502.6 MHz TG i.f. filter assembly
48 Board AE3a - Narrow band mixer/buffer
49 Board AE4 - TG buffer
50 Unit AE5 - TG output filter
51 Board AE5a - Wide band mixer/buffer
52 Board AE6 - Amplifier leveller
53 Board AE7 - Switch
54 Unit AF0 - Front panel
55 Board AF1 - Front panel keyboard
56 Board AF2 - Front panel logic
57 Unit AR0 - Rear panel
58 Board AR1 - Signal interface board
59 Board AR2 - Power supply interface
60 Board AZ1 - Optical encoder assembly
61 Board AZ2 - Sweep span switch

INTRODUCTION

1. Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification, e.g. A0, AA2, AB1 etc.

2. The complete component reference carries its unit number as a prefix e.g. AB3C3 (capacitor C3 on the memory board) but for convenience in the text and on circuit diagrams the prefix is not used. However, when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. The components are listed in alphanumerical order of the complete circuit reference and the following abbreviations are used :

C : capacitor
Carb : carbon
Cer : ceramic
D : semiconductor diode
Elec : electrolytic
FS : fuse
IC : integrated circuit (package)
L : inductor
LP : lamp
Max : maximum
ME : meter
Met : metal
Mic : mica
Min : minimum
Ox : oxide
PL : plug
Plas : plastic

R	:	resistor
S	:	switch
SK	:	socket
T	:	transformer
Tant	:	tantalum
TP	:	terminal
TR	:	transistor
Var	:	variable
W	:	watts at 70^0C
WW	:	wirewound
X	:	miscellaneous
XL	:	crystal

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by an * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detailed improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

ORDERING

6. When ordering replacements, address the order to our Service Division (address at rear of manual) or nearest agent and specify the following for each component required:-

(1) Type# and serial number of equipment.
(2) Complete circuit reference.
(3) Description.
(4) Part number.

#As given on the serial number label at the rear of the instrument; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number
Unit A0	- 400 MHz Spectrum Analyzer RF unit	
7. When ordering, prefix circuit reference with A0		
	Complete unit	52382-900A
	TRACKING GEN. BOX ASSY AE	44990-452G
	RF BOX ASSY AA/AB	44990-450J
	IF BOX ASSY AC/AD	44990-451F
	FRONT PANEL ASSY	44990-468A
	REAR PANEL ASSY	44990-469Z
	CABLE ASSY 24-WAY RIBBON (AD3-AF2)	43129-957V
	CABLE ASSY 16-WAY RIBBON (AD3-AR1)	43129-958S
	CABLE ASSY 26-WAY RIBBON (AD3-AB1)	43129-959W
	CABLE ASSY TG TO ATTEN (AE0-AA1a)	43129-917N
	CABLE ASSY (AE2-AA9)	43129-921L
	CABLE ASSY (AE4-AA7)	43129-923F
	CABLE ASSY (POWER)	43130-369S
	CABLE ASSY (DATA)	43130-082H

NOTES ...

(1) PROGRAMMED PROMS ARE LISTED UNDER BOARDS AD2 AND AD3.

(2) CABLE ASSEMBLIES NOT LISTED ABOVE CAN GENERALLY BE FOUND UNDER A RELEVANT BOX OR TRAY ASSEMBLY.

Circuit Ref	Description	Part Number
Unit AA0/AB0	- RF box assembly (AA/AB)	
8.	When ordering, prefix circuit reference with AA0/AB0	
	Complete unit	44990-450J
C1	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C36	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C37	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C38	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C39	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AA0/AB0	- RF box assembly (AA/AB)	(Contd.)
C40	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C41	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C42	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C43	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C45	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C48	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C49	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C50	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C53	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C57	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C58	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C59	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C60	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C61	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C62	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C63	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C64	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C65	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C66	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C67	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C68	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C69	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C70	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C71	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C72	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C73	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C74	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C75	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C76	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C77	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C78	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C79	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C80	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C81	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C82	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AA0/AB0	- RF box assembly (AA/AB)	(Contd.)
C83	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C84	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C85	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C86	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C87	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C88	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C89	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C90	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C91	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C92	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C93	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C94	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C95	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
L2	INDUCTOR CHOKE GEN	44190-036B
L3	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L6	INDUCTOR CHOKE GEN	44190-036B
L7	IND CHOKE 1000UH 10% LAQ	23642-567C
L8	INDUCTOR CHOKE GEN	44190-036B
L9	IND CHOKE 1000UH 10% LAQ	23642-567C
L11	IND CHOKE 1000UH 10% LAQ	23642-567C
L12	INDUCTOR CHOKE GEN	44190-036B
L13	INDUCTOR CHOKE GEN	44190-036B
L14	INDUCTOR CHOKE GEN	44190-036B
L15	IND CHOKE 1000UH 10% LAQ	23642-567C
L16	IND CHOKE 1000UH 10% LAQ	23642-567C
L17	IND CHOKE 1000UH 10% LAQ	23642-567C
L18	IND CHOKE 1000UH 10% LAQ	23642-567C
L20	IND CHOKE 1000UH 10% LAQ	23642-567C
L21	INDUCTOR CHOKE GEN	44190-036B
L22	INDUCTOR 1MH PWR	44190-042Z
L23	IND CHOKE 1000UH 10% LAQ	23642-567C
L24	INDUCTOR CHOKE GEN	44190-036B
L26	IND CHOKE 470UH 10% SCREENED	23642-333B
L27	INDUCTOR CHOKE GEN	44190-036B
L28	IND CHOKE 470UH 10% SCREENED	23642-333B
L29	INDUCTOR CHOKE GEN	44190-036B
L30	INDUCTOR	34900-918Y
L31	INDUCTOR CHOKE GEN	44190-036B

Circuit Ref	Description	Part Number
Unit AA0/AB0	- RF box assembly (AA/AB)	(Contd.)
L32	INDUCTOR CHOKE GEN	44190-036B
L33	IND CHOKE 1000UH 10% LAQ	23642-567C
L34	INDUCTOR CHOKE GEN	44190-036B
L35	IND CHOKE 1000UH 10% LAQ	23642-567C
L36	INDUCTOR CHOKE GEN	44190-036B
L37	IND CHOKE 470UH 10% SCREENED	23642-333B
L38	IND CHOKE 1000UH 10% LAQ	23642-567C
L39	IND CHOKE 470UH 10% SCREENED	23642-333B
L40	IND CHOKE 1.0UH 10% LAQ	23642-549L
L41	INDUCTOR	34900-918Y
L42	IND CHOKE 470UH 10% SCREENED	23642-333B
L43	IND CHOKE 1000UH 10% LAQ	23642-567C
L44	IND CHOKE 470UH 10% SCREENED	23642-333B
L45	IND CHOKE 1000UH 10% LAQ	23642-567C
L46	IND CHOKE 470UH 10% SCREENED	23642-333B
L47	INDUCTOR	34900-918Y
L48	IND CHOKE 100UH 10% SCREENED	23642-325P
L49	IND CHOKE 100UH 10% SCREENED	23642-325P
L50	INDUCTOR CHOKE GEN	44190-036B
PLS	CON RF SMC MALE 50 BKHD ELBOW	23444-383P
PLT	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
PLU	CON RF SMC MALE 50 BKHD ELBOW	23444-383P
PLAA	CON RF SMB MALE 50 BKHD ELB	23444-351P
PLAB	CON RF SMB MALE 50 BKHD ELB	23444-351P
PLAE	CON RF SMB MALE 50 BKHD ELB	23444-351P
PLAF	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
SKS	CON RF SMC FEM 50 FREE UT85	23444-371L
SKT	CON RF SMB FEM 50 FREE RG178	23444-321M
SKU	CON RF SMC FEM 50 FREE UT85	23444-371L
SKV	CON PART MIN HOUSING 1ROW 5P	23435-168R
SKAA	CON RF SMB FEM 50 FREE RG178	23444-321M
SKAE	CON RF SMB FEM 50 FREE RG178	23444-321M
	CABLE ASSY 10-WAY RIBBON	43129-962W
	CABLE ASSY ATTEN-AA2a	43129-918L

Circuit Ref	Description	Part Number
Unit AA1	- Input attenuator assembly	
9.	When ordering, prefix circuit reference with AA1	
	Complete unit	44990-423W
C1	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
C2	CAP CER 1NO 500V 20%+ L/T SCR	26373-714F
MP1	SW MICRO DRIVE ASSY	41319-027H
PLAH	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
PLAP	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
R1	RES CC 1KO 1/8W 5%	24331-967A
R2	RES CC 1KO 1/8W 5%	24331-967A
R3	RES CC 2K7 1/8W 5%	24331-969H
R4	RES CC 2K7 1/8W 5%	24331-969H
R5	RES CC 2K7 1/8W 5%	24331-969H
R6	RES CC 2K7 1/8W 5%	24331-969H
R7	RES CC 2K7 1/8W 5%	24331-969H
R8	RES CC 2K7 1/8W 5%	24331-969H
RLA	SOLENOID ASSY	44990-370Z
RLB	SOLENOID ASSY	44990-370Z
RLC	SOLENOID ASSY	44990-370Z
RLD	SOLENOID ASSY	44990-370Z
RLE	SOLENOID ASSY	44990-370Z
RLF	SOLENOID ASSY	44990-370Z
SKAJ	CON RF N FEM 50 PANEL	23443-740W
	CABLE ASSY 10-WAY RIBBON	43129-960V

Circuit Ref	Description	Part Number
Board AA1a	- Input attenuator	
10.	When ordering, prefix circuit reference with AA1a	
	Complete unit	44828-450Y
C1	CAP CER 1N0 63V 10% PLATE	26383-602E
C2	CAP CER 1N0 63V 10% PLATE	26383-602E
C3	CAP CER 1N0 63V 10% PLATE	26383-602E
D1	DI H/CARR HP5082-2826	28349-011U
D2	DI H/CARR HP5082-2826	28349-011U
D3	DI H/CARR HP5082-2826	28349-011U
D4	DI H/CARR HP5082-2826	28349-011U
R1	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R2	RES CC 1K0 1/8W 5%	24331-967A
R3	RES CC 120R 1/8W 5%	24331-998K
R4	RES CC 1K0 1/8W 5%	24331-967A
R5	RES CC 120R 1/8W 5%	24331-998K
R6	RES MF 292R 1/4W 1% 100PPM NI	24762-648V
R7	RES MF 17R6 1/4W 1% 100PPM NI	24762-515S
R8	RES MF 292R 1/4W 1% 100PPM NI	24762-648V
R9	RES MF 96R3 1/4W 1% 100PPM NI	24762-582S
R10	RES MF 71R2 1/4W 1% 100PPM NI	24762-572Y
R11	RES MF 96R3 1/4W 1% 100PPM NI	24762-582S
R12	RES MF 122R2 1/4W 1% 100PPM NI	24762-647G
R13	RES MF 122R2 1/4W 1% 100PPM NI	24762-647G
R14	RES MF 247R 1/4W 1% 100PPM NI	24762-631R
R15	RES CHIP 61R1 1%	24681-024W
R16	RES CHIP 53R3 1%	24681-023S
R17	RES MF 790R 1/4W 1% 100PPM NI	24762-646F
R18	RES CHIP 53R3 1%	24681-023S
SA	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SB	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SC	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SD	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SE	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SF	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SH	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SJ	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SK	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SL	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SM	SW MICRO 1CO PLUNGER OPERATED	23483-144G
SN	SW MICRO 1CO PLUNGER OPERATED	23483-144G

Circuit Ref	Description	Part Number
Unit AA2	- 400 MHz input filter assembly	
11.	When ordering, prefix circuit reference with AA2	
	Complete unit	44990-434B
C1	CAP VAR AIR 9P0 1P0 TRIM	26814-502R
C2	CAP VAR AIR 9P0 1P0 TRIM	26814-502R
C3	CAP VAR AIR 14P0 1P0 TRIM	26814-501C
C4	CAP VAR AIR 9P0 1P0 TRIM	26814-502R
C5	CAP VAR AIR 9P0 1P0 TRIM	26814-502R
L2	INDUCTOR	34900-920U
L3	INDUCTOR	34900-919N
L4	INDUCTOR	34900-921Y
L6	INDUCTOR	34900-921Y
L7	INDUCTOR	34900-919N
L8	INDUCTOR	34900-920U
MP1	CHASSIS FILTER	35903-716S
PLAF	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
X1	INS L/T 7/16"LG .0935"HOLE	23211-212W
X2	INS L/T 7/16"LG .0935"HOLE	23211-212W
X3	INS L/T 7/16"LG .0935"HOLE	23211-212W
X4	INS L/T 7/16"LG .0935"HOLE	23211-212W
X5	INS L/T 7/16"LG .0935"HOLE	23211-212W

Circuit Ref	Description	Part Number
Board AA2a	- Input mixer	
12.	When ordering, prefix circuit reference with AA2a	
	Complete unit	44828-451N
C1	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C2	CAP CER 4N7 63V 10% PLATE	26383-591B
C3	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C4	CAP CER 2P2 63V .5PF PLATE	26343-457R
C5	CAP ELEC 10U 40V 10%+ REV RAD	26417-302E
C6	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C7	CAP CER 4N7 63V 10% PLATE	26383-591B
C8	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C9	CAP CER 4N7 63V 10% PLATE	26383-591B
C10	CAP CER 4N7 63V 10% PLATE	26383-591B
C11	CAP CER 4N7 63V 10% PLATE	26383-591B
C12	CAP VAR PLAS 5P5 1P4 TRIM	26878-405H
C13	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C14	CAP CER 100N 50V 20% CHIP	26386-758E
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
C16	CAP CER 4N7 63V 10% PLATE	26383-591B
C17	CAP CER 4N7 63V 10% PLATE	26383-591B
C18	CAP CER 4N7 63V 10% PLATE	26383-591B
C20	CAP CER 1P8 63V .5PF PLATE	26343-456C
C21	CAP CER 56P 63V 2% PLATE	26343-585M
C22	CAP CER 2P7 63V .5PF PLATE	26343-458B
C23	CAP CER 56P 63V 2% PLATE	26343-585M
C24	CAP CER 1N0 63V 10% PLATE	26383-585M
C25	CAP CER 39P 63V 5% PLATE	26343-472N
C28	CAP CER 1P0 63V .5P PLATE	26343-502Z
C29	CAP CER 1P8 63V .5PF PLATE	26343-456C
C30	CAP CER 39P 63V 5% PLATE	26343-472N
C31	CAP CER 56P 63V 2% PLATE	26343-474J
C32	CAP CER 2P7 63V .5PF PLATE	26343-458B
C33	CAP CER 27P 63V 5% PLATE	26343-470U
C35	CAP CER 4N7 63V 10% PLATE	26383-591B
C36	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C37	CAP CER 2P2 63V .5PF PLATE	26343-457R
D1	DI SIL 1N3062 75V JUNC	28336-248R
D2	DI SIL 1N3062 75V JUNC	28336-248R
D3	DI PIN 5082-3379 50V	28383-997T
L2	INDUCTOR 20NH UHF	34901-312B

Circuit Ref	Description	Part Number
Board AA2a	- Input mixer	(Contd.)
L3	DAMPED 100NH CHOKE UHF	44190-050n
L5	INDUCTOR 20NH UHF	34900-915H
L6	INDUCTOR 2NH UHF	34900-917U
L7	COIL ASSEMBLY CHOKE UHF	44290-921B
L8	INDUCTOR 2NH UHF	34900-917U
L9	COIL ASSEMBLY CHOKE UHF	44290-921B
L10	INDUCTOR CHOKE GEN	44190-036B
L11	INDUCTOR 20NH UHF	34900-915H
L13	COIL ASSEMBLY CHOKE UHF	44290-921B
R1	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R2	RES CC 1K5 1/8W 5%	24331-959M
R3	RES CC 3K3 1/8W 5%	24331-948G
R4	RES MF 100R 1/4W 2% 100PPM	24773-249J
R5	RES CC 10K 1/8W 5%	24331-972H
R6	RES CC 120R 1/8W 5%	24331-998K
R7	RES CC 39R 1/8W 5%	24331-994M
R8	RES CC 43R 1/8W 5%	24331-995C
R9	RES MF 20R0 1/4W 1% 100PPM NI	24762-518T
R10	RES CC 2K4 1/8W 5%	24331-968Z
R11	RES CC 750R 1/8W 5%	24331-966K
R12	RES CC 200R 1/8W 5%	24331-999A
R13	RES CC 82R 1/8W 5%	24331-996R
R14	RES CC 22R 1/8W 5%	24331-988T
*R15	RES CC 68R 1/8W 5%	24331-979F
*R16	RES CC 68R 1/8W 5%	24331-979F
R20	RES CC 51R 1/8W 5%	24331-989P
R21	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R22	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES CC 1K5 1/8W 5%	24331-959M
R26	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R27	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R28	RES MF 130R 1/4W 2% 100PPM	24773-252J
R29	RES MF 130R 1/4W 2% 100PPM	24773-252J
R30	RES CC 1K5 1/8W 5%	24331-959M
R32	RES CC 10K 1/8W 5%	24331-972H
R33	RES CC 100R 1/8W 5%	24331-997B
R34	RES CC 10K 1/8W 5%	24331-972H
R35	RV CERM 5K0 LIN 1/2W 10%	25748-563F
R36	RES CC 1K0 1/8W 5%	24331-967A

Circuit Ref	Description	Part Number
Board AA2a	- Input mixer	(Contd.)
R37	RES CC 22R 1/8W 5%	24331-988T
R38	RES CC 51R 1/8W 5%	24331-989P
R39	RES MF 56R 1/4W 2% 100PPM	24773-243H
R40	RES CC 27R 1/8W 5%	24331-977L
R41	RES CC 27R 1/8W 5%	24331-977L
R42	RES CC 750R 1/8W 5%	24331-966K
R43	RES CC 1K8 1/8W 5%	24331-947F
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR NSI BFR91A 12V 6G - AMP	28451-694H
TR3	TR NSI BFR91A 12V 6G - AMP	28451-694H
TR5	TR PSI BC307A 45V 130M - GEN	28435-227H
TR6	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR7	TR PSI BC307A 45V 130M - GEN	28435-227H
TR8	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR10	TR NSI BFR96 15V 5G - AMP	28452-171Y
T1	TRANSFORMER ASSEMBLY 1:1 UHF	43590-132K
X1	MOD RF DBM178 DOUBLE BAL MIXER	28531-004H

Unit AA3 - 502.6 MHz BPF

13. When ordering, prefix circuit reference with AA3

Complete unit	44990-441H

Circuit Ref	Description		Part Number
Board AA3a	- Second mixer		
14.	When ordering, prefix circuit reference with AA3a		
	Complete unit		44828-452L
C5	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C6	CAP CER 1P8 63V .5PF PLATE		26343-456C
C7	CAP CER 4P7 63V .5PF PLATE		26343-461B
C8	CAP VAR PLAS 5P5 1P4 TRIM		26878-405H
C9	CAP CER 10N 25V 20% DISC		26383-006C
C10	CAP CER 10N 25V 20% DISC		26383-006C
C11	CAP CER 10N 25V 20% DISC		26383-006C
C12	CAP CER 2P7 63V .5PF PLATE		26343-458B
C13	CAP CER 56P 63V 2% PLATE		26343-474J
C14	CAP CER 5P6 63V .5PF PLATE		26343-462K
C15	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C16	CAP CER 56P 63V 2% PLATE		26343-474J
C17	CAP CER 39P 63V 5% PLATE		26343-472N
C18	CAP CER 39P 63V 5% PLATE		26343-472N
C19	CAP CER 56P 63V 2% PLATE		26343-474J
C20	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C21	CAP CER 39P 63V 5% PLATE		26343-472N
C22	CAP CER 1N0 63V 10% PLATE		26383-585M
C23	CAP CER 1N0 63V 10% PLATE		26383-585M
D3	DI ZEN BAT29 10V 5%	!	28349-014L
D4	DI ZEN BAT29 10V 5%	!	28349-014L
L5	IND CHOKE 1.0UH 10% LAQ		23642-549L
L6	IND CHOKE 10UH 10% LAQ		23642-555G
L7	INDUCTOR CHOKE GEN		44190-036B
L9	INDUCTOR 30NH		34900-916E
L10	INDUCTOR 30NH		34900-916E
L11	INDUCTOR 20NH UHF		34900-915H
L12	INDUCTOR CHOKE GEN		44190-036B
L13	INDUCTOR CHOKE GEN		44190-036B
R1	RES CC 2K2 1/8W 5%		24331-983G
R2	RES CC 2K2 1/8W 5%		24331-983G
R3	RES MF 5K6 1/4W 2% 100PPM		24773-291S
R4	RES MF 9K1 1/4W 2% 100PPM		24773-296X
R5	RES MF 470R 1/4W 2% 100PPM		24773-265M

Circuit Ref	Description		Part Number
Board AA3a	- Second mixer		(Contd.)
R6	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R7	RES CC 2K4 1/8W 5%		24331-968Z
R8	RES CC 47R 1/8W 5%		24331-975Y
R9	RES CC 4K7 1/8W 5%		24331-970A
R10	RES CC 1KO 1/8W 5%		24331-967A
R11	RES CC 39OR 1/8W 5%		24331-963C
R12	RES CC 68R 1/8W 5%		24331-979F
R13	RES CC 2K4 1/8W 5%		24331-968Z
R14	RES CC 4K7 1/8W 5%		24331-970A
R15	RES CC 1KO 1/8W 5%		24331-967A
R16	RES CC 39OR 1/8W 5%		24331-963C
R17	RES CC 47R 1/8W 5%		24331-975Y
R19	RES CC 4K7 1/8W 5%		24331-970A
R20	RES CC 1KO 1/8W 5%		24331-967A
R21	RES CC 22OR 1/8W 5%		24331-976N
R22	RES CC 2K4 1/8W 5%		24331-968Z
TR1	TR NMF BF960 20V 450M DG	!	28459-054R
TR2	TR NSI BFR90 15V 5G - AMP		28452-167U
TR3	TR NSI BFR90 15V 5G - AMP		28452-167U
TR4	TR NSI BFR90 15V 5G - AMP		28452-167U
TR5	TR PSI BC308B 20V 130M GEN		28433-455R

Circuit Ref	Description		Part Number
Board AA4	- Sampling gate		
15.	When ordering, prefix circuit reference with AA4		
	Complete unit		44828-453J
C1	CAP ELEC 22U 100V 20%+ AX		26415-807Z
C2	CAP ELEC 22U 25V 20%+ AX		26415-805K
C3	CAP ELEC 220U 16V 20%+ PCB		26421-124G
C4	CAP ELEC 22U 25V 20%+ AX		26415-805K
C5	CAP ELEC 22U 25V 20%+ AX		26415-805K
C6	CAP CER 2P7 63V .5PF PLATE		26343-458B
C7	CAP CER 56P 63V 2% PLATE		26343-474J
C8	CAP CER 2P7 63V .5PF PLATE		26343-458B
C9	CAP CER 56P 63V 2% PLATE		26343-474J
C10	CAP CER 1N0 63V 10% PLATE		26383-585M
C11	CAP CER 39P 63V 5% PLATE		26343-472N
C12	CAP CER 1N0 63V 10% PLATE		26383-585M
C13	CAP PETP 10N 400V 10% RAD		26582-232W
C14	CAP PETP 10N 400V 10% RAD		26582-232W
C15	CAP CER 5P6 63V .5PF PLATE		26343-462K
C16	CAP CER 56P 63V 2% PLATE		26343-474J
C17	CAP CER 47P 63V 5% PLATE		26343-473L
C18	CAP CER 330P 63V 2% PLATE		26343-483D
C19	CAP CER 330P 63V 2% PLATE		26343-483D
C20	CAP CER 47P 63V 5% PLATE		26343-473L
C22	CAP CER 10N 25V 20% DISC		26383-006C
C23	CAP CER 10N 25V 20% DISC		26383-006C
C24	CAP CER 10N 25V 20% DISC		26383-006C
C25	CAP CER 12P 63V 5% PLATE		26343-466E
C26	CAP CER 12P 63V 5% PLATE		26343-466E
C27	CAP CER 12P 63V 5% PLATE		26343-466E
C28	CAP CER 12P 63V 5% PLATE		26343-466E
C29	CAP ELEC 22U 25V 20% SUBMIN		26421-114E
C30	CAP ELEC 22U 25V 20%+ AX		26415-805K
C31	CAP PETP 1U0 100V 10% RAD		26582-217U
C32	CAP CER 1N0 63V 10% PLATE		26383-585M
C33	CAP CER 15P 63V 5% PLATE		26343-467U
C34	CAP CER 100P 63V 2% PLATE		26343-477V
C35	CAP CER 15P 63V 5% PLATE		26343-467U
C36	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C37	CAP CER 1N0 63V 10% PLATE		26383-585M
D1	DI H/CARR BAT29 5V	!	28349-014L
D2	DI H/CARR BAT29 5V	!	28349-014L

Circuit Ref	Description		Part Number
Board AA4	- Sampling gate		(Contd.)
D3	DI H/CARR BAT29 5V	!	28349-014L
D4	DI H/CARR BAT29 5V	!	28349-014L
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI STEP 5082-0180		28383-998P
D7	DI H/CARR BAT29 5V	!	28349-014L
D8	DI SIL 1N4148 75V JUNC		28336-676J
D9	DI SIL 1N4148 75V JUNC		28336-676J
D10	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC2	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC3	ICD CTR 74S196 4BIT DEC		28464-010J
IC4	ICA COMP LM339N QUAD		28461-693H
IC5	ICA AMP TL072CP DUAL FET I/P		28461-348Z
L2	INDUCTOR 30NH		34900-916E
L3	INDUCTOR CHOKE GEN		44190-036B
L4	INDUCTOR CHOKE GEN		44190-036B
L5	INDUCTOR CHOKE GEN		44190-036B
L6	IND CHOKE 680UH 10% LAQ		23642-566M
L7	IND		34900-914Z
L8	IND		34900-914Z
L9	IND CHOKE .68UH 10% LAQ		23642-548N
L10	IND CHOKE .1UH 20% LAQ		23642-543Z
L11	IND CHOKE .68UH 10% LAQ		23642-548N
L12	IND CHOKE 1.0UH 10% LAQ		36342-549L
MP2	CORE RING .079X.158X.039"LG		23635-404Y
MP5	CORE RING 6.0X3.0X3.8 FERR		23635-908K
R1	RES MF 10R 1/4W 2% 100PPM		24773-225W
R2	RES MF 10R 1/4W 2% 100PPM		24773-225W
R3	RES MF 1R0 1/4W 2% 100PPM		24773-201M
R4	RES MF 10R 1/4W 2% 100PPM		24773-225W
R5	RES MF 10R 1/4W 2% 100PPM		24773-225W
R6	RES CC 15R 1/8W 5%		24331-942U
R7	RES CC 82R 1/8W 5%		24331-996R
R8	RES CC 15R 1/8W 5%		24331-942U
R9	RES CC 47R 1/8W 5%		24331-975Y
R10	RES CC 4K7 1/8W 5%		24331-970A
R11	RES CC 3K6 1/8W 5%		24331-938E
R12	RES CC 390R 1/8W 5%		24331-963C
R13	RES CC 68R 1/8W 5%		24331-979F

Circuit Ref	Description	Part Number
Board AA4	- Sampling gate	(Contd.)
R14	RES CC 4K7 1/8W 5%	24331-970A
R15	RES CC 4K3 1/8W 5%	24331-956T
R16	RES CC 220R 1/8W 5%	24331-976N
R17	RES CC 150R 1/8W 5%	24331-990D
R18	RES CC 1KO 1/8W 5%	24331-967A
R19	RES CC 1KO 1/8W 5%	24331-967A
R20	RES MF 10K 1/4W 2% 100PPM	24773-297M
R21	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R24	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R26	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R27	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R28	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R29	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R30	RES MF 330R 1/4W 2% 100PPM	24773-261D
R31	RES MF 470R 1/4W 2% 100PPM	24773-265M
R32	RES MF 150R 1/4W 2% 100PPM	24773-253F
R33	RES MF 100R 1/4W 2% 100PPM	24773-249J
R34	RES CC 100R 1/8W 5%	24331-997B
R35	RES MF 200R 1/4W 2% 100PPM	24773-256S
R36	RES MF 200R 1/4W 2% 100PPM	24773-256S
R37	RES MF 200R 1/4W 2% 100PPM	24773-256S
R38	RES MF 100R 1/4W 2% 100PPM	24773-249J
R39	RES MF 200R 1/4W 2% 100PPM	24773-256S
R40	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R41	RES MF 300R 1/4W 2% 100PPM	24773-260W
R42	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R43	RES MF 27K 1/4W 2% 100PPM	24773-307K
R44	RES MF 12K 1/4W 2% 100PPM	24773-299R
R45	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R46	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R47	RES MF 100K 1/4W 2% 100PPM	24773-321L
R48	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R49	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R50	RES MF 270K 1/4W 2% 100PPM	24773-331D
R51	RES MF 9K1 1/4W 2% 100PPM	24773-296X
R52	RES MF 75K 1/4W 2% 100PPM	24773-318L
R53	RES MF 22K 1/4W 2% 100PPM	24773-305R
R54	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R55	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R56	RES MF 10R 1/4W 2% 100PPM	24773-225W
R57	RES MF 100R 1/4W 2% 100PPM	24773-249J

Circuit Ref	Description	Part Number
Board AA4	- Sampling gate	(Contd.)
R58	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R59	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R60	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R61	RES MF 10K 1/4W 2% 100PPM	24773-297M
R62	RES MF 10K 1/4W 2% 100PPM	24773-297M
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR3	TR NJF 2N4857 40V - 20MA 40R	28459-051X
TR4	TR NJF 2N4857 40V - 20MA 40R	28459-051X
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NSI BFY90 15V 1G - AMP	28452-157R
TR7	TR NSI BFY90 15V 1G - AMP	28452-157R
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR9	TR NSI BC237A 45V 150M - GEN	28455-421X
TR10	TR NJF 2N4857 40V - 20MA 40R	28459-051X
TR11	TR NSI BC449 100V 250M	28457-821N
TR12	TR NSI BC449 100V 250M	28457-821N
TR13	TR NSI BC449 100V 250M	28457-821N
TR14	TR NSI BC449 100V 250M	28457-821N
T1	BALUN TRANS	43590-114G
T2	PULSE TRANS	43590-121D

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	
16.	When ordering, prefix circuit reference with AA5	
	Complete unit	44828-454F
C1	CAP PETP 470N 63V 10% RAD	26582-410P
C3	CAP CER 1N0 63V 10% PLATE	26383-585M
C4	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C5	CAP CER 1N0 63V 10% PLATE	26383-585M
C6	CAP CER 1N0 50V 20% CHIP	26386-751C
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
C8	CAP CER 3P9 63V .5PF PLATE	26343-460R
C9	CAP CER 2P2 63V .5PF PLATE	26343-457R
C10	CAP TANT 10U 35V 20% BEAD	26486-225C
C11	CAP CER 1N0 63V 10% PLATE	26383-585M
C12	CAP CER 1N0 50V 20% CHIP	26386-751C
C13	CAP CER 1P8 63V .5PF PLATE	26343-456C
C14	CAP CER 2P7 63V .5PF PLATE	26343-458B
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
C16	CAP CER 1N0 63V 10% PLATE	26383-585M
C17	CAP CER 56P 63V 2% PLATE	26343-474J
C18	CAP CER 39P 63V 5% PLATE	26343-472N
C19	CAP CER 3P9 63V .5PF PLATE	26343-460R
C20	CAP CER 56P 63V 2% PLATE	26343-474J
C21	CAP CER 2P7 63V .5PF PLATE	26343-458B
C22	CAP CER 1N0 63V 10% PLATE	26383-585M
C23	CAP CER 56P 63V 2% PLATE	26343-474J
C24	CAP CER 2P7 63V .5PF PLATE	26343-458B
C25	CAP CER 1N0 63V 10% PLATE	26383-585M
C26	CAP CER 39P 63V 5% PLATE	26343-472N
C27	CAP CER 56P 63V 2% PLATE	26343-474J
C28	CAP CER 5P6 63V .5PF PLATE	26343-462K
C29	CAP CER 1N0 63V 10% PLATE	26383-585M
C30	CAP CER 1N0 63V 10% PLATE	26383-585M
C31	CAP CER 39P 63V 5% PLATE	26343-472N
C32	CAP CER 3P9 63V .5PF PLATE	26343-460R
C33	CAP CER 56P 63V 2% PLATE	26343-474J
C34	CAP CER 2P7 63V .5PF PLATE	26343-458B
C35	CAP CER 1N0 63V 10% PLATE	26383-585M
C36	CAP CER 56P 63V 2% PLATE	26343-474J
C37	CAP CER 2P7 63V .5PF PLATE	26343-458B
C38	CAP CER 1N0 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	(Contd.)
C39	CAP CER 39P 63V 5% PLATE	26343-472N
C40	CAP CER 56P 63V 2% PLATE	26343-474J
C41	CAP CER 2P7 63V .5PF PLATE	26343-458B
C42	CAP CER 1N0 63V 10% PLATE	26383-585M
C43	CAP CER 56P 63V 2% PLATE	26343-474J
C44	CAP CER 2P7 63V .5PF PLATE	26343-458B
C45	CAP CER 1N0 63V 10% PLATE	26383-585M
C46	CAP CER 39P 63V 5% PLATE	26343-472N
C47	CAP ELEC 22U 100V 20%+ AX	26415-807Z
C48	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C49	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C50	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C51	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C52	CAP CER 100P 63V 2% PLATE	26343-477V
C53	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C54	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C55	CAP CER 100P 63V 2% PLATE	26343-477V
C56	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C57	CAP CER 1N0 500V 20% DISC	26383-242P
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI V/CAP BB405B 3V 11.5PF	28381-101V
D9	DI V/CAP BB405B 3V 11.5PF	28381-101V
D10	DI V/CAP BB405B 3V 11.5PF	28381-101V
IC1	ICA VREG UA723C PROG DIL14	28461-706F
IC2	ICA VREG UA723C PROG DIL14	28461-706F
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR 30NH	34900-916E
L7	INDUCTOR 30NH	34900-916E
L8	INDUCTOR CHOKE GEN	44190-036B
L9	INDUCTOR 30NH	34900-916E
L10	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR CHOKE GEN	44190-036B
L13	INDUCTOR 30NH	34900-916E
L14	INDUCTOR CHOKE GEN	44190-036B

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	(Contd.)
L16	INDUCTOR CHOKE GEN	44190-036B
L17	INDUCTOR 30NH	34900-916E
L18	INDUCTOR 30NH	34900-916E
L19	INDUCTOR CHOKE GEN	44190-036B
L21	INDUCTOR CHOKE GEN	44190-036B
L22	INDUCTOR 30NH	34900-916E
L23	INDUCTOR 30NH	34900-916E
L24	INDUCTOR CHOKE GEN	44190-036B
R1	RES MF 15K 1/4W 2% 100PPM	24773-301P
R2	RES MF 15K 1/4W 2% 100PPM	24773-301P
R3	RES MF 15K 1/4W 2% 100PPM	24773-301P
R4	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R5	RES MF 75K 1/4W 2% 100PPM	24773-318L
R6	RES MF 10K 1/4W 2% 100PPM	24773-297M
R7	RES MF 15K 1/4W 2% 100PPM	24773-301P
R8	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R9	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R10	RES MF 7K5 1/4W 2% 100PPM	24773-294T
R11	RES MF 18K 1/4W 2% 100PPM	24773-303M
R12	RES MF 27K 1/4W 2% 100PPM	24773-307K
R13	RES MF 39K 1/4W 2% 100PPM	24773-311A
R14	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R15	RES MF 68K 1/4W 2% 100PPM	24773-317N
R16	RES MF 20K 1/4W 2% 100PPM	24773-304C
R17	RES MF 330R 1/4W 2% 100PPM	24773-261D
R18	RES MF 510R 1/4W 2% 100PPM	24773-266C
R19	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R20	RES MF 200R 1/4W 2% 100PPM	24773-256S
R21	RES MF 220R 1/4W 2% 100PPM	24773-257W
R22	RES MF 100R 1/4W 2% 100PPM	24773-249J
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 62R 1/4W 2% 100PPM	24773-244E
R26	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R27	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R30	RES CC 1K0 1/8W 5%	24331-967A
R31	RES CC 100K 1/8W 5%	24331-980L
R32	RES CC 100K 1/8W 5%	24331-980L

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	(Contd.)
R33	RES CC 100K 1/8W 5%	24331-980L
R34	RES CC 1KO 1/8W 5%	24331-967A
R35	RV CERM 2KO LIN .5W 10% HORZ	25711-639V
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES CC 1KO 1/8W 5%	24331-967A
R38	RES CC 220R 1/8W 5%	24331-976N
R39	RES MF 910R 1/4W 2% 100PPM	24773-272K
R40	RES MF 110R 1/4W 2% 100PPM	24773-250N
R41	RES CC 68R 1/8W 5%	24331-979F
R42	RES CC 3K3 1/8W 5%	24331-948G
R43	RES CC 6K2 1/8W 5%	24331-971Z
R44	RES CC 390R 1/8W 5%	24331-963C
R45	RES CC 68R 1/8W 5%	24331-979F
R47	RES CC 120R 1/8W 5%	24331-998K
R48	RES CC 30R 1/8W 5%	24331-939U
R49	RES CC 30R 1/8W 5%	24331-939U
R50	RES CC 27R 1/8W 5%	24331-977L
R51	RES CC 47R 1/8W 5%	24331-975Y
R52	RES CC 4K7 1/8W 5%	24331-970A
R53	RES CC 3K3 1/8W 5%	24331-948G
R54	RES CC 470R 1/8W 5%	24331-964R
R55	RES CC 47R 1/8W 5%	24331-975Y
R56	RES CC 4K7 1/8W 5%	24331-970A
R57	RES CC 3K6 1/8W 5%	24331-938E
R58	RES CC 270R 1/8W 5%	24331-992P
R59	RES CC 47R 1/8W 5%	24331-975Y
R61	RES CC 47R 1/8W 5%	24331-975Y
R62	RES CC 4K7 1/8W 5%	24331-970A
R63	RES CC 3K3 1/8W 5%	24331-948G
R64	RES CC 270R 1/8W 5%	24331-992P
R65	RES CC 47R 1/8W 5%	24331-975Y
R67	RES CC 120R 1/8W 5%	24331-998K
R68	RES CC 10R 1/8W 5%	24331-974U
R69	RES CC 150R 1/8W 5%	24331-990D
R70	RES CC 10R 1/8W 5%	24331-974U
R71	RES CC 47R 1/8W 5%	24331-975Y
R72	RES CC 4K7 1/8W 5%	24331-970A
R73	RES CC 3K3 1/8W 5%	24331-948G
R74	RES CC 330R 1/8W 5%	24331-945L
R75	RES CC 47R 1/8W 5%	24331-975Y
R76	RES CC 4K7 1/8W 5%	24331-970A

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	(Contd.)
R77	RES CC 3K6 1/8W 5%	24331-938E
R78	RES CC 200R 1/8W 5%	24331-999A
R79	RES CC 47R 1/8W 5%	24331-975Y
R81	RES CC 10R 1/8W 5%	24331-974U
R82	RES CC 150R 1/8W 5%	24331-990D
R83	RES CC 10R 1/8W 5%	24331-974U
R84	RES CC 47R 1/8W 5%	24331-975Y
R85	RES CC 4K7 1/8W 5%	24331-970A
R86	RES CC 3K3 1/8W 5%	24331-948G
R87	RES CC 330R 1/8W 5%	24331-945L
R88	RES CC 47R 1/8W 5%	24331-975Y
R89	RES CC 4K7 1/8W 5%	24331-970A
R90	RES CC 3K6 1/8W 5%	24331-938E
R91	RES CC 200R 1/8W 5%	24331-999A
R92	RES CC 47R 1/8W 5%	24331-975Y
R93	RES CC 120R 1/8W 5%	24331-998K
R94	RES MF 10R 1/4W 2% 100PPM	24773-225W
R95	RES MF 5R1 1/4W 2% 100PPM	24773-218F
R96	RES MF 10R 1/4W 2% 100PPM	24773-225W
R97	RES MF 10R 1/4W 2% 100PPM	24773-225W
R98	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R99	RES MF 10R 1/4W 2% 100PPM	24773-225W
R100	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R101	RES MF 12K 1/4W 2% 100PPM	24773-299R
R102	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R103	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R104	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R105	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R106	RES MF 12K 1/4W 2% 100PPM	24773-299R
R107	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R108	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R109	RES CC 10R 1/8W 5%	24331-974U
TR1	TR NSI BC449 100V 250M	28457-821N
TR2	TR NSI BC449 100V 250M	28457-821N
TR3	TR NSI BC449 100V 250M	28457-821N
TR4	TR NSI BC449 100V 250M	28457-821N
TR6	TR NSI BFR90 15V 5G - AMP	28452-167U
TR7	TR NSI BFR90 15V 5G - AMP	28452-167U
TR8	TR NSI BFR90 15V 5G - AMP	28452-167U
TR9	TR NSI BFR90 15V 5G - AMP	28452-167U
TR10	TR NSI BFR90 15V 5G - AMP	28452-167U
TR11	TR NSI BFR90 15V 5G - AMP	28452-167U
TR12	TR NSI BFR90 15V 5G - AMP	28452-167U

Circuit Ref	Description	Part Number
Board AA5	- Master VCO	(Contd.)
TR13	TR NSI BFR90 15V 5G - AMP	28452-167U
TR14	TR NSI BFR90 15V 5G - AMP	28452-167U
TR15	TR PSI BC307A 45V 130M - GEN	28435-227H
TR16	TR NSI BC237A 45V 150M - GEN	28455-421X
T1	TRIFILAR MATCHING TRANS	43590-130R
T2	BIFILAR OUTPUT TRANS	43590-128B
T3	TRIFILAR MATCHING TRANS	43590-130R
T4	BIFILAR OUTPUT TRANS	43590-128B

Circuit Ref	Description	Part Number
Board AA6	- Divider	
17.	When ordering, prefix circuit reference with AA6	
	Complete unit	44828-455G
C1	CAP CER 2P7 63V .5PF PLATE	26343-458B
C2	CAP CER 56P 63V 2% PLATE	26343-474J
C3	CAP CER 2P7 63V .5PF PLATE	26343-458B
C4	CAP CER 56P 63V 2% PLATE	26343-474J
C5	CAP CER 39P 63V 5% PLATE	26343-472N
C6	CAP CER 1NO 63V 10% PLATE	26383-585M
C7	CAP CER 1NO 63V 10% PLATE	26383-585M
C8	CAP CER 1NO 63V 10% PLATE	26383-585M
C9	CAP CER 1NO 63V 10% PLATE	26383-585M
C10	CAP CER 1NO 63V 10% PLATE	26383-585M
C11	CAP PETP 10N 400V 10% RAD	26582-232W
C12	CAP PETP 10N 400V 10% RAD	26582-232W
C13	CAP PETP 10N 400V 10% RAD	26582-232W
C14	CAP ELEC 22U 25V 20%+ AX	26415-805K
C15	CAP ELEC 22U 25V 20%+ AX	26415-805K
C16	CAP ELEC 22U 25V 20%+ AX	26415-805K
IC1	ICD DIV SP8755 /64 1.2GHZ	28469-418S
L2	INDUCTOR 30NH	34900-916E
L3	INDUCTOR 30NH	34900-916E
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR CHOKE GEN	44190-036B
R1	RES CC 36R 1/8W 5%	24331-936Z
R2	RES CC 22R 1/8W 5%	24331-988T
R3	RES CC 36R 1/8W 5%	24331-936Z
R4	RES CC 47R 1/8W 5%	24331-975Y
R5	RES CC 4K7 1/8W 5%	24331-970A
R6	RES CC 3K3 1/8W 5%	24331-948G
R7	RES CC 680R 1/8W 5%	24331-984V
R8	RES CC 68R 1/8W 5%	24331-979F
R9	RES CC 4K7 1/8W 5%	24331-970A
R10	RES CC 3K6 1/8W 5%	24331-938E
R11	RES CC 390R 1/8W 5%	24331-963C
R12	RES CC 68R 1/8W 5%	24331-979F
R13	RES MF 18K 1/4W 2% 100PPM	24773-303M
R14	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R15	RES MF 3K6 1/4W 2% 100PPM	24773-286G

Circuit Ref	Description	Part Number
Board AA6	- Divider	(Contd.)
R16	RES MF 10R 1/4W 2% 100PPM	24773-225W
R17	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R18	RES MF 100R 1/4W 2% 100PPM	24773-249J
R19	RES MF 10R 1/4W 2% 100PPM	24773-225W
R20	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R21	RES MF 10R 1/4W 2% 100PPM	24773-225W
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR90 15V 5G - AMP	28452-167U
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R

Circuit Ref	Description	Part Number
Board AA7	- Slave VCO	
18.	When ordering, prefix circuit reference with AA7	
	Complete unit	44828-456V
C1	CAP CER 1N0 63V 10% PLATE	26383-585M
C2	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C3	CAP CER 1N0 63V 10% PLATE	26383-585M
C4	CAP CER 1N0 50V 20% CHIP	26386-751C
C5	CAP CER 1N0 63V 10% PLATE	26383-585M
C6	CAP CER 3P9 63V .5PF PLATE	26343-460R
C7	CAP CER 2P2 63V .5PF PLATE	26343-457R
C8	CAP TANT 10U 35V 20% BEAD	26486-225C
C9	CAP CER 1N0 63V 10% PLATE	26383-585M
C10	CAP CER 1N0 50V 20% CHIP	26386-751C
C11	CAP CER 1P8 63V .5PF PLATE	26343-456C
C12	CAP CER 2P7 63V .5PF PLATE	26343-458B
C13	CAP CER 1N0 63V 10% PLATE	26383-585M
C14	CAP CER 1N0 63V 10% PLATE	26383-585M
C15	CAP CER 56P 63V 2% PLATE	26343-474J
C16	CAP CER 39P 63V 5% PLATE	26343-472N
C17	CAP CER 3P9 63V .5PF PLATE	26343-460R
C18	CAP CER 56P 63V 2% PLATE	26343-474J
C19	CAP CER 5P6 63V .5PF PLATE	26343-462K
C20	CAP CER 1N0 63V 10% PLATE	26383-585M
C21	CAP CER 1N0 63V 10% PLATE	26383-585M
C22	CAP CER 39P 63V 5% PLATE	26343-472N
C23	CAP CER 3P9 63V .5PF PLATE	26343-460R
C24	CAP CER 56P 63V 2% PLATE	26343-474J
C25	CAP CER 2P7 63V .5PF PLATE	26343-458B
C26	CAP CER 1N0 63V 10% PLATE	26383-585M
C27	CAP CER 56P 63V 2% PLATE	26343-474J
C28	CAP CER 2P7 63V .5PF PLATE	26343-458B
C29	CAP CER 1N0 63V 10% PLATE	26383-585M
C30	CAP CER 39P 63V 5% PLATE	26343-472N
C31	CAP CER 56P 63V 2% PLATE	26343-474J
C32	CAP CER 2P7 63V .5PF PLATE	26343-458B
C33	CAP CER 1N0 63V 10% PLATE	26383-585M
C34	CAP CER 56P 63V 2% PLATE	26343-474J
C35	CAP CER 2P7 63V .5PF PLATE	26343-458B
C36	CAP CER 1N0 63V 10% PLATE	26383-585M
C37	CAP CER 39P 63V 5% PLATE	26343-472N

Circuit Ref	Description	Part Number
Board AA7	- Slave VCO	(Contd.)
C38	CAP ELEC 22U 100V 20%+ AX	26415-807Z
C39	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C40	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C41	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C42	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C43	CAP CER 100P 63V 2% PLATE	26343-477V
C44	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C45	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C46	CAP CER 100P 63V 2% PLATE	26343-477V
C47	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C48	CAP CER 1N0 500V 20% DISC	26383-242P
C49	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C50	CAP PETP 47N 63V 10% RAD MIN	26582-428J
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI V/CAP BB405B 3V 11.5PF	28381-101V
D9	DI V/CAP BB405B 3V 11.5PF	28381-101V
D10	DI V/CAP BB405B 3V 11.5PF	28381-101V
IC1	ICA VREG UA723C PROG DIL14	28461-706F
IC2	ICA VREG UA723C PROG DIL14	28461-706F
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR 30NH	34900-916E
L7	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR 30NH	34900-916E
L9	INDUCTOR CHOKE GEN	44190-036B
L11	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR 30NH	34900-916E
L13	INDUCTOR 30NH	34900-916E
L14	INDUCTOR CHOKE GEN	44190-036B
L16	INDUCTOR CHOKE GEN	44190-036B
L17	INDUCTOR 30NH	34900-916E
L18	INDUCTOR 30NH	34900-916E
L19	INDUCTOR CHOKE GEN	44190-036B

Circuit Ref	Description	Part Number
Board AA7	- Slave VCO	(Contd.)
R1	RES MF 15K 1/4W 2% 100PPM	24773-301P
R2	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R3	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R4	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R5	RES MF 75K 1/4W 2% 100PPM	24773-318L
R6	RES MF 10K 1/4W 2% 100PPM	24773-297M
R7	RES MF 15K 1/4W 2% 100PPM	24773-301P
R8	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R9	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R10	RES MF 7K5 1/4W 2% 100PPM	24773-294T
R11	RES MF 18K 1/4W 2% 100PPM	24773-303M
R12	RES MF 27K 1/4W 2% 100PPM	24773-307K
R13	RES MF 39K 1/4W 2% 100PPM	24773-311A
R14	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R15	RES MF 68K 1/4W 2% 100PPM	24773-317N
R16	RES MF 20K 1/4W 2% 100PPM	24773-304C
R17	RES MF 330R 1/4W 2% 100PPM	24773-261D
R18	RES MF 510R 1/4W 2% 100PPM	24773-266C
R19	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R20	RES MF 200R 1/4W 2% 100PPM	24773-256S
R21	RES MF 220R 1/4W 2% 100PPM	24773-257W
R22	RES MF 100R 1/4W 2% 100PPM	24773-249J
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 20K 1/4W 2% 100PPM	24773-304C
R25	RES CC 1KO 1/8W 5%	24331-967A
R26	RES CC 100K 1/8W 5%	24331-980L
R27	RES CC 100K 1/8W 5%	24331-980L
R28	RES CC 100K 1/8W 5%	24331-980L
R29	RES CC 1KO 1/8W 5%	24331-967A
R30	RV CERM 2KO LIN .5W 10% HORZ	25711-639V
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES CC 1KO 1/8W 5%	24331-967A
R33	RES CC 220R 1/8W 5%	24331-976N
R34	RES MF 910R 1/4W 2% 100PPM	24773-272K
R35	RES MF 110R 1/4W 2% 100PPM	24773-250N
R36	RES CC 68R 1/8W 5%	24331-979F
R37	RES CC 3K3 1/8W 5%	24331-948G
R38	RES CC 8K2 1/8W 5%	24331-952V
R39	RES CC 390R 1/8W 5%	24331-963C
R40	RES CC 68R 1/8W 5%	24331-979F

Circuit Ref	Description	Part Number
Board AA7	- Slave VCO	(Contd.)
R41	RES CC 120R 1/8W 5%	24331-998K
R42	RES CC 120R 1/8W 5%	24331-998K
R43	RES CC 47R 1/8W 5%	24331-975Y
R44	RES CC 120R 1/8W 5%	24331-998K
R45	RES CC 47R 1/8W 5%	24331-975Y
R46	RES CC 4K7 1/8W 5%	24331-970A
R48	RES CC 3K3 1/8W 5%	24331-948G
R49	RES CC 270R 1/8W 5%	24331-992P
R50	RES CC 47R 1/8W 5%	24331-975Y
R52	RES CC 120R 1/8W 5%	24331-998K
R53	RES CC 10R 1/8W 5%	24331-974U
R54	RES CC 150R 1/8W 5%	24331-990D
R55	RES CC 10R 1/8W 5%	24331-974U
R56	RES CC 47R 1/8W 5%	24331-975Y
R57	RES CC 4K7 1/8W 5%	24331-970A
R58	RES CC 3K3 1/8W 5%	24331-948G
R59	RES CC 330R 1/8W 5%	24331-945L
R60	RES CC 47R 1/8W 5%	24331-975Y
R61	RES CC 4K7 1/8W 5%	24331-970A
R62	RES CC 3K6 1/8W 5%	24331-938E
R63	RES CC 200R 1/8W 5%	24331-999A
R64	RES CC 47R 1/8W 5%	24331-975Y
R65	RES CC 120R 1/8W 5%	24331-998K
R66	RES CC 10R 1/8W 5%	24331-974U
R67	RES CC 150R 1/8W 5%	24331-990D
R68	RES CC 10R 1/8W 5%	24331-974U
R69	RES CC 47R 1/8W 5%	24331-975Y
R70	RES CC 4K7 1/8W 5%	24331-970A
R71	RES CC 3K3 1/8W 5%	24331-948G
R72	RES CC 330R 1/8W 5%	24331-945L
R73	RES CC 47R 1/8W 5%	24331-975Y
R74	RES CC 4K7 1/8W 5%	24331-970A
R75	RES CC 3K6 1/8W 5%	24331-938E
R76	RES CC 200R 1/8W 5%	24331-999A
R77	RES CC 47R 1/8W 5%	24331-975Y
R78	RES CC 120R 1/8W 5%	24331-998K
R79	RES MF 10R 1/4W 2% 100PPM	24773-225W
R80	RES MF 5R1 1/4W 2% 100PPM	24773-218F
R81	RES MF 10R 1/4W 2% 100PPM	24773-225W
R82	RES MF 10R 1/4W 2% 100PPM	24773-225W
R83	RES MF 3K0 1/4W 2% 100PPM	24773-284J

Circuit Ref	Description	Part Number
Board AA7	- Slave VCO	(Contd.)
R84	RES MF 10R 1/4W 2% 100PPM	24773-225W
R85	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R86	RES MF 12K 1/4W 2% 100PPM	24773-299R
R87	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R88	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R89	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R90	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R91	RES MF 12K 1/4W 2% 100PPM	24773-299R
R92	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R93	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R94	RES MF 10K 1/4W 2% 100PPM	24773-297M
R95	RES MF 10K 1/4W 2% 100PPM	24773-297M
R96	RES CC 10R 1/8W 5%	24331-974U
TR1	TR NSI BC449 100V 250M	28457-821N
TR2	TR NSI BC449 100V 250M	28457-821N
TR3	TR NSI BC449 100V 250M	28457-821N
TR4	TR NSI BC449 100V 250M	28457-821N
TR5	TR NSI BFR90 15V 5G - AMP	28452-167U
TR6	TR NSI BFR90 15V 5G - AMP	28452-167U
TR7	TR NSI BFR90 15V 5G - AMP	28452-167U
TR8	TR NSI BFR90 15V 5G - AMP	28452-167U
TR9	TR NSI BFR90 15V 5G - AMP	28452-167U
TR10	TR NSI BFR90 15V 5G - AMP	28452-167U
TR11	TR NSI BFR90 15V 5G - AMP	28452-167U
TR12	TR PSI BC307A 45V 130M - GEN	28435-227H
TR13	TR NSI BC237A 45V 150M - GEN	28455-421X
T1	TRIFILAR MATCHING TRANS	43590-130R
T2	BIFILAR OUTPUT TRANS	43590-128B
T3	TRIFILAR MATCHING TRANS	43590-130R
T4	BIFILAR OUTPUT TRANS	43590-128B

Circuit Ref	Description	Part Number
Board AA8	- Phase detector	
19.	When ordering, prefix circuit reference with AA8	
	Complete unit	44828-457S
C1	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C2	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C3	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C4	CAP ELEC 22U 25V 20% L/LEAK	26421-015N
C5	CAP CER 1NO 63V 10% PLATE	26383-585M
C6	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C7	CAP CER 22P 63V 5% PLATE	26343-469N
C8	CAP CER 22P 63V 5% PLATE	26343-469N
C9	CAP CER 1NO 63V 10% PLATE	26383-585M
C10	CAP CER 1NO 63V 10% PLATE	26383-585M
C11	CAP CER 22P 63V 5% PLATE	26343-469N
C12	CAP CER 1NO 63V 10% PLATE	26383-585M
C13	CAP CER 1NO 63V 10% PLATE	26383-585M
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C15	CAP CER 1NO 63V 10% PLATE	26383-585M
C16	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C17	CAP PETP 1UO 50V 10% RAD MIN	26582-432F
C18	CAP PETP 15N 250V 10% RAD	26582-203P
C19	CAP CER 47P 63V 5% PLATE	26343-473L
C20	CAP CER 2P7 63V .5PF PLATE	26343-458B
C21	CAP CER 56P 63V 2% PLATE	26343-474J
C22	CAP CER 1NO 63V 10% PLATE	26383-585M
C23	CAP CER 2P7 63V .5PF PLATE	26343-458B
C24	CAP CER 1NO 63V 10% PLATE	26383-585M
C25	CAP CER 56P 63V 2% PLATE	26343-474J
C26	CAP CER 39P 63V 5% PLATE	26343-472N
C27	CAP CER 2P7 63V .5PF PLATE	26343-458B
C28	CAP CER 56P 63V 2% PLATE	26343-474J
C29	CAP CER 1NO 63V 10% PLATE	26383-585M
C30	CAP CER 2P7 63V .5PF PLATE	26343-458B
C31	CAP CER 1NO 63V 10% PLATE	26383-585M
C32	CAP CER 56P 63V 2% PLATE	26343-474J
C33	CAP CER 39P 63V 5% PLATE	26343-472N
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	LAMP LED TIL209 3V RED	28624-110P
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA AMP NE5534AN H-PRF DIL8	28461-358J

Circuit Ref	Description	Part Number
Board AA8	- Phase detector	(Contd.)
IC2	ICA MISC 1495L 4QUADR LIN MULT	28461-918D
IC3	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC4	ICA MISC 1495L 4QUADR LIN MULT	28461-918D
L2	INDUCTOR 30NH	34900-916E
L3	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L6	INDUCTOR 30NH	34900-916E
L7	INDUCTOR 30NH	34900-916E
L8	INDUCTOR CHOKE GEN	44190-036B
L9	INDUCTOR CHOKE GEN	44190-036B
R1	RES MF 10R 1/4W 2% 100PPM	24773-225W
R2	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R3	RES MF 10R 1/4W 2% 100PPM	24773-225W
R4	RES MF 10R 1/4W 2% 100PPM	24773-225W
R5	RES MF 62R 1/4W 2% 100PPM	24773-244E
R6	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R9	RES MF 750R 1/4W 2% 100PPM	24773-270R
R10	RES MF 150R 1/4W 2% 100PPM	24773-253F
R11	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R12	RV CERM 100R LIN .5W 10% HORZ	25711-635L
R13	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R14	RES MF 750R 1/4W 2% 100PPM	24773-270R
R15	RES MF 10R 1/4W 2% 100PPM	24773-225W
R16	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R17	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R18	RES MF 120R 1/4W 2% 100PPM	24773-251L
R19	RES MF 10R 1/4W 2% 100PPM	24773-225W
R20	RES MF 100R 1/4W 2% 100PPM	24773-249J
R21	RES MF 100R 1/4W 2% 100PPM	24773-249J
R22	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R23	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R25	RES MF 200R 1/4W 2% 100PPM	24773-256S
R26	RES MF 43R 1/4W 2% 100PPM	24773-240K
R27	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R28	RV CERM 200R LIN .5W 10% HORZ	25711-636J

Circuit Ref	Description	Part Number
Board AA8	- Phase detector	(Contd.)
R29	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R30	RV CERM 200R LIN .5W 10% HORZ	25711-636J
R31	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R32	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R33	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R34	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R35	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R36	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R37	RES MF 10K 1/4W 2% 100PPM	24773-297M
R38	RES MF 10K 1/4W 2% 100PPM	24773-297M
R39	RES MF 10K 1/4W 2% 100PPM	24773-297M
R40	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R41	RES MF 100K 1/4W 2% 100PPM	24773-321L
R42	RES MF 100R 1/4W 2% 100PPM	24773-249J
R43	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R44	RES MF 100K 1/4W 2% 100PPM	24773-321L
R45	RES MG 2M2 1/4W 5%	24321-877J
R46	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R47	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R48	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R49	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R50	RES MF 470R 1/4W 2% 100PPM	24773-265M
R51	RES MF 150K 1/4W 2% 100PPM	24773-325V
R52	RES CC 24R 1/8W 5%	24331-937H
R53	RES CC 36R 1/8W 5%	24331-936Z
R54	RES CC 24R 1/8W 5%	24331-937H
R55	RES CC 47R 1/8W 5%	24331-975Y
R56	RES CC 4K7 1/8W 5%	24331-970A
R57	RES CC 3K6 1/8W 5%	24331-938E
R58	RES CC 390R 1/8W 5%	24331-963C
R59	RES CC 68R 1/8W 5%	24331-979F
R60	RES CC 4K7 1/8W 5%	24331-970A
R61	RES CC 4K3 1/8W 5%	24331-956T
R62	RES CC 220R 1/8W 5%	24331-976N
R63	RES CC 150R 1/8W 5%	24331-990D
R64	RES CC 36R 1/8W 5%	24331-936Z
R65	RES CC 22R 1/8W 5%	24331-988T
R66	RES CC 36R 1/8W 5%	24331-936Z
R67	RES CC 47R 1/8W 5%	24331-975Y
R68	RES CC 4K7 1/8W 5%	24331-970A
R69	RES CC 3K3 1/8W 5%	24331-948G
R70	RES CC 470R 1/8W 5%	24331-964R
R71	RES CC 68R 1/8W 5%	24331-979F

Circuit Ref	Description	Part Number
Board AA8	- Phase detector	(Contd.)
R72	RES CC 4K7 1/8W 5%	24331-970A
R73	RES CC 3K6 1/8W 5%	24331-938E
R74	RES CC 270R 1/8W 5%	24331-992P
R75	RES CC 68R 1/8W 5%	24331-979F
R76	RES MF 220R 1/4W 2% 100PPM	24773-257W
R77	RES MF 220R 1/4W 2% 100PPM	24773-257W
R78	RES MF 750R 1/4W 2% 100PPM	24773-270R
R79	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R80	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R81	RES MF 5K1 1/4W 2% 100PPM	24773-290V
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NJF 2N4857 40V - 20MA 40R	28459-051X
TR3	TR NJF 2N4857 40V - 20MA 40R	28459-051X
TR4	TR NSI BFR90 15V 5G - AMP	28452-167U
TR5	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR6	TR NSI BFR90 15V 5G - AMP	28452-167U
TR7	TR NSI BFR90 15V 5G - AMP	28452-167U
X1	MOD RF SBL-1X DBL BAL MXR 1GHZ	28531-005E

Circuit Ref	Description	Part Number
Board AA9	- Second LO VCO	
20.	When ordering, prefix circuit reference with AA9	
	Complete unit	44828-458W
C1	CAP CER 1NO 63V 10% PLATE	26383-585M
C2	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C3	CAP CER 1NO 50V 20% CHIP	26386-751C
C4	CAP CER 1NO 63V 10% PLATE	26383-585M
C5	CAP CER 1NO 63V 10% PLATE	26383-585M
C6	CAP CER 4P7 63V .5PF PLATE	26343-461B
C7	CAP CER 3P9 63V .5PF PLATE	26343-460R
C8	CAP CER 1NO 63V 10% PLATE	26383-585M
C9	CAP CER 1NO 50V 20% CHIP	26386-751C
C10	CAP TANT 10U 35V 20% BEAD	26486-225C
C11	CAP CER 1P8 63V .5PF PLATE	26343-456C
C12	CAP CER 2P7 63V .5PF PLATE	26343-458B
C13	CAP CER 1NO 63V 10% PLATE	26383-585M
C14	CAP CER 1NO 63V 10% PLATE	26383-585M
C15	CAP CER 56P 63V 2% PLATE	26343-474J
C16	CAP CER 39P 63V 5% PLATE	26343-472N
C17	CAP CER 5P6 63V .5PF PLATE	26343-462K
C18	CAP CER 56P 63V 2% PLATE	26343-474J
C19	CAP CER 1NO 63V 10% PLATE	26383-585M
C20	CAP CER 3P9 63V .5PF PLATE	26343-460R
C21	CAP CER 5P6 63V .5PF PLATE	26343-462K
C22	CAP CER 56P 63V 2% PLATE	26343-474J
C23	CAP CER 1NO 63V 10% PLATE	26383-585M
C24	CAP CER 39P 63V 5% PLATE	26343-472N
C25	CAP CER 1NO 63V 10% PLATE	26383-585M
C26	CAP CER 3P9 63V .5PF PLATE	26343-460R
C27	CAP CER 1NO 63V 10% PLATE	26383-585M
C28	CAP CER 39P 63V 5% PLATE	26343-472N
C30	CAP CER 2P7 63V .5PF PLATE	26343-458B
C31	CAP CER 56P 63V 2% PLATE	26343-474J
C32	CAP CER 1NO 63V 10% PLATE	26383-585M
C33	CAP CER 56P 63V 2% PLATE	26343-474J
C34	CAP CER 2P7 63V .5PF PLATE	26343-458B
C35	CAP CER 1NO 63V 10% PLATE	26383-585M
C36	CAP CER 39P 63V 5% PLATE	26343-472N
C40	CAP CER 2P7 63V .5PF PLATE	26343-458B
C41	CAP CER 56P 63V 2% PLATE	26343-474J

Circuit Ref	Description	Part Number
Board AA9	- Second LO VCO	(Contd.)
C42	CAP CER 1N0 63V 10% PLATE	26383-585M
C43	CAP CER 56P 63V 2% PLATE	26343-474J
C44	CAP CER 2P7 63V .5PF PLATE	26343-458B
C45	CAP CER 1N0 63V 10% PLATE	26383-585M
C46	CAP CER 39P 63V 5% PLATE	26343-472N
C50	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C51	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C52	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C53	CAP CER 100P 63V 2% PLATE	26343-477V
C54	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C55	CAP CER 100P 63V 2% PLATE	26343-477V
C56	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C57	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C58	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
D1	DI V/CAP BB405B 3V 11.5PF	28381-101V
D2	DI V/CAP BB405B 3V 11.5PF	28381-101V
D3	DI V/CAP BB405B 3V 11.5PF	28381-101V
IC1	ICA VREG UA723C PROG DIL14	28461-706F
IC2	ICA VREG UA723C PROG DIL14	28461-706F
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR 30NH	34900-916E
L7	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR CHOKE GEN	44190-036B
L9	INDUCTOR 30NH	34900-916E
L11	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR 30NH	34900-916E
L13	INDUCTOR 30NH	34900-916E
L14	INDUCTOR CHOKE GEN	44190-036B
L16	INDUCTOR 30NH	34900-916E
L17	INDUCTOR CHOKE GEN	44190-036B
L18	INDUCTOR 30NH	34900-916E
L19	INDUCTOR CHOKE GEN	44190-036B
L21	INDUCTOR 30NH	34900-916E
L22	INDUCTOR CHOKE GEN	44190-036B
L23	INDUCTOR CHOKE GEN	44190-036B

Circuit Ref	Description	Part Number
Board AA9	- Second LO VCO	(Contd.)
R1	RES CC 100R 1/8W 5%	24331-997B
R2	RES CC 100K 1/8W 5%	24331-980L
R3	RES CC 100K 1/8W 5%	24331-980L
R4	RES CC 100K 1/8W 5%	24331-980L
R5	RES CC 1K0 1/8W 5%	24331-967A
R6	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R7	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R8	RES CC 1K0 1/8W 5%	24331-967A
R9	RES CC 220R 1/8W 5%	24331-976N
R10	RES MF 910R 1/4W 2% 100PPM	24773-272K
R11	RES MF 110R 1/4W 2% 100PPM	24773-250N
R12	RES CC 120R 1/8W 5%	24331-998K
R13	RES CC 3K3 1/8W 5%	24331-948G
R14	RES CC 390R 1/8W 5%	24331-963C
R15	RES CC 68R 1/8W 5%	24331-979F
R16	RES CC 6K2 1/8W 5%	24331-971Z
R17	RES CC 3K3 1/8W 5%	24331-948G
R18	RES CC 120R 1/8W 5%	24331-998K
R19	RES CC 47R 1/8W 5%	24331-975Y
R20	RES CC 4K7 1/8W 5%	24331-970A
R21	RES CC 270R 1/8W 5%	24331-992P
R22	RES CC 47R 1/8W 5%	24331-975Y
R23	RES CC 4K7 1/8W 5%	24331-970A
R24	RES CC 3K3 1/8W 5%	24331-948G
R25	RES CC 270R 1/8W 5%	24331-992P
R26	RES CC 47R 1/8W 5%	24331-975Y
R27	RES CC 47R 1/8W 5%	24331-975Y
R28	RES CC 120R 1/8W 5%	24331-998K
R29	RES CC 10R 1/8W 5%	24331-974U
R30	RES CC 10R 1/8W 5%	24331-974U
R31	RES CC 150R 1/8W 5%	24331-990D
R32	RES CC 10R 1/8W 5%	24331-974U
R33	RES CC 10R 1/8W 5%	24331-974U
R34	RES CC 150R 1/8W 5%	24331-990D
R35	RES CC 47R 1/8W 5%	24331-975Y
R36	RES CC 3K3 1/8W 5%	24331-948G
R37	RES CC 4K7 1/8W 5%	24331-970A
R38	RES CC 330R 1/8W 5%	24331-945L
R39	RES CC 47R 1/8W 5%	24331-975Y
R40	RES CC 3K6 1/8W 5%	24331-938E
R41	RES CC 4K7 1/8W 5%	24331-970A

Circuit Ref	Description	Part Number
Board AA9	- Second LO VCO	(Contd.)
R42	RES CC 200R 1/8W 5%	24331-999A
R43	RES CC 47R 1/8W 5%	24331-975Y
R44	RES CC 120R 1/8W 5%	24331-998K
R45	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R50	RES CC 47R 1/8W 5%	24331-975Y
R51	RES CC 3K3 1/8W 5%	24331-948G
R52	RES CC 4K7 1/8W 5%	24331-970A
R53	RES CC 330R 1/8W 5%	24331-945L
R54	RES CC 47R 1/8W 5%	24331-975Y
R55	RES CC 3K6 1/8W 5%	24331-938E
R56	RES CC 4K7 1/8W 5%	24331-970A
R57	RES CC 200R 1/8W 5%	24331-999A
R58	RES CC 47R 1/8W 5%	24331-975Y
R59	RES CC 120R 1/8W 5%	24331-998K
R60	RES MF 10R 1/4W 2% 100PPM	24773-225W
R61	RES MF 10R 1/4W 2% 100PPM	24773-225W
R62	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R63	RES MF 10R 1/4W 2% 100PPM	24773-225W
R64	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R65	RES MF 12K 1/4W 2% 100PPM	24773-299R
R66	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R67	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R68	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R69	RES MF 10R 1/4W 2% 100PPM	24773-225W
R70	RES MF 2K0 1/4W 2% 100PPM	24773-280U
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR90 15V 5G - AMP	28452-167U
TR3	TR NSI BFR90 15V 5G - AMP	28452-167U
TR4	TR NSI BFR90 15V 5G - AMP	28452-167U
TR5	TR NSI BFR90 15V 5G - AMP	28452-167U
TR6	TR NSI BFR90 15V 5G - AMP	28452-167U
TR7	TR NSI BFR90 15V 5G - AMP	28452-167U
TR8	TR PSI BC307A 45V 130M - GEN	28435-227H
TR9	TR NSI BFR90 15V 5G - AMP	28452-167U
T1	TRIFILAR MATCHING TRANS	43590-130R
T2	BIFILAR OUTPUT TRANS	43590-128B
T3	TRIFILAR MATCHING TRANS	43590-130R
T4	BIFILAR OUTPUT TRANS	43590-128B

Circuit Ref	Description		Part Number
Board AA10	- Sampling gate		
21.	When ordering, prefix circuit reference with AA10		
	Complete unit		44828-459D
C1	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C2	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C3	CAP CER 2P7 63V .5PF PLATE		26343-458B
C4	CAP CER 1NO 63V 10% PLATE		26383-585M
C5	CAP CER 1NO 63V 10% PLATE		26383-585M
C6	CAP CER 39P 63V 5% PLATE		26343-472N
C7	CAP CER 56P 63V 2% PLATE		26343-474J
C8	CAP CER 3P9 63V .5PF PLATE		26343-460R
C10	CAP CER 4P7 63V .5PF PLATE		26343-461B
C11	CAP CER 22P 63V 5% PLATE		26343-469N
C12	CAP CER 22P 63V 5% PLATE		26343-469N
C13	CAP CER 10P 63V .5PF PLATE		26343-465H
C14	CAP CER 10P 63V .5PF PLATE		26343-465H
C15	CAP CER 4N7 63V 10% PLATE		26383-591B
C16	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C17	CAP CER 4N7 63V 10% PLATE		26383-591B
C18	CAP CER 1NO 63V 10% PLATE		26383-585M
C24	CAP PETP 220N 63V 10% RAD		26582-406T
C26	CAP PETP 220N 63V 10% RAD		26582-406T
C27	CAP PETP 220N 63V 10% RAD		26582-406T
C28	CAP PETP 100N 100V 10% RAD		26582-211B
C29	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
D1	DI H/CARR BAT29 5V	!	28349-014L
D2	DI H/CARR BAT29 5V	!	28349-014L
D3	DI H/CARR BAT29 5V	!	28349-014L
D4	DI H/CARR BAT29 5V	!	28349-014L
D5	DI STEP 5082-0180		28383-998P
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
D8	DI SIL 1N4148 75V JUNC		28336-676J
D9	DI SIL 1N4448 75V JUNC		28336-246M
D10	DI SIL 1N4448 75V JUNC		28336-246M
IC1	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC2	ICA AMP TL074CN QUAD FET I/P		28461-349H
L1	INDUCTOR CHOKE GEN		44190-036B
L3	INDUCTOR CHOKE GEN		44190-036B
L6	IND CHOKE 22UH 10% LAQ		23642-557S
MP2	S/C ACC PAD TO18,ETC TO .1"GRD		28488-115L

Circuit Ref	Description	Part Number
Board AA10	- Sampling gate	(Contd.)
R1	RES MF 10R 1/4W 2% 100PPM	24773-225W
R2	RES MF 10R 1/4W 2% 100PPM	24773-225W
R3	RES CC 47R 1/8W 5%	24331-975Y
R4	RES CC 4K3 1/8W 5%	24331-956T
R5	RES CC 4K7 1/8W 5%	24331-970A
R6	RES CC 220R 1/8W 5%	24331-976N
R7	RES CC 150R 1/8W 5%	24331-990D
R10	RES CC 180R 1/8W 5%	24331-961X
R11	RES MF 10K 1/4W 2% 100PPM	24773-297M
R12	RES MF 10K 1/4W 2% 100PPM	24773-297M
R13	RES CC 100R 1/8W 5%	24331-997B
R14	RES CC 100R 1/8W 5%	24331-997B
R15	RES CC 200R 1/8W 5%	24331-999A
R16	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R17	RES MF 470R 1/4W 2% 100PPM	24773-265M
R18	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R19	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R20	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R21	RES MF 13K 1/4W 2% 100PPM	24773-300T
R22	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R23	RES MF 13K 1/4W 2% 100PPM	24773-300T
R24	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R33	RES MF 10K 1/4W 2% 100PPM	24773-297M
R34	RES MF 11K 1/4W 2% 100PPM	24773-298C
R35	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R38	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R39	RES MF 15K 1/4W 2% 100PPM	24773-301P
R40	RES MF 47R 1/4W 2% 100PPM	24773-241A
R41	RES MF 10R 1/4W 2% 100PPM	24773-225W
TR1	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR2	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NJF 2N4857 40V 40R - 20MA	28459-051X
T1	SAMPLING GATE TRANS	43590-131B

Circuit Ref	Description	Part Number
Board AA11	- Line cleaner	
22.	When ordering, prefix circuit reference with AA11	
	Complete unit	44828-460S
C1	CAP CER 100N 30V 20% DISC	26383-031S
C2	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C3	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C4	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C5	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C6	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C7	CAP CER 100N 30V 20% DISC	26383-031S
C8	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C9	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C10	CAP PETP 470N 63V 10% RAD MIN	26582-427L
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI ZEN BZX79C8V2 8.2V 5%	28371-671E
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI ZEN BZX79C8V2 8.2V 5%	28371-671E
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
D9	DI SIL 1N4148 75V JUNC	28336-676J
D10	DI SIL 1N4148 75V JUNC	28336-676J
D11	DI SIL 1N4148 75V JUNC	28336-676J
D12	DI ZEN BZX79C8V2 8.2V 5%	28371-671E
D13	DI SIL 1N4148 75V JUNC	28336-676J
D14	DI ZEN BZX79C8V2 8.2V 5%	28371-671E
IC1	ICA VREG+ LM317T PROG 1A5	28461-726A
IC2	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC3	ICA VREG- LM337T PROG 1A5	28461-727Z
MP1	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
MP2	S/C ACC BUSH 6BA/M3 INSUL	28488-126T
MP8	S/C ACC PAD TO5,ETC TO 0.1"GRD	28488-113Y
R1	RES MF 240R 1/4W 2% 100PPM	24773-258D
R2	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R3	RES MF 1R8 1/4W 2% 100PPM	24773-207Z
R4	RES MF 82K 1/4W 2% 100PPM	24773-319J
R5	RES MG 10M 1/4W 5%	24321-885W

Circuit Ref	Description	Part Number
Board AA11	- Line cleaner	(Contd.)
R6	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R7	RES MF 47K 1/4W 2% 100PPM	24773-313H
R8	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R9	RES MF 1R8 1/4W 2% 100PPM	24773-207Z
R11	RES MF 1R8 1/4W 2% 100PPM	24773-207Z
R12	RES MF 100K 1/4W 2% 100PPM	24773-321L
R13	RES MG 10M 1/4W 5%	24321-885W
R14	RES MF 27K 1/4W 2% 100PPM	24773-307K
R15	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R16	RES MF 100K 1/4W 2% 100PPM	24773-321L
R17	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R18	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R19	RES MG 10M 1/4W 5%	24321-885W
R20	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R21	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R22	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R23	RES MF 240R 1/4W 2% 100PPM	24773-258D
R24	RES MF 82K 1/4W 2% 100PPM	24773-319J
R25	RES MF 2R4 1/4W 2% 100PPM	24773-210Z
R26	RES MG 10M 1/4W 5%	24321-885W
R27	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R28	RES MF 47K 1/4W 2% 100PPM	24773-313H
R29	RES MF 82R 1/4W 2% 100PPM	24773-247N
R30	RV THERM 47K 20% BEA VA3410	25685-241S
R31	RES MF 1R8 1/4W 2% 100PPM	24773-207Z
TR1	TR PSI BC307A 45V 130M - GEN	28435-227H
TR2	TR PSI 2N2905A 60V 200M - GEN	28435-868C
TR3	TR NSI 2N2219A 40V 300M - GEN	28454-804V
TR4	TR NSI BC209C 20V 150M - GEN	28452-771P

Circuit Ref	Description	Part Number
Unit AB0	- AB tray assembly	
23.	When ordering, prefix circuit reference with AB0	
	Complete unit	44990-466B
C1	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C28	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C36	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C37	CAP CER 22P 300V 10% L/T SOL	26333-226Z

Circuit Ref	Description	Part Number
Unit AB0	- AB tray assembly	(Contd.)
C38	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C39	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C40	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C41	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C42	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C43	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C45	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C49	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C50	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C53	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C57	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C58	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C59	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C60	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C61	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C62	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C63	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C64	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR CHOKE GEN	44190-036B
L3	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR CHOKE GEN	44190-036B
L6	INDUCTOR CHOKE GEN	44190-036B
L7	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR CHOKE GEN	44190-036B
L9	IND CHOKE 100UH 10% LAQ	23642-561W
L10	IND CHOKE 470UH 10% SCREENED	23642-333B
L11	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR CHOKE GEN	44190-036B
L13	INDUCTOR CHOKE GEN	44190-036B
L14	INDUCTOR CHOKE GEN	44190-036B
L15	INDUCTOR CHOKE GEN	44190-036B
L16	INDUCTOR CHOKE GEN	44190-036B

Circuit Ref	Description	Part Number
Unit ABO	- AB tray assembly	(Contd.)
L17	INDUCTOR CHOKE GEN	44190-036B
L18	INDUCTOR CHOKE GEN	44190-036B
L19	INDUCTOR CHOKE GEN	44190-036B
L20	INDUCTOR CHOKE GEN	44190-036B
L21	INDUCTOR CHOKE GEN	44190-036B
L22	INDUCTOR CHOKE GEN	44190-036B
L23	IND CHOKE 47UH 10% LAQ	23642-559D
L24	INDUCTOR CHOKE GEN	23642-036B
L25	INDUCTOR CHOKE GEN	23642-036B
L26	IND CHOKE 47UH 10% LAQ	23642-559D
L27	INDUCTOR	34900-918Y
L28	INDUCTOR 1MH PWR	44190-042Z
L29	INDUCTOR 1MH PWR	44190-042Z
L30	INDUCTOR CHOKE GEN	44190-036B
L31	INDUCTOR CHOKE GEN	44190-036B
	CABLE ASSY 10-WAY RIBBON	43129-961S
	CABLE ASSY MIN COAX	43129-971C

Circuit Ref	Description	Part Number
Board AB1	- D to A converter	
24. When ordering, prefix circuit reference with AB1		
	Complete unit	44828-462D
C1	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C2	CAP CER 10N 25V 20% DISC	26383-006C
C3	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C4	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C5	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C6	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C7	CAP CER 10N 25V 20% DISC	26383-006C
C10	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C11	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C12	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C13	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C15	CAP CER 10N 25V 20% DISC	26383-006C
C16	CAP CER 100P 63V 2% PLATE	26343-477V
C17	CAP CER 47P 63V 5% PLATE	26343-473L
C20	CAP CER 10N 25V 20% DISC	26383-006C
C21	CAP CER 10N 25V 20% DISC	26383-006C
C22	CAP CER 10N 25V 20% DISC	26383-006C
C23	CAP CER 10N 25V 20% DISC	26383-006C
C24	CAP CER 10N 25V 20% DISC	26383-006C
C25	CAP CER 10N 25V 20% DISC	26383-006C
C26	CAP CER 10N 25V 20% DISC	26383-006C
C27	CAP CER 10N 25V 20% DISC	26383-006C
C28	CAP CER 100P 63V 2% PLATE	26343-477V
C30	CAP CER 10N 25V 20% DISC	26383-006C
C31	CAP CER 10N 25V 20% DISC	26383-006C
C32	CAP CER 10N 25V 20% DISC	26383-006C
C33	CAP CER 10N 25V 20% DISC	26383-006C
C34	CAP PETP 2U2 63V 10% RAD	26582-418Z
C35	CAP PETP 2U2 63V 10% RAD	26582-418Z
C36	CAP PETP 1U0 100V 10% RAD	26582-217U
C37	CAP PETP 5U6 63V 10% RAD	26582-423E
C41	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C45	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C46	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C47	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C50	CAP PETP 100N 63V 10% RAD MIN	26582-429F

Circuit Ref	Description	Part Number
Board AB1	- D to A converter	(Contd.)
C51	CAP ELEC 22U 100V 20%+ PCB	26421-120N
C52	CAP ELEC 22U 25V 20% SUBMIN	26421-114E
C53	CAP MICA 33P 350V 1P	26582-391L
C54	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C55	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C60	CAP ELEC 22U 100V 20%+ PCB	26421-120N
C61	CAP ELEC 2U2 50V 20% L/LEAK	26421-009E
C62	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C63	CAP ELEC 22U 100V 20%+ PCB	26421-120N
C64	CAP CER 100P 63V 2% PLATE	26343-477V
C67	CAP CER 47P 63V 5% PLATE	26343-473L
C68	CAP CER 47P 63V 5% PLATE	26343-473L
C69	CAP CER 100P 63V 2% PLATE	26343-477V
C70	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C71	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C72	CAP CER 10N 25V 20% DISC	26383-006C
C73	CAP CER 100P 63V 2% PLATE	26343-477V
C74	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C75	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C76	CAP CER 10N 25V 20% DISC	26383-006C
C77	CAP CER 100P 63V 2% PLATE	26343-477V
C78	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C79	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C80	CAP CER 10N 25V 20% DISC	26383-006C
C81	CAP CER 100P 63V 2% PLATE	26343-477V
C82	CAP ELEC 47U 63V 20%+ PCB	26421-121L
C84	CAP ELEC 470U 16V 20%+ PCB	26421-127W
C90	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C91	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C92	CAP CER 10N 25V 20% DISC	26383-006C
C93	CAP CER 47P 63V 5% PLATE	26343-473L
C94	CAP CER 100P 63V 2% PLATE	26343-477V
C100	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C101	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C102	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C103	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C104	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C105	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C106	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C107	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C108	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C109	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C110	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description		Part Number
Board AB1	- D to A converter		(Contd.)
C111	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C112	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C113	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	LAMP LED TIL209 3V RED		28624-110P
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICA DAC AD7524JN 8BIT	!	28469-400R
IC2	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC3	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC4	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC6	ICA VREG+ LM317T PROG 1A5		28461-726A
IC8	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC9	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC10	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC11	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC12	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC13	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC14	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC15	MOD HYB 80-CBI 12BIT DAC		28541-011L
IC16	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC17	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC18	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC19	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC20	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC21	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC22	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC23	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC24	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC25	ICA COMP LM339N QUAD		28461-693H
IC26	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC27	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC28	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC29	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC30	ICA COMP LM339N QUAD		28461-693H
IC31	ICA COMP LM339N QUAD		28461-693H
IC40	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC41	ICA AMP NE5534AN H-PRF DIL8		28461-358J

Circuit Ref	Description		Part Number
Board AB1	- D to A converter		(Contd.)
C111	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C112	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C113	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	LAMP LED TIL209 3V RED		28624-110P
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICA DAC AD7524JN 8BIT	!	28469-400R
IC2	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC3	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC4	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC6	ICA VREG+ LM317T PROG 1A5		28461-726A
IC8	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC9	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC10	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC11	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC12	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC13	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC14	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC15	MOD HYB 80-CBI 12BIT DAC		28541-011L
IC16	ICA DAC 888FX 8BIT LATCHED I/P		28469-434K
IC17	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC18	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC19	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC20	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC21	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC22	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC23	ICA AMP NE5534AN H-PRF DIL8		28461-358J
IC24	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC25	ICA COMP LM339N QUAD		28461-693H
IC26	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC27	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC28	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC29	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC30	ICA COMP LM339N QUAD		28461-693H
IC31	ICA COMP LM339N QUAD		28461-693H
IC40	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC41	ICA AMP NE5534AN H-PRF DIL8		28461-358J

Circuit Ref	Description	Part Number
Board AB1	- D to A converter	(Contd.)
R54	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R55	RES MF 470R 1/4W 2% 100PPM	24773-265M
R60	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R61	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R62	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R63	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R64	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R65	RES MF 220R 1/4W 2% 100PPM	24773-257W
R66	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R70	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R71	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R72	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R73	RES MF 24K 1/4W 2% 100PPM	24773-306B
R74	RES MF 12K 1/4W 2% 100PPM	24773-299R
R75	RES MF 240R 1/4W 2% 100PPM	24773-258D
R76	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R77	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R78	RES MF 100R 1/4W 2% 100PPM	24773-249J
R80	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R81	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R82	RES MF 75K 1/4W 2% 100PPM	24773-318L
R83	RES MF 10K 1/4W 2% 100PPM	24773-297M
R84	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R85	RES MF 560R 1/4W 2% 100PPM	24773-267R
R86	RES MF 12K 1/4W 0.5% 50PPM	24753-629L
R87	RES MF 3K0 1/4W 0.5% 50PPM	24753-475C
R88	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R89	RES MF 12K 1/4W 2% 100PPM	24773-299R
R90	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R91	RES MF 100R 1/4W 2% 100PPM	24773-249J
R92	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R93	RES MF 10K 1/4W 2% 100PPM	24773-297M
R94	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R95	RES MF 7R5 1/4W 2% 100PPM	24773-222G
R96	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R97	RES MF 130K 1/4W 2% 100PPM	24773-324G
R98	RES MF 10K 1/4W 2% 100PPM	24773-297M
R100	RES MF 27K 1/4W 2% 100PPM	24773-307K
R101	RES MF 12K 1/4W 2% 100PPM	24773-299R
R102	RES MF 2K0 1/4W .1% 50PPM	24723-402G
R103	RES MF 5K0 1/4W .1% 50PPM	24723-401F
R104	RES MF 2K0 1/4W .1% 50PPM	24723-402G
R105	RES MF 2K0 1/4W 2% 100PPM	24773-280U

Circuit Ref	Description	Part Number
Board AB1	- D to A converter (Contd.)	
R106	RES MF 320K 1/4W .1% 50PPM	24723-404S
R107	RES MF 1KO 1/4W .1% 50PPM	24723-403V
R108	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R109	RES MF 5KO 1/4W .1% 50PPM	24723-401F
R110	RES MF 1KO 1/4W .1% 50PPM	24723-403V
R111	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R112	RES MF 320K 1/4W .1% 50PPM	24723-404S
R113	RES MF 100R 1/4W 2% 100PPM	24773-249J
R114	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R115	RES MF 5KO 1/4W .1% 50PPM	24723-401F
R116	RES MF 10K 1/4W 2% 100PPM	24773-297M
R117	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R118	RES MF 20K 1/4W 2% 100PPM	24773-304C
R119	RES MF 20K 1/4W 2% 100PPM	24773-304C
R120	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R121	RES MF 240R 1/4W 2% 100PPM	24773-258D
R122	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R123	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R130	RES NET 220K 2% 8DIL	24681-505W
R131	RES NET 220K 2% 8DIL	24681-505W
SKPD	CON JUMP FEM 2 1 ROW	23435-990X
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR NJF 2N4857 40V 40R - 20MA	28459-051X
TR3	TR NJF 2N4857 40V 40R - 20MA	28459-051X
TR4	TR NSI BC209C 20V 150M - GEN	28452-771P
TR5	TR NSI BC209C 20V 150M - GEN	28452-771P
TR6	TR NJF 2N4857 40V 40R - 20MA	28459-051X
TR7	TR NJF 2N4857 40V 40R - 20MA	28459-051X
TR8	TR NJF 2N4857 40V 40R - 20MA	28459-051X
TR9	TR NSI BC449 100V 250M	28457-821N
TR10	TR NSI BC449 100V 250M	28457-821N
TR11	TR NSI BC449 100V 250M	28457-821N
TR12	TR NSI BC449 100V 250M	28457-821N
TR13	TR NSI BC449 100V 250M	28457-821N
TR14	TR NSI BC449 100V 250M	28457-821N
TR19	TR NSI BC209C 20V 150M - GEN	28452-771P
TR20	TR PSI BC450 100V 200M	28438-259F
TR21	TR NSI BC449 100V 250M	28457-821N
TR22	TR NSI BC449 100V 250M	28457-821N
TR24	TR NSI TIP112 100V 5M DAR	28457-822L
TR31	TR NJF 2N4857 40V 40R - 20MA	28459-051X

Circuit Ref	Description	Part Number
Board AB1	- D to A converter	(Contd.)
TR32	TR NJF 2N4857 40V 40R - 20MA	28459-051X
X1	S/C ACC PAD TO18,ETC TO 0.1"GRD	28488-115L
X2	S/C ACC SKT DIL16 LOW PROFILE	28488-041E
X7	S/C ACC WASHER 6BA/M3 INSUL	28488-127P
X8	S/C ACC BUSH M3 INSUL	28488-134R
X9	CORE BEAD 5X.7X10LG 3S2	23635-811Z
X10	S/C ACC H/SINK TO220 17K/W	28488-465W
X15	S/C ACC WASHER 6BA/M3 INSUL	28488-127P
X16	S/C ACC BUSH M3 INSUL	28488-134R
X17	S/C ACC PAD TO5 TO DIL8	28488-102R

Circuit Ref	Description	Part Number
Board AB2	- Interpolation oscillator	
25.	When ordering, prefix circuit reference with AB2	
	Complete unit	44828-463T
C1	CAP MICA 15P 350V 1PF	26272-020F
C2	CAP CER 18P 500V 5% N750 DIS	26343-060Y
C3	CAP CER 18P 500V 5% N750 DIS	26343-060Y
C4	CAP CER 4N7 63V 10% PLATE	26383-591B
C5	CAP CER 1N0 500V 20% DISC	26383-242P
C6	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C7	CAP CER 10N 25V 20% DISC	26383-006C
C8	CAP CER 10N 25V 20% DISC	26383-006C
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP CER 10N 25V 20% DISC	26383-006C
C13	CAP CER 10N 25V 20% DISC	26383-006C
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 10N 25V 20% DISC	26383-006C
C16	CAP CER 39P 63V 5% PLATE	26343-472N
C19	CAP CER 4N7 63V 10% PLATE	26383-591B
C20	CAP CER 47N 25V 20% DISC	26383-017U
C21	CAP CER 4N7 63V 10% PLATE	26383-591B
C22	CAP CER 4N7 63V 10% PLATE	26383-591B
C29	CAP CER 4N7 63V 10% PLATE	26383-591B
C30	CAP CER 4N7 63V 10% PLATE	26383-591B
C31	CAP CER 47N 25V 20% DISC	26383-017U
C32	CAP CER 4N7 63V 10% PLATE	26383-591B
C33	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C34	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C35	CAP CER 100P 63V 2% PLATE	26343-477V
C36	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C37	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
D1	DI V/CAP BB809 3V 29PF	28381-132G
D2	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI V/CAP BB809 3V 29PF	28381-132G
D4	DI V/CAP BB809 3V 29PF	28381-132G
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA VREG UA723C PROG DIL14	28461-706F

Circuit Ref	Description	Part Number
Board AB2	- Interpolation oscillator	(Contd.)
L1	IND CHOKE 1000UH 10% LAQ	23642-567C
L3	IND CHOKE 4.7UH 10% LAQ	23642-553J
L4	IND CHOKE 4.7UH 10% LAQ	23642-553J
L5	CHOKE ASSY	44190-034C
L6	CHOKE ASSY	44190-034C
MP1	S/C ACC SKT DIL14 LOW PROFILE	28488-040H
MP3	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
R1	RES MF 300K 1/4W 2% 100PPM	24773-332T
R2	RES MF 300K 1/4W 2% 100PPM	24773-332T
R3	RES MF 9K1 1/4W 2% 100PPM	24773-296X
R4	RES MF 27K 1/4W 2% 100PPM	24773-307K
R5	RES MF 56K 1/4W 2% 100PPM	24773-315U
R6	RES MF 160K 1/4W 2% 100PPM	24773-326S
R7	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R8	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R9	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R10	RES MF 9K9 1/4W 0.1% 15PPM	24723-393L
R11	RES MF 900R0 1/4W 0.1% 15PPM	24723-392N
R12	RES MF 200R 1/4W .1% 25PPM	24723-396G
R13	RES CC 2K4 1/8W 5%	24331-968Z
R14	RES CC 2K4 1/8W 5%	24331-968Z
R15	RES CC 56R 1/8W 5%	24331-944N
R16	RES CC 160R 1/8W 5%	24331-991T
R17	RES CC 820R 1/8W 5%	24331-993X
R18	RES CC 390R 1/8W 5%	24331-963C
R19	RES MF 200R 1/4W 2% 100PPM	24773-256S
R20	RES CC 36R 1/8W 5%	24331-936Z
R21	RES CC 100R 1/8W 5%	24331-997B
R22	RES MF 47R 1/4W 2% 100PPM	24773-241A
R23	RES CC 270R 1/8W 5%	24331-992P
R24	RES CC 100R 1/8W 5%	24331-997B
R25	RES MF 10R 1/4W 2% 100PPM	24773-225W
R32	RES MF 47R 1/4W 2% 100PPM	24773-241A
R33	RES CC 270R 1/8W 5%	24331-992P
R34	RES CC 100R 1/8W 5%	24331-997B
R35	RES MF 10R 1/4W 2% 100PPM	24773-225W
R40	RES CC 8K2 1/8W 5%	24331-952V

Circuit Ref	Description	Part Number
Board AB2	- Interpolation oscillator	(Contd.)
R41	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R42	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R43	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R44	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R45	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R46	RES MF 2R2 1/4W 2% 100PPM	24773-209E
TR1	TR NJF J310 25V - 24MA	28459-028E
TR2	TR NJF 2N4857 40V 40R 20MA	28459-051X
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NSI BFY90 15V 1G - AMP	28452-157R
TR7	TR PSI BC308B 20V 130M - GEN	28433-455R
T1	OSC TRANS ASSY	43590-120W
T2	MATCHING TRANS ASSY	43590-127R
T3	SPLITTER TRANS ASSY	43590-123P
T4	BUFFER O/P TRANS ASSY	43590-122T
T5	BUFFER O/P TRANS ASSY	43590-122T

Circuit Ref	Description	Part Number
Board AB3	- Master VCO	
26.	When ordering, prefix circuit reference with AB3	
	Complete unit	44828-464P
C1	CAP MICA 33P 350V 1PF	26272-391L
C2	CAP PS 15P 63V 1PF RAD	26538-506K
C3	CAP PS 15P 63V 1PF RAD	26538-506K
C4	CAP CER 4N7 63V 10% PLATE	26383-591B
C5	CAP PS 150P 63V 2% RAD	26538-571R
C7	CAP CER 10N 25V 20% DISC	26383-006C
C8	CAP CER 330P 63V 2% PLATE	26343-483D
C9	CAP CER 22N 18V 20% DISC	26383-007R
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP CER 10N 25V 20% DISC	26383-006C
C13	CAP CER 10N 25V 20% DISC	26383-006C
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 10N 25V 20% DISC	26383-006C
C16	CAP CER 39P 63V 5% PLATE	26343-472N
C19	CAP CER 4N7 63V 10% PLATE	26383-591B
C20	CAP CER 47N 25V 20% DISC	26383-017U
C21	CAP CER 4N7 63V 10% PLATE	26383-591B
C22	CAP CER 4N7 63V 10% PLATE	26383-591B
C29	CAP CER 4N7 63V 10% PLATE	26383-591B
C30	CAP CER 47N 25V 20% DISC	26383-017U
C31	CAP CER 4N7 63V 10% PLATE	26383-591B
C32	CAP CER 4N7 63V 10% PLATE	26383-591B
C33	CAP CER 4N7 63V 10% PLATE	26383-591B
C34	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C35	CAP CER 4N7 63V 10% PLATE	26383-591B
C36	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C37	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C38	CAP CER 100P 63V 2% PLATE	26343-477V
C39	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C40	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C41	CAP CER 22N 18V 20% DISC	26383-007R
C42	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C43	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C47	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
D1	DI V/CAP BB809 3V 29PF	28381-132G
D2	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI V/CAP BB809 3V 29PF	28381-132G

Circuit Ref	Description	Part Number
Board AB3	- Master VCO	(Contd.)
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI ZEN BZX79C20 20V 5%	28372-785K
IC1	ICA VREG UA723C PROG DIL14	28461-706F
IC2	ICA AMP TL072CP DUAL FET I/P	28461-348Z
L1	OSC COIL ASSY	44290-870V
L4	IND CHOKE 4.7UH 10% LAQ	23642-553J
L5	IND CHOKE 4.7UH 10% LAQ	23642-553J
L6	CHOKE ASSY	44190-034C
L7	CHOKE ASSY	44190-034C
L8	IND CHOKE 4.7UH 10% LAQ	23642-553J
MP1	S/C ACC SKT DIL14 LOW PROFILE	28488-040H
MP3	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
R1	RES MF 300K 1/4W 2% 100PPM	24773-332T
R2	RES MF 300K 1/4W 2% 100PPM	24773-332T
R3	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R5	RES MF 240R 1/4W 2% 100PPM	24773-258D
R6	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R12	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R13	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R14	RES MF 56R 1/4W 2% 100PPM	24773-243H
R15	RES MF 160R 1/4W 2% 100PPM	24773-254G
R16	RES MF 820R 1/4W 2% 100PPM	24773-271B
R17	RES CC 390R 1/8W 5%	24331-963C
R18	RES CC 200R 1/8W 5%	24331-999A
R19	RES MF 36R 1/4W 2% 100PPM	24773-238A
R20	RES CC 100R 1/8W 5%	24331-997B
R21	RES MF 47R 1/4W 2% 100PPM	24773-241A
R22	RES CC 270R 1/8W 5%	24331-992P
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 10R 1/4W 2% 100PPM	24773-225W

Circuit Ref	Description	Part Number
Board AB3	- Master VCO	(Contd.)
R31	RES MF 47R 1/4W 2% 100PPM	24773-241A
R32	RES CC 270R 1/8W 5%	24331-992P
R33	RES MF 100R 1/4W 2% 100PPM	24773-249J
R34	RES CC 10R 1/8W 5%	24331-974U
R35	RES MF 43R 1/4W 2% 100PPM	24773-240K
R36	RES MF 82R 1/4W 2% 100PPM	24773-247N
R37	RES MF 100R 1/4W 2% 100PPM	24773-249J
R40	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R41	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R42	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R43	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R44	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R45	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R46	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R47	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R50	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R52	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R53	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R54	RES MF 390R 1/4W 2% 100PPM	24773-263P
R56	RES MF 390R 1/4W 2% 100PPM	24773-263P
R57	RES MF 24K 1/4W 2% 100PPM	24773-306B
R58	RES MF 200R 1/4W 2% 100PPM	24773-256S
R60	RES MF 10K 1/4W 2% 100PPM	24773-297M
R61	RES CC 100R 1/8W 5%	24331-997B
TR1	TR NJF J310 25V - 24MA	28459-028E
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NSI BFY90 15V 1G - AMP	28452-157R
TR7	TR PSI BC308B 20V 130M - GEN	28433-455R
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR9	TR NJF 2N4857 40V 40R 20MA	28459-051X
T1	MATCHING TRANS ASSY	43590-127R
T2	SPLITTER TRANS ASSY	43590-123P
T3	BUFFER O/P TRANS ASSY	43590-122T
T4	BUFFER O/P TRANS ASSY	43590-122T
T5	O/P BALUN	43590-147V

Circuit Ref	Description		Part Number
Board AB4	- Sampling gate		
27.	When ordering, prefix circuit reference with AB4		
	Complete unit		44828-465X
C1	CAP CER 4N7 63V 10% PLATE		26383-591B
C2	CAP CER 4N7 63V 10% PLATE		26383-591B
C3	CAP TANT 2U2 35V 20% BEAD		26486-214V
C4	CAP CER 4N7 63V 10% PLATE		26383-591B
C5	CAP CER 4N7 63V 10% PLATE		26383-591B
C6	CAP CER 4N7 63V 10% PLATE		26383-591B
C7	CAP CER 4N7 63V 10% PLATE		26383-591B
C8	CAP CER 27P 63V 5% PLATE		26343-470U
C9	CAP CER 6P8 63V .5PF PLATE		26343-463A
C10	CAP CER 68P 63V 2% PLATE		26343-475F
C11	CAP CER 4N7 63V 10% PLATE		26383-591B
C12	CAP CER 4N7 63V 10% PLATE		26383-591B
C13	CAP TANT 2U2 35V 20% BEAD		26486-214V
C14	CAP CER 4N7 63V 10% PLATE		26383-591B
C15	CAP CER 4N7 63V 10% PLATE		26383-591B
C16	CAP CER 220P 63V 2% PLATE		26343-481S
C17	CAP CER 6P8 63V .5PF PLATE		26343-463A
C18	CAP PETP 220N 63V 10% RAD		26582-406T
C19	CAP CER 4N7 63V 10% PLATE		26383-591B
C20	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C23	CAP ELEC 470U 6V 20%+ PCB		26421-126S
C24	CAP ELEC 1000U 10V 20%+ AX		26415-824S
C25	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
D1	DI H/CARR BAT29 5V	!	28349-014L
D2	DI H/CARR BAT29 5V	!	28349-014L
D3	DI H/CARR BAT29 5V	!	28349-014L
D4	DI H/CARR BAT29 5V	!	28349-014L
D5	DI ZEN BZX79C5V6 5.6V 5%		28371-417X
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
D8	DI H/CARR BAT29 5V	!	28349-014L
D9	DI H/CARR BAT29 5V	!	28349-014L
D10	DI H/CARR BAT29 5V	!	28349-014L
D11	DI H/CARR BAT29 5V	!	28349-014L
D12	DI ZEN BZX79C5V6 5.6V 5%		28371-417X

Circuit Ref	Description	Part Number
Board AB4	- Sampling gate	(Contd.)
D13	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA AMP TL071CP FET I/P DIL8	28461-347A
IC2	ICA AMP TL071CP FET I/P DIL8	28461-347A
IC3	ICA AMP UA741CN GP DIL8	28461-304T
IC4	ICD CTR 10138 4BIT DEC	28464-019X
IC5	ICD CTR 10138 4BIT DEC	28464-019X
IC6	ICD CTR 10138 4BIT DEC	28464-019X
L1	IND CHOKE 4.7UH 10% LAQ	23642-553J
L2	IND CHOKE 1.0UH 10% LAQ	23642-549L
MP1	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
MP4	S/C ACC PAD CBE TO TO5	28488-108E
R1	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R2	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R3	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R4	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R5	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R6	RES MF 200R 1/4W 2% 100PPM	24773-256S
R7	RES MF 200R 1/4W 2% 100PPM	24773-256S
R8	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R9	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R10	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R11	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R12	RES MF 10K 1/4W 2% 100PPM	24773-297M
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 200R 1/4W 2% 100PPM	24773-256S
R15	RES MF 200R 1/4W 2% 100PPM	24773-256S
R16	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R17	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R18	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R19	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R20	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R21	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R22	RES MF 680R 1/4W 2% 100PPM	24773-269K
R23	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R24	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R25	RES MF 360R 1/4W 2% 100PPM	24773-262T
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Board AB4	- Sampling gate	(Contd.)
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R28	RES MF 100K 1/4W 2% 100PPM	24773-321L
R29	RES MF 20K 1/4W 2% 100PPM	24773-304C
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R33	RES MF 390R 1/4W 2% 100PPM	24773-263P
R34	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R35	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R36	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R37	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R38	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R39	RES MF 20R 1/4W 2% 100PPM	24773-232X
R40	RES MF 10R 1/4W 2% 100PPM	24773-225W
R41	RES MF 100R 1/4W 2% 100PPM	24773-249J
R42	RES MF 10R 1/4W 2% 100PPM	24773-225W
R43	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R44	RES MF 20R 1/4W 2% 100PPM	24773-232X
R45	RES MF 200R 1/4W 2% 100PPM	24773-256S
R46	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R47	RES MF 62R 1/4W 2% 100PPM	24773-244E
R48	RES MF 820R 1/4W 2% 100PPM	24773-271B
R49	RES MF 330R 1/4W 2% 100PPM	24773-261D
TR1	TR PSI MPSL08 12V 700M - SW	28431-767E
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR3	TR NSI BC208B 20V 150M - GEN	28452-781A
TR4	TR PSI BC308B 20V 130M - GEN	28433-455R
TR5	TR NSI 2N2369 15V 500M - SW	28452-197H
TR6	TR PSI MPSL08 12V 700M - SW	28431-767E
TR7	TR NSI BC208B 20V 150M - GEN	28452-781A
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR9	TR NSI BFY90 15V 1G - AMP	28452-157R
T1	BALUN ASSY	43590-125M
T2	UNBAL ASSY	43590-124X
T3	BALUN ASSY	43590-125M
T4	UNBAL ASSY	43590-124X
T5	UNBAL ASSY	43590-124X

Circuit Ref	Description	Part Number
Board AB5	- Slave VCO	
28.	When ordering, prefix circuit reference with AB5	
	Complete unit	44828-466M
C1	CAP MICA 33P 350V 1PF	26272-391L
C2	CAP PS 33P 63V 1PF RAD	26538-530D
C3	CAP PS 33P 63V 1PF RAD	26538-530D
C4	CAP CER 4N7 63V 10% PLATE	26383-591B
C5	CAP PS 100P 63V 2% RAD	26538-557S
C6	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C7	CAP CER 10N 25V 20% DISC	26383-006C
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP CER 10N 25V 20% DISC	26383-006C
C13	CAP CER 10N 25V 20% DISC	26383-006C
C14	CAP CER 10N 25V 20% DISC	26383-006C
C15	CAP CER 10N 25V 20% DISC	26383-006C
C16	CAP CER 39P 63V 5% PLATE	26343-472N
C19	CAP CER 4N7 63V 10% PLATE	26383-591B
C20	CAP CER 47N 25V 20% DISC	26383-017U
C21	CAP CER 4N7 63V 10% PLATE	26383-591B
C22	CAP CER 4N7 63V 10% PLATE	26383-591B
C29	CAP CER 4N7 63V 10% PLATE	26383-591B
C30	CAP CER 47N 25V 20% DISC	26383-017U
C31	CAP CER 4N7 63V 10% PLATE	26383-591B
C32	CAP CER 4N7 63V 10% PLATE	26383-591B
C33	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C34	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C35	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C36	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C37	CAP CER 33P 63V 5% PLATE	26343-471Y
C38	CAP CER 22N 18V 20% DISC	26383-007R
C39	CAP CER 22N 18V 20% DISC	26383-007R
D1	DI V/CAP BB809 3V 29PF	28381-132G
D2	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA AMP NE5534AN H-PRF DIL8	28461-358J
L1	OSC COIL ASSY	44290-870V
L3	IND CHOKE 4.7UH 10% LAQ	23642-553J
L4	IND CHOKE 4.7UH 10% LAQ	23642-553J

Circuit Ref	Description	Part Number
Board AB5	- Slave VCO	(Contd.)
L5	CHOKE ASSY	44190-034C
L6	CHOKE ASSY	44190-034C
MP2	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
R1	RES MF 300K 1/4W 2% 100PPM	24773-332T
R2	RES MF 300K 1/4W 2% 100PPM	24773-332T
R3	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R4	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R5	RES MF 470R 1/4W 2% 100PPM	24773-265M
R6	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R12	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R13	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R14	RES MF 56R 1/4W 2% 100PPM	24773-243H
R15	RES MF 160R 1/4W 2% 100PPM	24773-254G
R16	RES MF 820R 1/4W 2% 100PPM	24773-271B
R17	RES MF 390R 1/4W 2% 100PPM	24773-263P
R18	RES MF 200R 1/4W 2% 100PPM	24773-256S
R19	RES MF 36R 1/4W 2% 100PPM	24773-238A
R20	RES CC 100R 1/8W 5%	24331-997B
R21	RES MF 47R 1/4W 2% 100PPM	24773-241A
R22	RES CC 270R 1/8W 5%	24331-992P
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 10R 1/4W 2% 100PPM	24773-225W
R31	RES MF 47R 1/4W 2% 100PPM	24773-241A
R32	RES CC 270R 1/8W 5%	24331-992P
R33	RES MF 100R 1/4W 2% 100PPM	24773-249J
R34	RES MF 10R 1/4W 2% 100PPM	24773-225W
R45	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R46	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R47	RES MF 2R2 1/4W 2% 100PPM	24773-209E
R51	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R52	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R53	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R54	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R55	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R57	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Board AB5	- Slave VCO	(Contd.)
TR1	TR NJF J310 25V - 24MA	28459-028E
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NSI BFY90 15V 1G - AMP	28452-157R
T1	MATCHING TRANS ASSY	43590-127R
T2	SPLITTER TRANS ASSY	43590-123P
T3	BUFFER O/P TRANS ASSY	43590-122T
T4	BUFFER O/P TRANS ASSY	43590-122T

Circuit Ref	Description		Part Number
Board AB6	- Phase detector		
29.	When ordering, prefix circuit reference with AB6		
	Complete unit		44828-467C
C1	CAP CER 22N 18V 20% DISC		26383-007R
C2	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C5	CAP CER 47N 25V 20% DISC		26383-017U
C6	CAP CER 220P 63V 2% PLATE		26343-481S
C9	CAP PETP 100N 100V 10% RAD		26582-211B
C10	CAP CER 100P 63V 2% PLATE		26343-477V
C11	CAP PETP 100N 100V 10% RAD		26582-211B
C12	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C13	CAP CER 10N 25V 20% DISC		26383-006C
C14	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C20	CAP CER 4N7 63V 2% PLATE		26343-591B
C21	CAP ELEC 2U2 50V 20% L/LEAK		26421-009E
D1	LAMP LED TIL209 3V RED		28624-110P
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICD CTR 74LS93 4BIT BIN 2,8,16		28464-117W
IC2	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC3	ICD FF D 74HCT74 +EDG TR	!	28462-630W
IC4	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC5	ICA AMP TL074CN QUAD FET I/P		28461-349H
L1	INDUCTOR CHOKE 40UH		44190-036B
MP2	S/C ACC PAD TO18,ETC TO .1"GRD		28488-115L
MP3	S/C ACC SKT DIL16 LOW PROFILE		28488-041E
R1	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R2	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R3	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R4	RES MF 330R 1/4W 2% 100PPM		24773-261D
R5	RES MF 510R 1/4W 2% 100PPM		24773-266C
R6	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R7	RES MF 15R 1/4W 2% 100PPM		24773-229X
R8	RES MF 3KO 1/4W 2% 100PPM		24773-284J

Circuit Ref	Description	Part Number
Board AB6	- Phase detector (Contd.)	
R9	RES MF 910R 1/4W 2% 100PPM	24773-272K
R10	RES MF 510R 1/4W 2% 100PPM	24773-266C
R11	RES MF 33R 1/4W 2% 100PPM	24773-237K
R12	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R13	RES MF 10K 1/4W 2% 100PPM	24773-297M
R14	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R15	RES MF 150K 1/4W 2% 100PPM	24773-325V
R16	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R17	RES MF 820K 1/4W 2% 100PPM	24773-344Z
R18	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R19	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R20	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R21	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R24	RES MF 100K 1/4W 2% 100PPM	24773-321L
R25	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R26	RES MF 100K 1/4W 2% 100PPM	24773-321L
R27	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R28	RES MF 30K 1/4W 2% 100PPM	24773-308A
R29	RES MF 15K 1/4W 2% 100PPM	24773-301P
R30	RES MF 100K 1/4W 2% 100PPM	24773-321L
R31	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R32	RES MF 10R 1/4W 2% 100PPM	24773-225W
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NSI BC209C 20V 150M - GEN	28452-771P
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
TR4	TR NJF 2N4857 40V 40R 20MA	28459-051X
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR NJF 2N4857 40V 40R 20MA	28459-051X
T1	BALUN TRANS ASSY	43590-129K
T2	BALUN TRANS ASSY	43590-129K
X1	MOD RF SBL-1 DOUBLE BAL MIXER	28531-002A

Circuit Ref	Description	Part Number
Board AB7	- Oscillator select	
30.	When ordering, prefix circuit reference with AB7	
	Complete unit	44828-468R
C1	CAP CER 4N7 63V 10% PLATE	26383-591B
C2	CAP CER 4N7 63V 10% PLATE	26383-591B
C3	CAP CER 10N 25V 20% DISC	26383-006C
C4	CAP CER 4N7 63V 10% PLATE	26383-591B
C5	CAP CER 4N7 63V 10% PLATE	26383-591B
C6	CAP CER 10N 25V 20% DISC	26383-006C
C7	CAP CER 4N7 63V 10% PLATE	26383-591B
C8	CAP CER 4N7 63V 10% PLATE	26383-591B
C9	CAP CER 10N 25V 20% DISC	26383-006C
C10	CAP CER 100N 30V 20% DISC	26383-031S
C11	CAP CER 100N 30V 20% DISC	26383-031S
C12	CAP CER 100N 30V 20% DISC	26383-031S
C13	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
IC1	ICD OR 74LS32 QUAD 2INP	28466-108U
IC2	ICD NAND 74S10 TRIP 3INP	28466-338B
MP2	S/C ACC PAD CBE TO TO5	28488-108E
MP3	S/C ACC PAD TO18	28488-115L
R1	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R2	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R3	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R4	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R5	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R6	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R7	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R8	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R9	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R10	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R11	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R12	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R13	RES MF 15K 1/4W 2% 100PPM	24773-301P
R14	RES MF 15K 1/4W 2% 100PPM	24773-301P
R15	RES MF 15K 1/4W 2% 100PPM	24773-301P
TR1	TR PSI MPSL08 12V 700M - SW	28431-767E
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR3	TR PSI MPSL08 12V 700M - SW	28431-767E
TR4	TR NSI 2N2369 15V 500M - SW	28452-197H
TR5	TR PSI MPSL08 12V 700M - SW	28431-767E
TR6	TR NSI 2N2369 15V 500M - SW	28452-197H

Circuit Ref	Description		Part Number
Board AB8	- Attenuator control		
31.	When ordering, prefix circuit reference with AB8		
	Complete unit		44828-469B
C1	CAP ELEC 3U3 50V 20% SUBMIN		26421-109Z
C2	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C3	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C4	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C5	CAP CER 4N7 63V 10% PLATE		26383-591B
C6	CAP CER 4N7 63V 10% PLATE		26383-591B
C7	CAP CER 22N 18V 20% DISC		26383-007R
C8	CAP ELEC 3U3 50V 20% SUBMIN		26421-109Z
D1	DI H/CARR HP5082-2826	!	28349-011U
D2	DI H/CARR HP5082-2826	!	28349-011U
D3	DI RECT 1N4004 400V		28357-028K
D4	DI SIL 1N4148 75V JUNC		28336-676J
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI H/CARR BAT29 5V	!	28349-014L
D8	DI H/CARR BAT29 5V	!	28349-014L
D9	DI H/CARR BAT29 5V	!	28349-014L
D10	DI H/CARR BAT29 5V	!	28349-014L
IC1	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC2	ICA COMP LM311N DIL8		28461-695U
IC3	ICA COMP LM311N DIL8		28461-695U
IC4	ICD NAND 74LS132 QUAD 2INP SCH		28469-205N
IC5	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC6	ICA COMP LM339N QUAD		28461-693H
IC7	ICA COMP LM339N QUAD		28461-693H
IC8	ICD MONO 74LS123 DUAL RETR		28468-309B
R1	RES MF 10K 1/4W 2% 100PPM		24773-297M
R2	RES MF 10K 1/4W 2% 100PPM		24773-297M
R3	RES MF 953K 1/4W .5% 50PPM		24753-335P
R4	RES MF 470K 1/4W 2% 100PPM		24773-337R
R5	RES MF 1M0 1/4W .5% 50PPM		24753-337M
R6	RES MF 3K0 1/4W 0.5% 50PPM		24753-475C

Circuit Ref	Description	Part Number
Board AB8	- Attenuator control	(Contd.)
R7	RES MF 120K 1/4W .5% 50PPM	24753-338C
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 10K 1/4W 2% 100PPM	24773-297M
R10	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R11	RES MF 3K16 1/4W 0.5% 50PPM	24753-476R
R12	RES MF 100K 1/4W .5% 50PPM	24753-340M
R13	RES MF 3K0 1/4W 0.5% 50PPM	24753-475C
R14	RES MF 100K 1/4W .5% 50PPM	24753-340M
R15	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R16	RES MF 10K 1/4W 2% 100PPM	24773-297M
R17	RES MF 47K 1/4W 2% 100PPM	24773-313H
R18	RES MF 27K 1/4W 2% 100PPM	24773-307K
R19	RES MF 12K 1/4W 2% 100PPM	24773-299R
R20	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R21	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R22	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R23	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R24	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R25	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R26	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R28	RES MF 10K 1/4W 2% 100PPM	24773-297M
R29	RES MF 120R 1/4W 2% 100PPM	24773-251L
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MF 47K 1/4W 2% 100PPM	24773-313H
R32	RES MF 10K 1/4W 2% 100PPM	24773-297M
R33	RES MF 100K 1/4W 2% 100PPM	24773-321L
TR1	TR NSI 2N2219A 40V 300M - GEN	28454-804V
TR2	TR PSI BC212B 50V 200M - GEN	28435-428K
TR3	TR PSI BC212B 50V 200M - GEN	28435-428K
TR4	TR PSI BC212B 50V 200M - GEN	28435-428K
TR5	TR PSI BC212B 50V 200M - GEN	28435-428K
TR6	TR PSI BC212B 50V 200M - GEN	28435-428K
TR7	TR PSI BC212B 50V 200M - GEN	28435-428K

Circuit Ref	Description	Part Number
Unit AC0/AD0	- IF box assembly (AC/AD)	
32.	When ordering, prefix circuit reference with AC0/AD0	
	Complete unit	44990-451F
C2	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C3	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C4	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C11	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C12	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C13	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C36	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C37	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C38	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C39	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C40	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C41	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C42	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C43	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K

Circuit Ref	Description	Part Number
Unit AC0/AD0	- IF box assembly (AC/AD)	(Contd.)
C45	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C48	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C49	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C50	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C53	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C57	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C58	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C59	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C60	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C61	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C62	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C63	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C64	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C65	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C66	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C67	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C68	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C69	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C70	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C71	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C72	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C73	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C74	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C75	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C76	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C80	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C81	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C82	CAP ELEC 220U 16V 20%+ PCB	26421-124G
L1	IND CHOKE 470UH 10% SCREENED	23642-333B
L2	IND CHOKE 470UH 10% SCREENED	23642-333B
L3	IND CHOKE 470UH 10% SCREENED	23642-333B
L4	IND CHOKE 470UH 10% SCREENED	23642-333B
L5	INDUCTOR 1MH PWR	44190-042Z
L6	INDUCTOR CHOKE GEN	44190-036B
L7	IND CHOKE 470UH 10% SCREENED	23642-333B
L8	INDUCTOR	34900-918Y
L9	IND CHOKE 680UH 10% LAQ	23642-566M
L10	IND CHOKE 680UH 10% LAQ	23642-566M

Circuit Ref	Description	Part Number
Unit AC0/AD0	- IF box assembly (AC/AD)	(Contd.)
L11	IND CHOKE 470UH 10% SCREENED	23642-333B
L12	IND CHOKE 470UH 10% SCREENED	23642-333B
L13	IND CHOKE 680UH 10% LAQ	23642-566M
L14	IND CHOKE 470UH 10% SCREENED	23642-333B
L15	INDUCTOR 1MH PWR	44190-042Z
L16	IND CHOKE 470UH 10% SCREENED	23642-333B
L17	IND CHOKE 680UH 10% LAQ	23642-566M
L20	IND CHOKE GEN 470UH	44190-333B
PLZ	CON RF SMB MALE 50 BKHD ELB	23444-351P
R2	RES MF 100K 1/4W 2% 100PPM	24773-321L
R3	RES MF 100K 1/4W 2% 100PPM	24773-321L
R4	RES MF 100K 1/4W 2% 100PPM	24773-321L
R5	RES MF 510R 1/4W 2% 100PPM	24773-266C
R6	RES MF 100K 1/4W 2% 100PPM	24773-321L
R7	RES MF 100K 1/4W 2% 100PPM	24773-321L
R8	RES MF 100K 1/4W 2% 100PPM	24773-321L
R9	RES MF 100K 1/4W 2% 100PPM	24773-321L
R10	RES MF 100K 1/4W 2% 100PPM	24773-321L
R11	RES MF 100K 1/4W 2% 100PPM	24773-321L
R12	RES MF 510R 1/4W 2% 100PPM	24773-266C
R13	RES MF 510R 1/4W 2% 100PPM	24773-266C
R14	RES MF 510R 1/4W 2% 100PPM	24773-266C
R15	RES MF 100K 1/4W 2% 100PPM	24773-321L
R16	RES MF 100K 1/4W 2% 100PPM	24773-321L
R17	RES MF 100K 1/4W 2% 100PPM	24773-321L
	CABLE ASSY AC3-47.4MHZ O/P	43130-248K
	CABLE ASSY 16-WAY RIBBON	43129-952N
	CABLE ASSY 10-WAY RIBBON	43129-953L
	CABLE ASSY 16-WAY RIBBON	43129-954J
	CABLE ASSY MIN COAX	43129-972R
	CABLE ASSY MIN COAX	43129-975A

Circuit Ref	Description	Part Number
Board AC1	- 50 MHz crystal oscillator	
33.	When ordering, prefix circuit reference with AC1	
	Complete unit	44828-472B
C1	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C2	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C10	CAP CER 22N 18V 20% DISC	26383-007R
C11	CAP CER 1N0 63V 10% PLATE	26383-585M
C12	CAP CER 100P 63V 2% PLATE	26343-477V
C13	CAP CER 4N7 63V 10% PLATE	26383-591B
C14	CAP CER 4N7 63V 10% PLATE	26383-591B
C15	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C16	CAP CER 4N7 63V 10% PLATE	26383-591B
C17	CAP CER 4N7 63V 10% PLATE	26383-591B
C18	CAP CER 4N7 63V 10% PLATE	26383-591B
C20	CAP CER 22N 18V 20% DISC	26383-007R
C21	CAP CER 4N7 63V 10% PLATE	26383-591B
C22	CAP CER 4N7 63V 10% PLATE	26383-591B
C23	CAP CER 4N7 63V 10% PLATE	26383-591B
C25	CAP CER 4N7 63V 10% PLATE	26383-591B
C26	CAP CER 4N7 63V 10% PLATE	26383-591B
C30	CAP CER 4N7 63V 10% PLATE	26383-591B
C31	CAP CER 4N7 63V 10% PLATE	26383-591B
C32	CAP CER 4N7 63V 10% PLATE	26383-591B
C33	CAP CER 4N7 63V 10% PLATE	26383-591B
C34	CAP CER 22N 18V 20% DISC	26383-007R
C35	CAP CER 4N7 63V 10% PLATE	26383-591B
D1	DI V/CAP BB405B 3V 11.5PF	28381-101V
D2	DI V/CAP BB405B 3V 11.5PF	28381-101V
D3	DI V/CAP BB405B 3V 11.5PF	28381-101V
D4	DI V/CAP BB405B 3V 11.5PF	28381-101V
D5	DI RECT 1N4004 400V	28357-028K
IC1	ICA VREG+ LM317T PROG 1A5	28461-726A
L2	INDUCTOR (AC1)	44290-873D
L3	INDUCTOR (AC1)	44290-872W
R2	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R3	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R4	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R5	RES MF 300R 1/4W 2% 100PPM	24773-260W
R6	RES MF 1K0 1/4W 2% 100PPM	24773-273A

Circuit Ref	Description	Part Number
Board AC1	- 50 MHz crystal oscillator (Contd.)	
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 20K 1/4W 2% 100PPM	24773-304C
R9	RES MF 100R 1/4W 2% 100PPM	24773-249J
R10	RES MF 10K 1/4W 2% 100PPM	24773-297M
R11	RES MF 10K 1/4W 2% 100PPM	24773-297M
R12	RES MF 150R 1/4W 2% 100PPM	24773-253F
R13	RES MF 390R 1/4W 2% 100PPM	24773-263P
R14	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R15	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R16	RES MF 820R 1/4W 2% 100PPM	24773-271B
R17	RES MF 47R 1/4W 2% 100PPM	24773-241A
R20	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R21	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R22	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R23	RES MF 200R 1/4W 2% 100PPM	24773-256S
R24	RES MF 200R 1/4W 2% 100PPM	24773-256S
R25	RES MF 750R 1/4W 2% 100PPM	24773-270R
R26	RES MF 47R 1/4W 2% 100PPM	24773-241A
R27	RES MF 680R 1/4W 2% 100PPM	24773-269K
R28	RES MF 56R 1/4W 2% 100PPM	24773-243H
R32	RES MF 47R 1/4W 2% 100PPM	24773-241A
R33	RES MF 470R 1/4W 2% 100PPM	24773-265M
R34	RES MF 56R 1/4W 2% 100PPM	24773-243H
R35	RES MF 470R 1/4W 2% 100PPM	24773-265M
R36	RES MF 47R 1/4W 2% 100PPM	24773-241A
R37	RES MF 47R 1/4W 2% 100PPM	24773-241A
R38	RES MF 56R 1/4W 2% 100PPM	24773-243H
R40	RES MO 270R 1/2W 2% 250PPM	24573-059Y
R41	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R42	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R43	RES MF 24R 1/4W 2% 100PPM	24773-234C
R44	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R45	RES MF 330R 1/4W 2% 100PPM	24773-261D
R46	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R51	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R52	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R53	RES MF 24R 1/4W 2% 100PPM	24773-234C
R54	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R55	RES MF 820R 1/4W 2% 100PPM	24773-271B
R56	RES MF 330R 1/4W 2% 100PPM	24773-261D
R57	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R58	RES MF 220R 1/4W 2% 100PPM	24773-257W
R59	RES MF 1K8 1/4W 2% 100PPM	24773-279N

Circuit Ref	Description	Part Number
Board AC1	- 50 MHz crystal oscillator	(Contd.)
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NSI BFY90 15V 1G - AMP	28452-157R
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR7	TR NSI BFY90 15V 1G - AMP	28452-157R
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR9	TR NSI BFY90 15V 1G - AMP	28452-157R
TR10	TR PSI 2N4959 30V 1G - LN AMP	28433-836K
TR11	TR PSI 2N4959 30V 1G - LN AMP	28433-836K
TR12	TR PSI MPS6534 40V 260M - AMP	28434-827E
X10	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
X11	S/C ACC BUSH 6BA/M3 INSUL	28488-126T
X12	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
XL1	XTAL 50.0015M S-	28312-086J

Circuit Ref	Description	Part Number
Board AC2	- 47.4 MHz i.f. amplifier	
34.	When ordering, prefix circuit reference with AC2	
	Complete unit	44828-473K
C1	CAP CER 100N 30V 20% DISC	26383-031S
C2	CAP CER 10P 63V 0P5 PLATE	26343-465H
C3	CAP CER 10P 63V 0P5 PLATE	26343-465H
C4	CAP VAR PLAS 10P 2P TRIM	26876-001F
C5	CAP CER 15P 63V 2% PLATE N470	26343-455M
C8	CAP CER 100P 63V 2% PLATE	26343-477V
C9	CAP VAR PLAS 10P 2P TRIM	26876-001F
C10	CAP CER 8P2 63V 0P5 PLATE	26343-464Z
C11	CAP VAR PLAS 10P 2P TRIM	26876-001F
C12	CAP CER 8P2 63V 0P5 PLATE	26343-464Z
C13	CAP VAR PLAS 10P 2P TRIM	26876-001F
C14	CAP CER 8P2 63V 0P5 PLATE	26343-464Z
C15	CAP VAR PLAS 10P 2P TRIM	26876-001F
C16	CAP CER 10P 63V 0P5 PLATE	26343-465H
C17	CAP CER 100P 63V 2% PLATE	26343-477V
C18	CAP CER 10N 25V 20% DISC	26383-006C
C19	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C20	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C25	CAP CER 100N 30V 20% DISC	26383-031S
C27	CAP CER 10N 25V 20% DISC	26383-006C
C29	CAP CER 10N 25V 20% DISC	26383-006C
C30	CAP CER 82P 63V 2% PLATE	26343-431A
C31	CAP CER 100N 30V 20% DISC	26383-031S
C32	CAP CER 18P 63V 5% PLATE	26343-468Y
C33	CAP VAR PLAS 22P 2P TRIM	26878-407U
C34	CAP CER 47P 63V 5% PLATE	26343-473L
C35	CAP CER 100N 30V 20% DISC	26383-031S
C40	CAP CER 100N 30V 20% DISC	26383-031S
C41	CAP CER 100N 30V 20% DISC	26383-031S
C42	CAP CER 100N 30V 20% DISC	26383-031S
C43	CAP CER 68P 63V 2% PLATE	26343-475F
C44	CAP CER 68P 63V 2% PLATE	26343-475F
C52	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C53	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C54	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C55	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C56	CAP PETP 100N 63V 10% RAD MIN	26582-429F

Circuit Ref	Description		Part Number
Board AC2	- 47.4 MHz i.f. amplifier		(Contd.)
C57	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C58	CAP ELEC 3U3 50V 20% SUBMIN		26421-109Z
C59	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C60	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C61	CAP ELEC 3U3 50V 20% SUBMIN		26421-109Z
C62	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C63	CAP CER 15P 63V 2% N470 PLATE		26343-455N
C64	CAP CER 100P 63V 2% PLATE N150		26343-437N
D1	DI ZEN BZX79C6V8 6.8V 5%		28371-550W
IC1	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC2	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC3	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC4	ICA AMP TL074CN QUAD FET I/P		28461-349H
L1	IND CHOKE .82UH 5%		23642-454V
L2	INDUCTOR		34900-927V
L3	INDUCTOR		34900-927V
L4	INDUCTOR		34900-927V
L5	INDUCTOR		34900-927V
L6	IND CHOKE .22UH 10% LAQ		23642-545E
L7	IND CHOKE 47UH 10% LAQ		23642-559D
L8	IND CHOKE 47UH 10% LAQ		23642-559D
L9	IND CHOKE .68UH 10% LAQ		23642-548N
L10	IND CHOKE .1UH 20% LAQ		23642-543N
	INDUCTOR ASSY		44190-048L
R1	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R2	RES MF 100R 1/4W 2% 100PPM		24773-249J
R3	RES MF 100R 1/4W 2% 100PPM		24773-249J
R4	RES MF 330R 1/4W 2% 100PPM		24773-261D
R5	RES MF 36R 1/4W 2% 100PPM		24773-238A
R6	RES MF 680R 1/4W 2% 100PPM		24773-269K
R7	RES MF 100K 1/4W 2% 100PPM		24773-321L
R8	RES MF 100R 1/4W 2% 100PPM		24773-249J
R9	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R10	RES MF 100R 1/4W 2% 100PPM		24773-249J
R11	RES MF 22R 1/4W 2% 100PPM		24773-233M
R12	RES MF 1K5 1/4W 2% 100PPM		24773-277U
R13	RES MF 20K 1/4W 2% 100PPM		24773-304C
R14	RES MF 10K 1/4W 2% 100PPM		24773-297M
R15	RES MF 47R 1/4W 2% 100PPM		24773-241A
R16	RES MF 2K7 1/4W 2% 100PPM		24773-283L

Circuit Ref	Description	Part Number
Board AC2	- 47.4 MHz i.f. amplifier	(Contd.)
R17	RES MF 100R 1/4W 2% 100PPM	24773-249J
R18	RES CC 51R 1/8W 5%	24331-989P
R19	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R20	RES MF 100R 1/4W 2% 100PPM	24773-249J
R21	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R22	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R23	RES MF 330R 1/4W 2% 100PPM	24773-261D
R24	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R25	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R26	RES MF 100R 1/4W 2% 100PPM	24773-249J
R27	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R28	RES MF 330R 1/4W 2% 100PPM	24773-261D
R29	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R30	RES MF 100R 1/4W 2% 100PPM	24773-249J
R31	RES MF 100R 1/4W 2% 100PPM	24773-249J
R32	RES CC 51R 1/8W 5%	24331-989P
R33	RES CC 51R 1/8W 5%	24331-989P
R34	RES MF 3KO 1/4W 2% 100PPM	24773-284J
R35	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R36	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R37	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R39	RES MF 360R 1/4W 2% 100PPM	24773-262T
R40	RES MF 100K 1/4W 2% 100PPM	24773-321L
R41	RES MF 12K 1/4W 2% 100PPM	24773-299R
R46	RES MF 100R 1/4W 2% 100PPM	24773-249J
R47	RES MF 100R 1/4W 2% 100PPM	24773-249J
R48	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R49	RES MF 180R 1/4W 2% 100PPM	24773-255V
R50	RES MF 1K8 1/4W .1% 25PPM	24723-395F
R51	RES MF 200R 1/4W .1% 25PPM	24723-396G
R52	RES MF 100R 1/4W 2% 100PPM	24773-249J
R53	RES MF 100R 1/4W 2% 100PPM	24773-249J
R54	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R55	RES MF 200R 1/4W 2% 100PPM	24773-256S
R56	RES MF 649R 1/4W .1% 25PPM	24723-398S
R57	RES MF 300R 1/4W .1% 25PPM	24723-397V
R58	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R59	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R60	RES MF 100R 1/4W 2% 100PPM	24773-249J
R61	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R62	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R63	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R64	RES MF 120R 1/4W 2% 100PPM	24773-251L

Circuit Ref	Description	Part Number
Board AC2	- 47.4 MHz i.f. amplifier (Contd.)	
R65	RES MF 100R 1/4W 2% 100PPM	24773-249J
R66	RES MF 180R 1/4W 2% 100PPM	24773-255V
R67	RES MF 1K8 1/4W .1% 25PPM	24723-395F
R68	RES MF 200R 1/4W .1% 25PPM	24723-396G
R69	RES MF 100R 1/4W 2% 100PPM	24773-249J
R70	RES MF 100R 1/4W 2% 100PPM	24773-249J
R71	RES MF 3K0 1/4W 2% 100PPM	24773-284J
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NSI BFY90 15V 1G - AMP	28452-157R
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
TR6	TR NJF U431 25V - 24MA DUA	28459-041G
TR7	TR NSI BFY90 15V 1G - AMP	28452-157R
TR8	TR NSI BFY90 15V 1G - AMP	28452-157R
TR11	TR NSI BC209C 20V 150M - GEN	28452-771P
TR12	TR NSI BC209C 20V 150M - GEN	28452-771P
TR15	TR PSI BC308B 20V 130M - GEN	28433-455R
TR16	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR17	TR NSI BC209C 20V 150M - GEN	28452-771P
T1	TRANSFORMER ASSY.	43590-117W
T2	TRANSFORMER ASSY.	43590-116S
X2	S/C ACC PAD TO5 TO DIL8	28488-102R
X3	S/C ACC PAD TO18 TO .1"GRD ETC.	28488-115L

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter	
35.	When ordering, prefix circuit reference with AC3	
	Complete unit	44828-474A
C1	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C2	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C3	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C4	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C5	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C6	CAP CER 56P 63V 2% PLATE	26343-474J
C7	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C8	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C9	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP CER 3P9 63V 0P5 PLATE	26343-496Z
C12	CAP VAR PLAS 200P 15P TRIM	26878-401B
C13	CAP CER 2N2 100V 5% PLATE	26343-557M
C14	CAP CER 2N2 100V 5% PLATE	26343-557M
C15	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C16	CAP CER 56P 63V 2% PLATE	26343-474J
C17	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C18	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C19	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C20	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C21	CAP CER 15P 63V 5% PLATE	26343-493B
C22	CAP VAR PLAS 200P - 15P TRIM	26878-401B
C23	CAP CER 2N2 100V 5% PLATE	26343-557M
C24	CAP CER 2N2 100V 5% PLATE	26343-557M
C25	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C26	CAP CER 56P 63V 2% PLATE	26343-474J
C27	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C28	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C29	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C30	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C31	CAP CER 3P9 63V 0P5 PLATE	26343-496Z
C32	CAP VAR PLAS 200P 15P TRIM	26878-401B
C33	CAP CER 2N2 100V 5% PLATE	26343-557M
C34	CAP CER 2N2 100V 5% PLATE	26343-557M
C35	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C36	CAP CER 56P 63V 2% PLATE	26343-474J
C37	CAP PETP 100N 63V 10% RAD MIN	26582-429F

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter	(Contd.)
C38	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C39	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C40	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C41	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C42	CAP VAR PLAS 200P 15P TRIM	26878-401B
C43	CAP CER 2N2 100V 5% PLATE	26343-557M
C44	CAP CER 2N2 100V 5% PLATE	26343-557M
C45	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C46	CAP CER 56P 63V 2% PLATE	26343-474J
C47	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C48	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C49	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C50	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C51	CAP CER 15P 63V 5% PLATE	26343-493B
C52	CAP VAR PLAS 200P 15P TRIM	26878-401B
C53	CAP CER 2N2 100V 5% PLATE	26343-557M
C54	CAP CER 2N2 100V 5% PLATE	26343-557M
C55	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C56	CAP CER 56P 63V 2% PLATE	26343-474J
C57	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C58	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C59	CAP CER 3P9 63V 0P5 PLATE	26343-496Z
C60	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C61	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C62	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C63	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C64	CAP CER 15P 63V 5% PLATE	26343-493B
C65	CAP CER 3P9 63V 0P5 PLATE	26343-496Z
C66	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C67	CAP CER 15P 63V 5% PLATE	26343-493B
C68	CAP CER 3P9 63V 0P5 PLATE	26343-496Z
C69	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C70	CAP CER 15P 63V 5% PLATE	26343-493B
C71	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C73	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C74	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C75	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C76	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C77	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C78	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C79	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C80	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C81	CAP CER 1N5 63V 10% PLATE	26383-603U

Circuit Ref	Description		Part Number
Board AC3	- 2.6 MHz LC filter		(Contd.)
C82	CAP CER 1N5 63V 10% PLATE		26383-603U
C83	CAP PETP 47N 63V 10% RAD MIN		26582-428J
D1	DI PIN 5082-3379 50V	!	28383-997T
D2	DI PIN 5082-3379 50V	!	28383-997T
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	DI V/CAP BB809 3V 29PF		28381-132G
D5	DI V/CAP BB809 3V 29PF		28381-132G
D6	DI V/CAP BB809 3V 29PF		28381-132G
D7	DI V/CAP BB809 3V 29PF		28381-132G
D8	DI V/CAP BB809 3V 29PF		28381-132G
D9	DI V/CAP BB809 3V 29PF		28381-132G
D10	DI V/CAP BB809 3V 29PF		28381-132G
D11	DI V/CAP BB809 3V 29PF		28381-132G
D12	DI V/CAP BB809 3V 29PF		28381-132G
D13	DI V/CAP BB809 3V 29PF		28381-132G
IC1	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC2	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC3	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC4	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC5	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC6	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC7	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC8	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC9	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC10	ICA AMP TL072CP DUAL FET I/P		28461-348Z
L1	IND CHOKE 680UH 10% LAQ		23642-566M
L2	IND CHOKE 33UH 10% LAQ		23642-558W
L3	IND CHOKE 33UH 10% LAQ		23642-558W
L11	COIL ASSY.		44190-035R
L12	COIL ASSY.		44190-035R
L13	COIL ASSY.		44190-035R
L14	COIL ASSY.		44190-035R
L15	COIL ASSY.		44190-035R
R1	RES MF 3K09 1/4W .1% 25PPM		24723-399W
R2	RES MF 100R9 1/4W .1% 25PPM		24723-400J
R3	RES MF 100R 1/4W 2% 100PPM		24773-249J
R4	RES MF 1MO 1/4W 2% 100PPM		24773-346E
R6	RES MF 2KO 1/4W 2% 100PPM		24773-280U

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter (Contd.)	
R7	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R8	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R9	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R10	RES MF 18R 1/4W 2% 100PPM	24773-231P
R11	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R12	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R13	RES MF 9K1 1/4W 2% 100PPM	24773-296X
R14	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R15	RES MF 10R 1/4W 2% 100PPM	24773-225W
R16	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R17	RES MF 18R 1/4W 2% 100PPM	24773-231P
R18	RES MF 18R 1/4W 2% 100PPM	24773-231P
R19	RES MF 18R 1/4W 2% 100PPM	24773-231P
R20	RES MF 100R 1/4W 2% 100PPM	24773-249J
R21	RES MF 10K 1/4W 2% 100PPM	24773-297M
R22	RES MF 100R 1/4W 2% 100PPM	24773-249J
R23	RES MF 20K 1/4W 2% 100PPM	24773-304C
R24	RES MF 620R 1/4W 2% 100PPM	24773-268B
R25	RES MF 100R 1/4W 2% 100PPM	24773-249J
R26	RES MF 100R 1/4W 2% 100PPM	24773-249J
R27	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R28	RES MF 18R 1/4W 2% 100PPM	24773-231P
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 10K 1/4W 2% 100PPM	24773-297M
R33	RES MF 10K 1/4W 2% 100PPM	24773-297M
R34	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R35	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R36	RES MF 510R 1/4W 2% 100PPM	24773-266C
R37	RES MF 150R 1/4W 2% 100PPM	24773-253F
R38	RES MF 100R 1/4W 2% 100PPM	24773-249J
R39	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R40	RES MF 240R 1/4W 2% 100PPM	24773-258D
R41	RV THERM 470R 10% DISC	25685-402U
R42	RES MF 10R 1/4W 2% 100PPM	24773-225W
R43	RES MF 100R 1/4W 2% 100PPM	24773-249J
R44	RES MF 620R 1/4W 2% 100PPM	24773-268B
R45	RES MF 100R 1/4W 2% 100PPM	24773-249J
R46	RES MF 20K 1/4W 2% 100PPM	24773-304C
R47	RES MF 100R 1/4W 2% 100PPM	24773-249J
R48	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R49	RES MF 1M0 1/4W 2% 100PPM	24773-346E

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter	(Contd.)
R50	RES MF 10K 1/4W 2% 100PPM	24773-297M
R51	RES MF 10K 1/4W 2% 100PPM	24773-297M
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 10K 1/4W 2% 100PPM	24773-297M
R54	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R55	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R56	RES MF 510R 1/4W 2% 100PPM	24773-266C
R57	RES MF 150R 1/4W 2% 100PPM	24773-253F
R58	RES MF 100R 1/4W 2% 100PPM	24773-249J
R59	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R60	RES MF 240R 1/4W 2% 100PPM	24773-258D
R61	RV THERM 470R 10% DISC	25685-402U
R62	RES MF 10R 1/4W 2% 100PPM	24773-225W
R63	RES MF 100R 1/4W 2% 100PPM	24773-249J
R64	RES MF 620R 1/4W 2% 100PPM	24773-268B
R65	RES MF 100R 1/4W 2% 100PPM	24773-249J
R66	RES MF 20K 1/4W 2% 100PPM	24773-304C
R67	RES MF 100R 1/4W 2% 100PPM	24773-249J
R68	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R69	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R70	RES MF 10K 1/4W 2% 100PPM	24773-297M
R71	RES MF 10K 1/4W 2% 100PPM	24773-297M
R72	RES MF 10K 1/4W 2% 100PPM	24773-297M
R73	RES MF 10K 1/4W 2% 100PPM	24773-297M
R74	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R75	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R76	RES MF 510R 1/4W 2% 100PPM	24773-266C
R77	RES MF 150R 1/4W 2% 100PPM	24773-253F
R78	RES MF 100R 1/4W 2% 100PPM	24773-249J
R79	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R80	RES MF 240R 1/4W 2% 100PPM	24773-258D
R81	RV THERM 470R 10% DISC	25685-402U
R82	RES MF 10R 1/4W 2% 100PPM	24773-225W
R83	RES MF 100R 1/4W 2% 100PPM	24773-249J
R84	RES MF 620R 1/4W 2% 100PPM	24773-268B
R85	RES MF 100R 1/4W 2% 100PPM	24773-249J
R86	RES MF 20K 1/4W 2% 100PPM	24773-304C
R87	RES MF 100R 1/4W 2% 100PPM	24773-249J
R88	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R89	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R90	RES MF 10K 1/4W 2% 100PPM	24773-297M
R91	RES MF 10K 1/4W 2% 100PPM	24773-297M
R92	RES MF 10K 1/4W 2% 100PPM	24773-297M

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter	(Contd.)
R93	RES MF 10K 1/4W 2% 100PPM	24773-297M
R94	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R95	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R96	RES MF 510R 1/4W 2% 100PPM	24773-266C
R97	RES MF 150R 1/4W 2% 100PPM	24773-253F
R98	RES MF 100R 1/4W 2% 100PPM	24773-249J
R99	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R100	RES MF 240R 1/4W 2% 100PPM	24773-258D
R101	RV THERM 470R 10% DISC	25685-402U
R102	RES MF 10R 1/4W 2% 100PPM	24773-225W
R103	RES MF 100R 1/4W 2% 100PPM	24773-249J
R104	RES MF 620R 1/4W 2% 100PPM	24773-268B
R105	RES MF 100R 1/4W 2% 100PPM	24773-249J
R106	RES MF 20K 1/4W 2% 100PPM	24773-304C
R107	RES MF 100R 1/4W 2% 100PPM	24773-249J
R108	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R109	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R110	RES MF 10K 1/4W 2% 100PPM	24773-297M
R111	RES MF 10K 1/4W 2% 100PPM	24773-297M
R112	RES MF 10K 1/4W 2% 100PPM	24773-297M
R113	RES MF 10K 1/4W 2% 100PPM	24773-297M
R114	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R115	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R116	RES MF 510R 1/4W 2% 100PPM	24773-266C
R117	RES MF 150R 1/4W 2% 100PPM	24773-253F
R118	RES MF 100R 1/4W 2% 100PPM	24773-249J
R119	RV CERM 2KO LIN .5W 10% HORZ	25711-639V
R120	RES MF 240R 1/4W 2% 100PPM	24773-258D
R121	RV THERM 470R 10% DISC	25685-402U
R122	RES MF 10R 1/4W 2% 100PPM	24773-225W
R123	RES MF 100R 1/4W 2% 100PPM	24773-249J
R124	RES MF 330R 1/4W 2% 100PPM	24773-261D
R125	RES MF 100R 1/4W 2% 100PPM	24773-249J
R126	RES MF 20K 1/4W 2% 100PPM	24773-304C
R127	RES MF 100R 1/4W 2% 100PPM	24773-249J
R128	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R129	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R130	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R131	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R132	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R133	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R134	RES MF 1MO 1/4W 2% 100PPM	24773-346E

Circuit Ref	Description	Part Number
Board AC3	- 2.6 MHz LC filter	(Contd.)
R135	RES MF 20K 1/4W 2% 100PPM	24773-304C
R136	RES MF 10K 1/4W 2% 100PPM	24773-297M
R137	RES MF 100K 1/4W 2% 100PPM	24773-321L
R138	RES MF 11K 1/4W 2% 100PPM	24773-298C
R142	RES MF 10R 1/4W 2% 100PPM	24773-225W
R144	RES MF 510R 1/4W 2% 100PPM	24773-266C
R145	RES MF 100R 1/4W 2% 100PPM	24773-249J
R146	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R147	RES MF 3K 1/4W 2% 100PPM	24773-284J
R148	RES MF 68K 1/4W 2% 100PPM	24773-317N
R149	RES MF 470K 1/4W 2% 100PPM	24773-337R
R150	RES MF 240R 1/4W 2% 100PPM	24773-258D
R151	RV CERM 20KO LIN .5W 10% VERT	25711-611S
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR3	TR NSI BC209C 20V 150M - GEN	28452-771P
TR4	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR NSI BC209C 20V 150M - GEN	28452-771P
TR8	TR NSI BC209C 20V 150M - GEN	28452-771P
TR9	TR NSI BC209C 20V 150M - GEN	28452-771P
TR10	TR NSI BC209C 20V 150M - GEN	28452-771P
TR11	TR NSI BC209C 20V 150M - GEN	28452-771P
TR12	TR NSI BC209C 20V 150M - GEN	28452-771P
TR13	TR NSI BC209C 20V 150M - GEN	28452-771P
TR14	TR NSI BC209C 20V 150M - GEN	28452-771P
TR15	TR NSI BC209C 20V 150M - GEN	28452-771P
TR16	TR NSI BC209C 20V 150M - GEN	28452-771P
TR17	TR NJF BF245B 30V 6MA	28459-048X
TR18	TR NSI 2N3904 40V 250M - GEN	28454-786H
T1	TRANSFORMER	43590-115V
X1	S/C ACC PAD CBE TO TO5	28488-108E
X2	S/C ACC PAD CBE TO TO5	28488-108E

Circuit Ref	Description	Part Number
Board AC4	- 100 kHz i.f. crystal filter	
36.	When ordering, prefix circuit reference with AC4	
	Complete unit	44828-475Z
C1	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C2	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C3	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C4	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C5	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C6	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C7	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C9	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C10	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C11	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C12	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C13	CAP CER 150P 63V 2% PLATE	26343-479W
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C20	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C21	CAP CER 18P 63V 5% PLATE	26343-468Y
C22	CAP CER 27P 63V 5% PLATE	26343-470U
C23	CAP VAR PLAS 22P 2P TRIM	26878-407U
C24	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C25	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C26	CAP CER 18P 63V 5% PLATE	26343-468Y
C30	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C31	CAP CER 56P 63V 2% PLATE	26343-474J
C32	CAP VAR PLAS 22P 2P TRIM	26878-407U
C40	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C41	CAP CER 18P 63V 5% PLATE	26343-468Y
C42	CAP CER 27P 63V 5% PLATE	26343-470U
C43	CAP VAR PLAS 22P 2P TRIM	26878-407U
C44	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C45	CAP CER 18P 63V 5% PLATE	26343-468Y
C50	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C51	CAP CER 56P 63V 2% PLATE	26343-474J
C52	CAP VAR PLAS 22P 2P TRIM	26878-407U
C60	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C61	CAP CER 18P 63V 5% PLATE	26343-468Y
C62	CAP CER 27P 63V 5% PLATE	26343-470U
C63	CAP VAR PLAS 22P 2P TRIM	26878-407U
C64	CAP PETP 220N 63V 10% RAD MIN	26582-430L

Circuit Ref	Description	Part Number
Board AC4	- 100 kHz i.f. crystal filter	(Contd.)
C65	CAP CER 18P 63V 5% PLATE	26343-468Y
C70	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C71	CAP CER 56P 63V 2% PLATE	26343-474J
C72	CAP VAR PLAS 22P 2P TRIM	26878-407U
C80	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C81	CAP CER 18P 63V 5% PLATE	26343-468Y
C82	CAP CER 27P 63V 5% PLATE	26343-470U
C83	CAP VAR PLAS 22P 2P TRIM	26878-407U
C84	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C85	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C86	CAP CER 18P 63V 5% PLATE	26343-468Y
C87	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C88	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C90	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C91	CAP CER 33P 63V 5% PLATE	26343-471Y
C92	CAP VAR PLAS 22P 2P TRIM	26878-407U
C100	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C101	CAP CER 18P 63V 5% PLATE	26343-468Y
C102	CAP CER 27P 63V 5% PLATE	26343-470U
C103	CAP VAR PLAS 22P 2P TRIM	26878-407U
C104	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C106	CAP CER 18P 63V 5% PLATE	26343-468Y
C110	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C111	CAP CER 56P 63V 2% PLATE	26343-474J
C112	CAP VAR PLAS 22P 2P TRIM	26878-407U
C120	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C122	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C123	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C124	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C125	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C126	CAP CER 2N2 63V 10% PLATE	26383-587R
C127	CAP CER 2N2 63V 10% PLATE	26383-587R
C128	CAP CER 2N2 63V 10% PLATE	26383-587R
C129	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C130	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C131	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C132	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C133	CAP CER 4P7 63V 0P5 PLATE	26343-485P
C134	CAP PETP 10N 63V 10% RAD MIN	26582-426N
D1	DI V/CAP BB809 3V 29PF	28381-132G
D2	DI V/CAP BB809 3V 29PF	28381-132G
D3	DI V/CAP BB809 3V 29PF	28381-132G
D4	DI V/CAP BB809 3V 29PF	28381-132G

Circuit Ref	Description		Part Number
Board AC4	- 100 kHz i.f. crystal filter		(Contd.)
D5	DI V/CAP BB809 3V 29PF		28381-132G
D6	DI H/CARR BAT29 5V	!	28349-014L
D7	DI H/CARR BAT29 5V	!	28349-014L
IC1	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC2	ICD FF D 74S74 DUAL +EDG TR		28462-607K
IC3	ICD NAND 74LS03 QUAD 2INP O/C		28466-346E
IC4	ICD NAND 74LS03 QUAD 2INP O/C		28466-346E
IC5	ICD NAND 74LS03 QUAD 2INP O/C		28466-346E
IC6	ICD INV 74HCT04 HEX	!	28469-144S
IC7	ICA SW SD5002 QUAD DMOS	!	28469-717Y
IC11	ICA AMP TL072CP DUAL FET I/P		28461-348Z
L1	IND CHOKE 150UH 10% LAQ		23642-562D
L2	IND CHOKE 22MH 10% MOULDED AX		23642-401C
L3	IND CHOKE 22MH 10% MOULDED AX		23642-401C
L4	IND CHOKE 22MH 10% MOULDED AX		23642-401C
L5	IND CHOKE 22MH 10% MOULDED AX		23642-401C
L6	IND CHOKE 22MH 10% MOULDED AX		23642-401C
L7	IND CHOKE 470UH 10% LAQ		23642-565X
L8	IND CHOKE 1MH 10% LAQ		23642-567C
R1	RES MF 10K 1/4W 2% 100PPM		24773-297M
R2	RES MF 10K 1/4W 2% 100PPM		24773-297M
R3	RES MF 62R 1/4W 2% 100PPM		24773-244E
R4	RES MF 1K2 1/4W 2% 100PPM		24773-275H
R5	RES MF 12K 1/4W 2% 100PPM		24773-299R
R7	RES MF 2KO 1/4W 2% 100PPM		24773-280U
R9	RES MF 47K 1/4W 2% 100PPM		24773-313H
R10	RES MF 2KO 1/4W 2% 100PPM		24773-280U
R11	RES MF 100R 1/4W 2% 100PPM		24773-249J
R12	RES MF 330R 1/4W 2% 100PPM		24773-261D
R13	RV CERM 5KO LIN .5W 10% HORZ		25711-640F
R14	RES MF 22K 1/4W 2% 100PPM		24773-305R
R15	RV CERM 50K LIN .5W 10% HORZ		25711-643S
R16	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R17	RV CERM 50K LIN .5W 10% HORZ		25711-643S
R18	RES MF 1K2 1/4W 2% 100PPM		24773-275H
R19	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R20	RES MF 100R 1/4W 2% 100PPM		24773-249J
R21	RES MF 3K3 1/4W 2% 100PPM		24773-285F
R22	RES MF 510R 1/4W 2% 100PPM		24773-266C
R23	RES MF 6K8 1/4W 2% 100PPM		24773-293D
R24	RES MF 1K5 1/4W 2% 100PPM		24773-277U
R25	RV CERM 1KO LIN .5W 10% HORZ		25711-638G
R26	RES MF 100R 1/4W 2% 100PPM		24773-249J

Circuit Ref	Description	Part Number
Board AC4	- 100 kHz i.f. crystal filter	(Contd.)
R27	RES MF 13K 1/4W 2% 100PPM	24773-300T
R28	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R29	RES MG 4M7 1/4W 5%	24321-881F
R30	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R32	RES MF 39K 1/4W 2% 100PPM	24773-311A
R33	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R34	RES MF 330R 1/4W 2% 100PPM	24773-261D
R35	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R36	RES MF 820R 1/4W 2% 100PPM	24773-271B
R37	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R38	RES MG 4M7 1/4W 5%	24321-881F
R39	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R40	RES MF 100R 1/4W 2% 100PPM	24773-249J
R41	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R42	RES MF 510R 1/4W 2% 100PPM	24773-266C
R43	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R44	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R45	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R46	RES MF 100R 1/4W 2% 100PPM	24773-249J
R47	RES MF 13K 1/4W 2% 100PPM	24773-300T
R48	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R52	RES MF 39K 1/4W 2% 100PPM	24773-311A
R58	RES MG 4M7 1/4W 5%	24321-881F
R59	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R60	RES MF 100R 1/4W 2% 100PPM	24773-249J
R61	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R62	RES MF 510R 1/4W 2% 100PPM	24773-266C
R63	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R64	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R65	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R66	RES MF 100R 1/4W 2% 100PPM	24773-249J
R67	RES MF 13K 1/4W 2% 100PPM	24773-300T
R68	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R72	RES MF 39K 1/4W 2% 100PPM	24773-311A
R78	RES MG 4M7 1/4W 5%	24321-881F
R79	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R80	RES MF 100R 1/4W 2% 100PPM	24773-249J
R81	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R82	RES MF 510R 1/4W 2% 100PPM	24773-266C
R83	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R84	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R85	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R86	RES MF 120K 1/4W 2% 100PPM	24773-323F

Circuit Ref	Description	Part Number
Board AC4	- 100 kHz i.f. crystal filter	(Contd.)
R87	RES MF 13K 1/4W 2% 100PPM	24773-300T
R88	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R89	RES MF 100R 1/4W 2% 100PPM	24773-249J
R92	RES MF 39K 1/4W 2% 100PPM	24773-311A
R93	RES MF 47K 1/4W 2% 100PPM	24773-313H
R94	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R95	RES MF 270R 1/4W 2% 100PPM	24773-259T
R96	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R98	RES MG 4M7 1/4W 5%	24321-881F
R99	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R100	RES MF 100R 1/4W 2% 100PPM	24773-249J
R101	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R102	RES MF 510R 1/4W 2% 100PPM	24773-266C
R103	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R104	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R105	RV CERM 1K0 LIN .5W 10% HORZ	25711-638G
R106	RES MF 100R 1/4W 2% 100PPM	24773-249J
R107	RES MF 13K 1/4W 2% 100PPM	24773-300T
R108	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R109	RES MF 10K 1/4W 2% 100PPM	24773-297M
R110	RES MF 10K 1/4W 2% 100PPM	24773-297M
R112	RES MF 39K 1/4W 2% 100PPM	24773-311A
R119	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R120	RES MF 100R 1/4W 2% 100PPM	24773-249J
R121	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R122	RES MF 100R 1/4W 2% 100PPM	24773-249J
R123	RES MF 100R 1/4W 2% 100PPM	24773-249J
R124	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R125	RES MF 10K 1/4W 2% 100PPM	24773-297M
R126	RES MF 10K 1/4W 2% 100PPM	24773-297M
R127	RES MF 10K 1/4W 2% 100PPM	24773-297M
R128	RES MF 27K 1/4W 2% 100PPM	24773-307K
R129	RES MF 12K 1/4W 2% 100PPM	24773-299R
R130	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R131	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R132	RES MF 43K 1/4W 2% 100PPM	24773-312Z
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR NSI BC209C 20V 150M - GEN	28452-771P
TR8	TR NSI BC208B 20V 150M - GEN	28452-781A
TR9	TR NSI BC209C 20V 150M - GEN	28452-771P
TR10	TR NSI BC208B 20V 150M - GEN	28452-781A

Circuit Ref	Description	Part Number
Unit AC4	- 100 kHz i.f. crystal filter	(Contd.)
TR13	TR NSI BC209C 20V 150M - GEN	28452-771P
TR14	TR NSI BC208B 20V 150M - GEN	28452-781A
TR15	TR NSI BC209C 20V 150M - GEN	28452-771P
TR16	TR NSI BC208B 20V 150M - GEN	28452-781A
TR18	TR NSI BC209C 20V 150M - GEN	28452-771P
TR19	TR NSI BC209C 20V 150M - GEN	28452-771P
TR20	TR NSI BC208B 20V 150M - GEN	28452-781A
TR21	TR PSI BC308B 20V 130M - GEN	28433-455R
TR22	TR NSI BC209C 20V 150M - GEN	28452-771P
T1	TRANSFORMER ASSY.	43590-118D
T2	BALUN TRANS ASSY	43590-129K
T3	BALUN TRANS	43590-114G
T4	TRANSFORMER ASSY	43590-158C
T5	TRANSFORMER ASSY	43590-158C
XL1	XTAL 0.1M S50P 750R 60H SET 5	28311-372U
XL2	XTAL 0.1M S50P 750R 60H SET 5	28311-372U
XL3	XTAL 0.1M S50P 750R 60H SET 5	28311-372U
XL4	XTAL 0.1M S50P 750R 60H SET 5	28311-372U
XL5	XTAL 0.1M S50P 750R 60H SET 5	28311-372U

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	
37.	When ordering, prefix circuit reference with AC5	
	Complete unit	44828-476H
C1	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C2	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C3	CAP CER 27P 63V 5% PLATE	26343-470U
C4	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C5	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C6	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C7	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C8	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C9	CAP VAR PLAS 5P5 1P4 TRIM	26878-409N
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP CER 10P 63V 0P5 PLATE	26343-465H
C12	CAP VAR PLAS 22P 2P TRIM	26878-407U
C13	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C15	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C16	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C17	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C18	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C19	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C20	CAP VAR PLAS 5P5 1P4 TRIM	26878-409N
C21	CAP CER 10P 63V 0P5 PLATE	26343-465H
C22	CAP VAR PLAS 22P 2P TRIM	26878-407U
C23	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C24	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C25	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C27	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C28	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C29	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C30	CAP CER 10P 63V 0P5 PLATE	26343-465H
C31	CAP VAR PLAS 5P5 1P4 TRIM	26878-409N
C32	CAP CER 10P 63V 0P5 PLATE	26343-465H
C33	CAP VAR PLAS 22P 2P TRIM	26878-407U
C34	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C35	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C36	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C37	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C38	CAP PETP 100N 63V 10% RAD MIN	26582-429F

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
C39	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C40	CAP VAR PLAS 5P5 1P4 TRIM	26878-409N
C41	CAP CER 10P 63V 0P5 PLATE	26343-465H
C42	CAP VAR PLAS 22P 2P TRIM	26878-407U
C43	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C44	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C45	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C46	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C47	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C49	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C51	CAP VAR PLAS 5P5 1P4 TRIM	26878-409N
C52	CAP CER 10P 63V 0P5 PLATE	26343-465H
C53	CAP VAR PLAS 22P 2P TRIM	26878-407U
C54	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C55	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C56	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C57	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C58	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C59	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C60	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C61	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C62	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C64	CAP CER 10P 63V 0P5 PLATE	26343-465H
C65	CAP CER 10P 63V 0P5 PLATE	26343-465H
C66	CAP CER 10P 63V 0P5 PLATE	26343-465H
C67	CAP CER 10P 63V 0P5 PLATE	26343-465H
C68	CAP PETP 100N 63V 10% RAD MIN	26582-429F
D1	DI V/CAP BB405B 3V 11.5PF	28381-101V
D2	DI SIL 1N3062 75V JUNC	28336-248R
D3	DI SIL 1N3062 75V JUNC	28336-248R
D4	DI SIL 1N3062 75V JUNC	28336-248R
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI V/CAP BB405B 3V 11.5PF	28381-101V
D7	DI SIL 1N3062 75V JUNC	28336-248R
D8	DI SIL 1N3062 75V JUNC	28336-248R
D9	DI SIL 1N3062 75V JUNC	28336-248R
D10	DI SIL 1N4148 75V JUNC	28336-676J
D11	DI V/CAP BB405B 3V 11.5PF	28381-101V
D12	DI SIL 1N3062 75V JUNC	28336-248R
D13	DI SIL 1N3062 75V JUNC	28336-248R
D14	DI SIL 1N3062 75V JUNC	28336-248R
D15	DI SIL 1N4148 75V JUNC	28336-676J
D16	DI V/CAP BB405B 3V 11.5PF	28381-101V

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
D17	DI SIL 1N3062 75V JUNC	28336-248R
D18	DI SIL 1N3062 75V JUNC	28336-248R
D19	DI SIL 1N3062 75V JUNC	28336-248R
D20	DI SIL 1N4148 75V JUNC	28336-676J
D21	DI V/CAP BB405B 3V 11.5PF	28381-101V
D22	DI SIL 1N3062 75V JUNC	28336-248R
D23	DI SIL 1N3062 75V JUNC	28336-248R
D24	DI SIL 1N3062 75V JUNC	28336-248R
D25	DI SIL 1N4148 75V JUNC	28336-676J
D26	DI V/CAP BB405B 3V 11.5PF	28381-101V
D27	DI V/CAP BB405B 3V 11.5PF	28381-101V
D28	DI V/CAP BB405B 3V 11.5PF	28381-101V
D29	DI V/CAP BB405B 3V 11.5PF	28381-101V
D30	DI V/CAP BB405B 3V 11.5PF	28381-101V
D31	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA AMP TL074CN QUAD FET I/P	28461-349H
L1	IND CHOKE 100UH 10% LAQ	23642-561W
L2	INDUCTOR	44290-869W
L3	INDUCTOR	44290-869W
L4	INDUCTOR	44290-869W
L5	INDUCTOR	44290-869W
L6	INDUCTOR	44290-869W
R1	RES MF 10K 1/4W 2% 100PPM	24773-297M
R2	RES MF 39K 1/4W 2% 100PPM	24773-311A
R3	RES MF 100R 1/4W 2% 100PPM	24773-249J
R4	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R5	RES MF 47K 1/4W 2% 100PPM	24773-313H
R6	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R7	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R8	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R9	RES MF 47K 1/4W 2% 100PPM	24773-313H
R10	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R11	RV CERM 5K0 LIN .5W 10% HORZ	25711-640F
R12	RES MF 10R 1/4W 2% 100PPM	24773-225W
R13	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R14	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R15	RES MF 100R 1/4W 2% 100PPM	24773-249J
R16	RES MF 2K0 1/4W 2% 100PPM	24773-280U

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
R17	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R18	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R19	RES MF 100R 1/4W 2% 100PPM	24773-249J
R20	RES MF 10R 1/4W 2% 100PPM	24773-225W
R21	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R22	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R23	RES MF 27K 1/4W 2% 100PPM	24773-307K
R24	RES MF 12K 1/4W 2% 100PPM	24773-299R
R25	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R26	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R27	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R28	RES MF 100K 1/4W 2% 100PPM	24773-321L
R29	RES MF 470K 1/4W 2% 100PPM	24773-337R
R30	RES MF 820R 1/4W 2% 100PPM	24773-271B
R31	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R32	RES MF 15K 1/4W 2% 100PPM	24773-301P
R33	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R34	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R35	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R36	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R37	RES MF 100R 1/4W 2% 100PPM	24773-249J
R38	RES MF 100R 1/4W 2% 100PPM	24773-249J
R39	RES MF 15K 1/4W 2% 100PPM	24773-301P
R40	RES MF 100R 1/4W 2% 100PPM	24773-249J
R41	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R42	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R43	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R44	RES MF 56K 1/4W 2% 100PPM	24773-315U
R45	RES MF 820R 1/4W 2% 100PPM	24773-271B
R46	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R47	RES MF 15K 1/4W 2% 100PPM	24773-301P
R48	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R49	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R50	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R51	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R52	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R53	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R54	RES MF 100R 1/4W 2% 100PPM	24773-249J
R55	RES MF 100R 1/4W 2% 100PPM	24773-249J
R56	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R57	RES MO 470R 1/2W 2% 250PPM	24573-065J
R58	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R59	RV CERM 100K LIN .5W 10% HORZ	25711-644W

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
R60	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R61	RES MF 820R 1/4W 2% 100PPM	24773-271B
R62	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R63	RES MF 15K 1/4W 2% 100PPM	24773-301P
R64	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R65	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R66	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R67	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R68	RES MF 100R 1/4W 2% 100PPM	24773-249J
R69	RES MF 15K 1/4W 2% 100PPM	24773-301P
R70	RES MF 100R 1/4W 2% 100PPM	24773-249J
R71	RES MF 100R 1/4W 2% 100PPM	24773-249J
R72	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R73	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R74	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R75	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R76	RES MF 820R 1/4W 2% 100PPM	24773-271B
R77	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R78	RES MF 15K 1/4W 2% 100PPM	24773-301P
R79	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R80	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R81	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R82	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R83	RES MF 100R 1/4W 2% 100PPM	24773-249J
R84	RES MF 100R 1/4W 2% 100PPM	24773-249J
R85	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R86	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R87	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R88	RES MO 470R 1/2W 2% 250PPM	24573-065J
R89	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R90	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R91	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R92	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R93	RES MF 820R 1/4W 2% 100PPM	24773-271B
R94	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R95	RES MF 15K 1/4W 2% 100PPM	24773-301P
R96	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R97	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R98	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R99	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R100	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R101	RES MF 100R 1/4W 2% 100PPM	24773-249J

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
R102	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R103	RES MF 10R 1/4W 2% 100PPM	24773-225W
R104	RES MF 100R 1/4W 2% 100PPM	24773-249J
R105	RES MF 10R 1/4W 2% 100PPM	24773-225W
R106	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R107	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R108	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R109	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R110	RES MF 56K 1/4W 2% 100PPM	24773-315U
R111	RES MF 20K 1/4W 2% 100PPM	24773-304C
R112	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R113	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R114	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R115	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R116	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R117	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R118	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R119	RES MF 470K 1/4W 2% 100PPM	24773-337R
R120	RES MF 100K 1/4W 2% 100PPM	24773-321L
R121	RES MF 1/4W 2% 100PPM	24773-302X
TR1	TR PSI 2N4959 30V 1G - LN AMP	28433-836K
TR2	TR PSI MPSL08 12V 700M - SW	28431-767E
TR3	TR PSI MPSL08 12V 700M - SW	28431-767E
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
TR5	TR NSI BC209C 20V 150M - GEN	28452-771P
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR NSI BC209C 20V 150M - GEN	28452-771P
TR8	TR NSI BC209C 20V 150M - GEN	28452-771P
TR9	TR NSI 2N2219A 40V 300M - GEN	28454-804V
TR10	TR NSI BC209C 20V 150M - GEN	28452-771P
TR11	TR NSI BC209C 20V 150M - GEN	28452-771P
TR12	TR NSI BC209C 20V 150M - GEN	28452-771P
TR13	TR NSI 2N2219A 40V 300M - GEN	28454-804V
TR14	TR PSI BCY71 45V 200M - GEN	28435-235L
TR15	TR NSI 2N2219A 40V 300M - GEN	28454-804V
TR16	TR NJF BF245B 30V 6MA	28459-048X
TR17	TR NJF BF245B 30V 6MA	28459-048X
T1	TRANSFORMER	43590-148S
T2	TRANSFORMER	43590-148S
T3	TRANSFORMER	43590-148S
T4	TRANSFORMER	43590-148S
T5	TRANSFORMER	43590-148S

Circuit Ref	Description	Part Number
Board AC5	- 2.6 MHz crystal filter	(Contd.)
X1	S/C ACC PAD CBE TO TO5	28488-108E
X2	S/C ACC PAD CBE TO TO5	28488-113Y
X3	S/C ACC PAD TO18	28488-115L
XL1	XTAL 2.6M S30P 100R 0.44H B	28312-089V
XL2	XTAL 2.6M S30P 100R 0.47H A	28312-090F
XL3	XTAL 2.6M S30P 100R 0.44H B	28312-089V
XL4	XTAL 2.6M S30P 100R 0.47H A	28312-090F
XL5	XTAL 2.6M S30P 100R 0.44H B	28312-089V

Circuit Ref	Description	Part Number
Board AC6	- Phase detector	
38.	When ordering, prefix circuit reference with AC6	
	Complete unit	44828-477E
C1	CAP CER 22N 18V 20% DISC	26383-007R
C2	CAP CER 330P 63V 2% PLATE	26343-483D
C3	CAP CER 22N 18V 20% DISC	26383-007R
C4	CAP CER 470P 400V 20% DISC	26383-139M
C5	CAP PETP 68N 100V 10% RAD	26582-224J
C6	CAP PETP 220N 63V 10% RAD	26582-406T
C7	CAP PETP 220N 63V 10% RAD	26582-406T
C8	CAP ELEC 4U7 50V 20% L/LEAK	26421-011H
C9	CAP CER 100P 63V 2% PLATE	26343-477V
C10	CAP CER 4N7 63V 10% PLATE	26383-591B
C11	CAP CER 22N 18V 20% DISC	26383-007R
C12	CAP CER 4N7 63V 10% PLATE	26383-591B
C13	CAP CER 4N7 63V 10% PLATE	26383-591B
C14	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C15	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C16	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C17	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C18	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C19	CAP CER 15P 63V 5% PLATE	26343-467U
D1	DI SIL 1N3062 75V JUNC	28336-248R
D2	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA AMP TL071CP FET I/P DIL8	28461-347A
IC2	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC3	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC4	ICD MONO 74LS122 RETR	28468-310C
IC5	ICD CTR 74LS92 4BIT 2,6,12	28464-125M
IC6	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
IC7	ICD CTR 74LS92 4BIT 2,6,12	28464-125M
IC8	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
IC9	ICD CTR 74S196 4BIT DEC	28464-010J
IC10	ICD INV 74LS04 HEX	28469-171L
L1	CHOKE	44190-039Z
L2	IND CHOKE 15UH 10% LAQ	23642-556V

Circuit Ref	Description	Part Number
Board AC6	- Phase detector	(Contd.)
R1	RES MF 10K 1/4W 2% 100PPM	24773-297M
R2	RES MF 100K 1/4W 2% 100PPM	24773-321L
R3	RES MF 10K 1/4W 2% 100PPM	24773-297M
R4	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R5	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES MF 56K 1/4W 2% 100PPM	24773-315U
R7	RES MF 360K 1/4W 2% 100PPM	24773-334X
R8	RES MF 680K 1/4W 2% 100PPM	24773-342K
R9	RES MF 20K 1/4W 2% 100PPM	24773-304C
R10	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R11	RES MF 240K 1/4W 2% 100PPM	24773-330W
R12	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R13	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R14	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R15	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R16	RES MF 100R 1/4W 2% 100PPM	24773-249J
R17	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R18	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R19	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R20	RES MF 10R 1/4W 2% 100PPM	24773-225W
R21	RES MF 75K 1/4W 2% 100PPM	24773-318L
R22	RES MF 160R 1/4W 2% 100PPM	24773-254G
R23	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R24	RES MF 2K0 1/4W 2% 100PPM	24773-280U
TR1	TR PSI 2N4959 30V 1G - LN AMP	28433-836K
TR2	TR NJF BF245B 30V 6MA	28459-048X
TR3	TR PSI MPSL08 12V 700M - SW	28431-767E
TR4	TR NSI 2N2369 15V 500M - SW	28452-197H
TR5	TR PSI MPSL08 12V 700M - SW	28431-767E
X3	S/C ACC PAD CBE TO TO5	28488-108E

Circuit Ref	Description	Part Number
Unit AD0	- AD tray	
39.	When ordering, prefix circuit reference with AD0	
	Complete unit	44990-467K
C1	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C3	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C5	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 22P 300V 10%+ L/T SOL	26373-226Z
C29	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C30	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C31	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C32	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C33	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C34	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C35	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C36	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C37	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C38	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C39	CAP CER 22P 300V 10% L/T SOL	26333-226Z

Circuit Ref	Description	Part Number
Unit AD0	- AD tray	(Contd.)
C40	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C41	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C42	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C43	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C44	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C45	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C49	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C50	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1N0 300V 20% L/T SOL	26333-733K
C53	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C57	CAP CER 200P 500V 20% L/T SCR	26333-568H
C58	CAP CER 47P 63V 5% PLATE	26343-473L
C59	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C60	CAP CER 22P 300V 10% L/T SOL	26333-226Z
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR	34900-918Y
L3	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR	34900-918Y
L5	INDUCTOR CHOKE GEN	44190-036B
L6	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR CHOKE GEN	44190-036B
L9	INDUCTOR CHOKE GEN	44190-036B
L10	INDUCTOR CHOKE GEN	44190-036B
L11	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR CHOKE GEN	44190-036B
L13	INDUCTOR CHOKE GEN	44190-036B
L14	INDUCTOR CHOKE GEN	44190-036B
L15	INDUCTOR CHOKE GEN	44190-036B
L16	INDUCTOR CHOKE GEN	44190-036B
L17	INDUCTOR CHOKE GEN	44190-036B
L18	INDUCTOR CHOKE GEN	44190-036B
L19	INDUCTOR CHOKE GEN	44190-036B
L20	INDUCTOR CHOKE GEN	44190-036B
L22	INDUCTOR CHOKE GEN	44190-036B
L24	INDUCTOR CHOKE GEN	44190-036B
L25	INDUCTOR CHOKE GEN	44190-036B
L26	INDUCTOR CHOKE GEN	44190-036B
L27	IND CHOKE 470UH 10% SCREENED	23642-333B

Circuit Ref	Description	Part Number
Unit AD0	- AD tray	(Contd.)
L28	INDUCTOR CHOKE GEN	44190-036B
L29	IND CHOKE .22UH 10% LAQ	23642-545E
L30	INDUCTOR ASSY	44190-052J
R1	RES MF 270R 1/4W 2% 100PPM	24773-259T
R2	RES MF 270R 1/4W 2% 100PPM	24773-259T
	CABLE ASSY 26-WAY RIBBON	43129-951Y
	CABLE ASSY 16-WAY RIBBON	43129-955F
	CABLE ASSY 16-WAY RIBBON	43129-956G
	CABLE ASSY AD4-'EXT STD'	43130-246R
	CABLE ASSY	43130-470J

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	
40.	When ordering, prefix circuit reference with AD1	
	Complete unit	44828-479Y
C1	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C2	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C3	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C4	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C5	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C6	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
C8	CAP CER 100P 63V 2% PLATE	26343-477V
C9	CAP CER 1N0 63V 10% PLATE	26383-585M
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP CER 12P 63V 5% PLATE	26343-466E
C12	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C13	CAP CER 4P7 63V 0P5 PLATE	26343-461B
C14	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C15	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C16	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C17	CAP CER 1N0 63V 10% PLATE	26383-602E
C18	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C19	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C20	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C21	CAP CER 1N0 63V 10% PLATE	26383-585M
C22	CAP CER 12P 63V 5% PLATE	26343-466E
C23	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C24	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C25	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C26	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C27	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C28	CAP CER 1N0 63V 10% PLATE	26383-602E
C29	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C30	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C31	CAP CER 1N0 63V 10% PLATE	26383-585M
C32	CAP CER 12P 63V 5% PLATE	26343-466E
C33	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C34	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C35	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C36	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C37	CAP CER 1N0 63V 10% PLATE	26383-602E

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
C38	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C39	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C40	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C41	CAP CER 1N0 63V 10% PLATE	26383-585M
C42	CAP CER 12P 63V 5% PLATE	26343-466E
C43	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C44	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C45	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C46	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C47	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C48	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C49	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C50	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C51	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C52	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C53	CAP CER 100P 63V 2% PLATE	26343-477V
C54	CAP CER 10N 25V 20% DISC	26383-006C
C55	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C56	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C57	CAP CER 2N2 63V 10% PLATE	26383-587R
C58	CAP CER 2N2 63V 10% PLATE	26383-587R
C59	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C60	CAP CER 680P 63V 10% PLATE	26383-583P
C61	CAP CER 680P 63V 10% PLATE	26383-583P
C62	CAP CER 27P 63V 5% PLATE	26343-470U
C63	CAP CER 27P 63V 5% PLATE	26343-470U
C64	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C65	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C66	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C67	CAP PS 2N2 63V 1% RAD	26538-910T
C68	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C69	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C70	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C71	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C72	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C73	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C74	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C75	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C76	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C77	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C78	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C79	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
D1	DI SIL 1N4148 75V JUNC	28336-676J

Circuit Ref	Description		Part Number
Board AD1	- Logarithmic amplifier (Contd.)		
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	DI SIL 1N4148 75V JUNC		28336-676J
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D8	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D9	DI SIL 1N4148 75V JUNC		28336-676J
D10	DI SIL 1N4148 75V JUNC		28336-676J
D11	DI SIL 1N4148 75V JUNC		28336-676J
D12	DI SIL 1N4148 75V JUNC		28336-676J
D13	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D14	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D15	DI SIL 1N4148 75V JUNC		28336-676J
D16	DI SIL 1N4148 75V JUNC		28336-676J
D17	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D18	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D19	DI SIL 1N4148 75V JUNC		28336-676J
D20	DI SIL 1N4148 75V JUNC		28336-676J
D21	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D22	DI ZEN BZX79C5V2 6.2V 5%		28371-481D
D23	DI SIL 1N4148 75V JUNC		28336-676J
D24	DI H/CARR HP5082-2811	!	28349-008U
D25	DI H/CARR HP5082-2811	!	28349-008U
D26	DI SIL 1N4148 75V JUNC		28336-676J
D27	DI SIL 1N4148 75V JUNC		28336-676J
D28	DI SIL 1N4148 75V JUNC		28336-676J
D29	DI SIL 1N4148 75V JUNC		28336-676J
D30	DI H/CARR BAT42 30V FAST	!	28349-013N
D31	DI H/CARR BAT42 30V FAST	!	28349-013N
D32	DI H/CARR BAT42 30V FAST	!	28349-013N
D33	DI H/CARR BAT42 30V FAST	!	28349-013N
D34	DI ZEN BZX79C3V9 3.9V 5%		28371-242D
IC1	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC2	ICA SW SD5000N QUAD DMOS	!	28469-735X
IC3	ICA COMP LM311N DIL8		28461-695U
IC4	ICD FF D 74HCT74 DUAL +EDG TR		28462-630W
IC5	ICD NOR 74LS02 QUAD 2INP		28466-214Y
IC6	ICA SW SD5000N QUAD DMOS	!	28469-735X
IC7	ICA COMP LM311N DIL8		28461-695U
IC8	ICA SW SD5000N QUAD DMOS	!	28469-735X
IC9	ICA COMP LM311N DIL8		28461-695U
IC10	ICD FF D 74HCT74 DUAL +EDG TR		28462-630W

Circuit Ref	Description		Part Number
Board AD1	- Logarithmic amplifier		(Contd.)
IC11	ICA SW SD5000N QUAD DMOS	!	28469-735X
IC12	ICA COMP LM311N DIL8		28461-695U
IC13	ICA COMP LM311N DIL8		28461-695U
IC14	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC15	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC16	ICA MISC SMP11GY S/H AMP H PRF		28461-929K
L1	IND CHOKE 150UH 10% LAQ		23642-562D
L2	IND CHOKE 150UH 10% LAQ		23642-562D
L3	IND CHOKE 150UH 10% LAQ		23642-562D
L4	IND CHOKE 150UH 10% LAQ		23642-562D
R1	RES MF 10K 1/4W 2% 100PPM		24773-297M
R2	RES MF 100R 1/4W 2% 100PPM		24773-249J
R3	RES MF 10R 1/4W 2% 100PPM		24773-225W
R4	RES MF 10R 1/4W 2% 100PPM		24773-225W
R5	RES MF 300R 1/4W 2% 100PPM		24773-260W
R6	RES MF 6K2 1/4W 2% 100PPM		24773-292W
R7	RES MF 470K 1/4W 2% 100PPM		24773-337R
R8	RES MF 470K 1/4W 2% 100PPM		24773-337R
R10	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R11	RES MF 27K 1/4W 2% 100PPM		24773-307K
R12	RES MF 12K 1/4W 2% 100PPM		24773-299R
R13	RES MF 100R 1/4W 2% 100PPM		24773-249J
R14	RES MF 2K7 1/4W 2% 100PPM		24773-283L
R15	RES MF 27K 1/4W 2% 100PPM		24773-307K
R16	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R17	RES MF 5K6 1/4W 2% 100PPM		24773-291S
R18	RES MF 180R 1/4W 2% 100PPM		24773-255V
R20	RES MF 62K 1/4W 2% 100PPM		24773-316Y
R21	RES MF 100R 1/4W 2% 100PPM		24773-249J
R22	RES MF 6K2 1/4W 2% 100PPM		24773-292W
R23	RES MF 10R 1/4W 2% 100PPM		24773-225W
R24	RES MF 560K 1/4W 2% 100PPM		24773-340R
R25	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R26	RES MF 10K 1/4W 2% 100PPM		24773-297M
R27	RES MF 1K0 1/4W 2% 100PPM		24773-273A

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
R28	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R29	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R30	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R33	RES MF 470R 1/4W 2% 100PPM	24773-265M
R34	RES MF 22K 1/4W 2% 100PPM	24773-305R
R35	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R37	RES MF 1K0 1/4W 0.1% 15PPM	24723-306P
R38	RES MF 4R7 1/4W 2% 100PPM	24773-217J
R39	RV CERM 10R LIN .5W 10% HORZ	25711-632U
R40	RES MF 54R2 1/4W .1% 25PPM	24723-411P
R41	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R42	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R43	RES MF 18K 1/4W 2% 100PPM	24773-303M
R44	RES MF 18K 1/4W 2% 100PPM	24773-303M
R48	RES MF 100R 1/4W 2% 100PPM	24773-249J
R49	RES MF 150R 1/4W 2% 100PPM	24773-253F
R50	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R51	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R52	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R53	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R54	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R55	RES MF 10R 1/4W 2% 100PPM	24773-225W
R56	RES MF 820R 1/4W 2% 100PPM	24773-271B
R57	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R58	RES MF 27K 1/4W 2% 100PPM	24773-307K
R59	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R61	RES MF 10R 1/4W 2% 100PPM	24773-225W
R62	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R63	RES MF 180R 1/4W 2% 100PPM	24773-255V
R65	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R66	RES MF 100R 1/4W 2% 100PPM	24773-249J
R67	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R68	RES MF 10R 1/4W 2% 100PPM	24773-225W
R69	RES MF 560K 1/4W 2% 100PPM	24773-340R
R71	RES MF 470R 1/4W 2% 100PPM	24773-265M
R72	RES MF 22K 1/4W 2% 100PPM	24773-305R
R73	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R74	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R75	RES MF 1K0 1/4W 0.1% 15PPM	24723-306P
R76	RES MF 4R7 1/4W 2% 100PPM	24773-217J
R77	RV CERM 10R LIN .5W 10% HORZ	25711-632U
R78	RES MF 54R2 1/4W .1% 25PPM	24723-411P

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
R79	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R80	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R81	RES MF 18K 1/4W 2% 100PPM	24773-303M
R82	RES MF 18K 1/4W 2% 100PPM	24773-303M
R83	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R85	RES MF 100R 1/4W 2% 100PPM	24773-249J
R86	RES MF 150R 1/4W 2% 100PPM	24773-253F
R87	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R88	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R89	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R90	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R91	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R92	RES MF 10R 1/4W 2% 100PPM	24773-225W
R94	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R95	RES MF 820R 1/4W 2% 100PPM	24773-271B
R96	RES MF 27K 1/4W 2% 100PPM	24773-307K
R97	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R98	RES MF 10R 1/4W 2% 100PPM	24773-225W
R99	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R100	RES MF 180R 1/4W 2% 100PPM	24773-255V
R102	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R103	RES MF 100R 1/4W 2% 100PPM	24773-249J
R104	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R105	RES MF 10R 1/4W 2% 100PPM	24773-225W
R106	RES MF 560K 1/4W 2% 100PPM	24773-340R
R108	RES MF 470R 1/4W 2% 100PPM	24773-265M
R109	RES MF 22K 1/4W 2% 100PPM	24773-305R
R110	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R111	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R112	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R113	RES MF 1K0 1/4W 0.1% 15PPM	24723-306P
R114	RES MF 4R7 1/4W 2% 100PPM	24773-217J
R115	RV CERM 10R LIN .5W 10% HORZ	25711-632U
R116	RES MF 54R2 1/4W .1% 25PPM	24723-411P
R117	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R118	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R119	RES MF 18K 1/4W 2% 100PPM	24773-303M
R120	RES MF 18K 1/4W 2% 100PPM	24773-303M
R122	RES MF 100R 1/4W 2% 100PPM	24773-249J
R123	RES MF 150R 1/4W 2% 100PPM	24773-253F
R124	RES MF 3K6 1/4W 2% 100PPM	24773-286G
R125	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R126	RES MF 3K0 1/4W 2% 100PPM	24773-284J

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
R127	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R128	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R129	RES MF 10R 1/4W 2% 100PPM	24773-225W
R130	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R131	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R132	RES MF 820R 1/4W 2% 100PPM	24773-271B
R133	RES MF 11K 1/4W 2% 100PPM	24773-298C
R134	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R135	RES MF 10R 1/4W 2% 100PPM	24773-225W
R136	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R137	RES MF 750R 1/4W 2% 100PPM	24773-270R
R139	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R140	RES MF 100R 1/4W 2% 100PPM	24773-249J
R141	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R142	RES MF 10R 1/4W 2% 100PPM	24773-225W
R143	RES MF 560K 1/4W 2% 100PPM	24773-340R
R144	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R145	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R146	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R147	RES MF 10R 1/4W 2% 100PPM	24773-225W
R148	RES MF 470R 1/4W 2% 100PPM	24773-265M
R149	RES MF 22K 1/4W 2% 100PPM	24773-305R
R150	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R153	RES MF 1K0 1/4W 0.1% 15PPM	24723-306P
R154	RES MF 22R 1/4W 2% 100PPM	24773-233M
R155	RV CERM 20R LIN .5W 10% HORZ	25711-633Y
R156	RES MF 294R 1/4W .1% 25PPM	24723-412X
R157	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R158	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R159	RES MF 18K 1/4W 2% 100PPM	24773-303M
R160	RES MF 18K 1/4W 2% 100PPM	24773-303M
R161	RES CC 47R 1/8W 5%	24331-975Y
R162	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R163	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R164	RV CERM 5K0 LIN .5W 10% HORZ	25711-640F
R165	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R166	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R167	RES MF 100R 1/4W 2% 100PPM	24773-249J
R168	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R169	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R170	RES MF 10K 1/4W 2% 100PPM	24773-297M
R171	RES MF 3K6 1/4W 2% 100PPM	24773-286G

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
R172	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R173	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R174	RES MF 10R 1/4W 2% 100PPM	24773-225W
R175	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R176	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R177	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R178	RES MF 100R 1/4W 2% 100PPM	24773-249J
R179	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R180	RES CC 22R 1/8W 5%	24331-988T
R181	RES MF 910R 1/4W 2% 100PPM	24773-272K
R182	RES MF 200R 1/4W 2% 100PPM	24773-256S
R183	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R184	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R185	RES MF 10R 1/4W 2% 100PPM	24773-225W
R186	RES MF 180R 1/4W 2% 100PPM	24773-255V
R187	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R188	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R189	RES MF 100K 1/4W 2% 100PPM	24773-321L
R190	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R191	RES MF 820R 1/4W 2% 100PPM	24773-271B
R192	RES MF 560R 1/4W 2% 100PPM	24773-267R
R193	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R194	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R195	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R196	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R197	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R198	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R199	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R200	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R201	RES MF 10R 1/4W 2% 100PPM	24773-225W
R202	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R203	RES MF 100R 1/4W 2% 100PPM	24773-249J
R205	RES MF 47R 1/4W 2% 100PPM	24773-241A
R206	RV THERM 470R 10% DISC	25685-402U
R207	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R208	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R209	RES MF 10R 1/4W 2% 100PPM	24773-225W
R210	RES MF 10R 1/4W 2% 100PPM	24773-225W
R211	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R212	RES MF 100R 1/4W 2% 100PPM	24773-249J
R213	RES MF 10K 1/4W 2% 100PPM	24773-297M
R214	RES MF 15K 1/4W 2% 100PPM	24773-301P
R215	RES MF 470R 1/4W 2% 100PPM	24773-265M

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
R216	RES MF 470R 1/4W 2% 100PPM	24773-265M
R217	RES MF 470R 1/4W 2% 100PPM	24773-265M
R218	RES MF 470R 1/4W 2% 100PPM	24773-265M
R219	RES MF 10R 1/4W 2% 100PPM	24773-225W
R220	RES MF 200K 1/4W 2% 100PPM	24773-328D
TR1	TR NSI BC209C 20V 150M - GEN	28452-771P
TR2	TR NJF 2N4857 40V 40R 20MA	28459-051X
TR3	TR NJF 2N4857 40V 40R 20MA	28459-051X
TR4	TR NSI BC209C 20V 150M - GEN	28452-771P
TR5	TR NSI BC209C 20V 150M - GEN	28452-771P
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
TR7	TR PSI BC308B 20V 130M - GEN	28433-455R
TR8	TR PSI MPSL08 12V 700M - SW	28431-767E
TR10	TR PSI BCY71 45V 200M - GEN	28435-235L
TR11	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR12	TR NSI BC209C 20V 150M - GEN	28452-771P
TR13	TR NSI BC209C 20V 150M - GEN	28452-771P
TR14	TR NSI BC209C 20V 150M - GEN	28452-771P
TR15	TR PSI BC308B 20V 130M - GEN	28433-455R
TR17	TR PSI 2N3906 40V 250M - GEN	28434-856A
TR18	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR19	TR NSI BC209C 20V 150M - GEN	28452-771P
TR20	TR NSI BC209C 20V 150M - GEN	28452-771P
TR21	TR NSI BC209C 20V 150M - GEN	28452-771P
TR22	TR PSI BC308B 20V 130M - GEN	28433-455R
TR24	TR PSI 2N3906 40V 250M - GEN	28434-856A
TR25	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR26	TR NSI BC209C 20V 150M - GEN	28452-771P
TR27	TR NSI BC209C 20V 150M - GEN	28452-771P
TR28	TR NSI BC209C 20V 150M - GEN	28452-771P
TR29	TR PSI BC308B 20V 130M - GEN	28433-455R
TR30	TR PSI MPSL08 12V 700M - SW	28431-767E
TR32	TR PSI 2N3906 40V 250M - GEN	28434-856A
TR33	TR PSI 2N3906 40V 250M - GEN	28434-856A
TR34	TR NSI 2N3904 40V 250M - GEN	28454-786H
TR35	TR NSI BC209C 20V 150M - GEN	28452-771P
TR36	TR NSI BFY90 15V 1G - AMP	28452-157R
TR37	TR NSI BFY90 15V 1G - AMP	28452-157R
TR38	TR NSI BFY90 15V 1G - AMP	28452-157R
TR39	TR NSI 2N2369 15V 500M - SW	28452-197H
TR40	TR NSI 2N2369 15V 500M - SW	28452-197H
TR41	TR PSI MPSL08 12V 700M - SW	28431-767E

Circuit Ref	Description	Part Number
Board AD1	- Logarithmic amplifier	(Contd.)
T1	TRANSFORMER	43590-115V
T2	TRANSFORMER	43590-115V
T3	TRANSFORMER	43590-115V
T4	TRANSFORMER	43590-115V
X1	CORE BEAD .079X.158X.197"LG A1	23635-833X
X2	S/C ACC PAD CBE TO TO5	28488-108E
X3	S/C ACC PAD TO18 ETC TO 0.1" GRID	28488-115L

Circuit Ref	Description	Part Number
Board AD2	- Logarithmic amplifier interface	
41.	When ordering, prefix circuit reference with AD2	
	Complete unit	44828-480E
C1	CAP CER 1N0 63V 10% PLATE	26383-585M
C2	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C3	CAP CER 1N5 63V 10% PLATE	26383-593A
C4	CAP CER 2P2 63V 0P5 PLATE	26343-457R
C5	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C6	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C7	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C8	CAP ELEC 470N 50V 20% SUBMIN	26421-104C
C9	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C12	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C13	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C15	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C16	CAP ELEC 100U 35V 20%+ PCB	26421-122J
C17	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AD2	- Logarithmic amplifier interface (Contd.)	
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C46	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C48	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C49	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C50	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C51	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C52	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C53	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C54	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C55	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C56	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C57	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C58	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C59	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C60	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C61	CAP CER 120P 63V 2% PLATE	26343-478S
C62	CAP CER 120P 63V 2% PLATE	26343-478S
C63	CAP CER 120P 63V 2% PLATE	26343-478S
C64	CAP ELEC 3U3 50V 20% SUBMIN	26421-109Z
C65	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICA SW DG211CJ QUAD CMOS !	28461-936E
IC2	ICD MUX 74LS153 DUAL 4INP	28469-711K
IC3	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC4	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC5	ICA AMP LF357N FET I/P LN DIL8	28461-356N
IC6	ICD MONO 74LS122 RETR	28468-310C
IC8	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC9	ICD DECOD 74LS42 4-10	28465-019U
IC10	ICD CTR 74LS192 DEC U/D SPEC	28464-128B

Circuit Ref	Description		Part Number
Board AD2	- Logarithmic amplifier interface (Contd.)		
IC11	ICD CTR 74LS192 DEC U/D SPEC		28464-128B
IC12	ICA ADC AD578 12BIT 6USEC		28461-928B
IC13	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC14	ICM PROM 2732A 4KX8 250NS UV	!	} Note (1)
IC15	ICM PROM 2732A 4KX8 250NS UV	!	
IC16	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC17	ICD LATCH 74LS75 QUAD		28462-408U
IC18	ICD ADDER 74LS283 4BIT FULL		28469-397A
IC19	ICD SH REG 74LS166 8BIT PISO		28467-523T
IC20	ICD SH REG 74LS166 8BIT PISO		28467-523T
IC21	ICD ADDER 74LS283 4BIT FULL		28469-397A
IC22	ICD ADDER 74LS283 4BIT FULL		28469-397A
IC23	ICD AND 74LS08 QUAD 2INP		28466-012L
IC24	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC30	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC31	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC32	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC33	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC34	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC35	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC36	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC37	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC40	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC41	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC42	ICD CTR 74LS161 4BIT BIN PRE		28464-118D
IC43	ICD CTR 74LS193 4BIT BIN U/D		28464-126C
IC44	ICD CTR 74LS193 4BIT BIN U/D		28464-126C
IC45	ICD CTR 74LS193 4BIT BIN U/D		28464-126C
IC46	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC47	ICD MP SUP AM9513A TIM'G CTLR	!	28469-416G
IC50	ICD INV 74LS04 HEX		28469-171L
IC51	ICD INV 74LS04 HEX		28469-171L
IC52	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC53	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC54	ICD OR 74LS32 QUAD 2INP		28466-108U
IC55	ICD OR 74LS32 QUAD 2INP		28466-108U
IC56	ICD AND 74LS08 QUAD 2INP		28466-012L
IC57	ICD NAND 74LS00 QUAD 2INP		28466-345H

Note (1) PROGRAMMED PROM SET IC14,IC15 ! 44533-191P

Circuit Ref	Description	Part Number
Board AD2	- Logarithmic amplifier interface (Contd.)	
R1	RES MG 10M 1/4W 5%	24321-885W
R2	RES MF 470K 1/4W 2% 100PPM	24773-337R
R3	RES MF 7K5 1/4W 2% 100PPM	24773-294T
R4	RES MF 560R 1/4W 2% 100PPM	24773-267R
R5	RES MF 68K 1/4W 2% 100PPM	24773-317N
R10	RES MF 560R 1/4W 2% 100PPM	24773-267R
R11	RES MF 47K 1/4W 2% 100PPM	24773-313H
R12	RES MF 47K 1/4W 2% 100PPM	24773-313H
R13	RES MF 120K 1/4W 2% 100PPM	24773-323F
R14	RES MF 120K 1/4W 2% 100PPM	24773-323F
R15	RES MF 120K 1/4W 2% 100PPM	24773-323F
R16	RES MF 120K 1/4W 2% 100PPM	24773-323F
R17	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R20	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R21	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R22	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R23	RES MF 30K 1/4W 2% 100PPM	24773-308A
R24	RES MF 120K 1/4W 2% 100PPM	24773-323F
R25	RES MF 30K 1/4W 2% 100PPM	24773-308A
R26	RES MF 120K 1/4W 2% 100PPM	24773-323F
R27	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R28	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R29	RES MF 10R 1/4W 2% 100PPM	24773-225W
R30	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R31	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R32	RES MF 9K1 1/4W 2% 100PPM	24773-296X
R33	RES MF 47K 1/4W 2% 100PPM	24773-313H
R34	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R35	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R36	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R37	RES MF 220K 1/4W 2% 100PPM	24773-329T
R39	RES MF 10R 1/4W 2% 100PPM	24773-225W
R40	RES MF 910R 1/4W 2% 100PPM	24773-272K
R41	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R42	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R43	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R44	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R47	RES MF 10K 1/4W 2% 100PPM	24773-297M
R48	RES MF 9K1 1/4W 2% 100PPM	24773-296X
TR1	TR NJF BF245B 30V 6MA	28459-048X
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H

Circuit Ref	Description	Part Number
Board AD2	- Logarithmic amplifier interface (Contd.)	
SK1	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
SK2	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
SK47	S/C ACC SKT DIL40 LOW PROFILE	28488-046J
X1	S/C ACC PAD TO18 TO 0.1" GRID	28488-115L

Circuit Ref	Description	Part Number
Board AD3	- Microprocessor	
42.	When ordering, prefix circuit reference with AD3	
	Complete unit	44828-481U
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description		Part Number
Board AD3	- Microprocessor		(Contd.)
C41	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C46	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C48	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C49	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C60	CAP CER 4N7 63V 10% PLATE		26383-591B
C61	CAP CER 4N7 63V 10% PLATE		26383-591B
C63	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
D1	DI H/CARR BAT29 5V	!	28349-014L
D2	DI H/CARR BAT29 5V	!	28349-014L
IC1	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC2	ICD DEC/DMX 74LS138 3-8		28465-027F
IC3	ICD DEC/DMX 74LS138 3-8		28465-027F
IC4	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC5	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC7	ICD DEC/DMX 74LS138 3-8		28465-027F
IC8	ICD CTR 74LS90 4BIT DEC 2,5,10		28464-014S
IC9	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC10	ICD CTR 74LS93 4BIT BIN 2,8,16		28464-117W
IC11	ICD MP SUP 8251A USART DIL28	!	28469-189K
IC12	ICD MP SUP 8259A PROG INT CTLR	!	28467-012X
IC13	ICD MP SUP 8259A PROG INT CTLR	!	28467-012X
IC14	ICD BUFF 74LS245 OCT TXRX		28469-188B
IC15	ICD DEC/DMX 74LS138 3-8		28465-027F
IC16	ICD CTR 74197 50MHZ BINARY/BCD		28464-103H
IC17	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC18	ICD DEC/DMX 74LS138 3-8		28465-027F
IC19	ICD DEC/DMX 74LS155 DUAL 2-4		28465-026J
IC20	ICD RAM HM6116P-4 2KX8 200NS	!	28469-307N
IC21	ICD RAM HM6116P-4 2KX8 200NS	!	28469-307N
IC22	ICD PROM X2816A 2KX8 EE DIL24	!	28471-022V
IC23	ICD PROM X2816A 2KX8 EE DIL24	!	28471-022V
IC24	ICD MONO 74LS221 DUAL		28468-404D
IC28	ICD LATCH 74LS75 QUAD		28462-408U
IC29	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC30	ICD MP SUP AM9513A TIM'G CTLR	!	28469-416G
IC31	ICD FF D 74S74 DUAL +EDG TR		28462-607K
IC32	ICD MP P8085A 8BIT NMOS	!	28469-396K
IC33	ICD LATCH 74LS373 OCT 3ST		28462-410E
IC34	ICD LATCH 74LS373 OCT 3ST		28462-410E
IC35	ICD BUFF 74LS245 OCT TXRX		28469-188B

Circuit Ref	Description		Part Number
Board AD3	- Microprocessor		(Contd.)
IC36	ICD DEC/DMX 74LS138 3-8		28465-027F
IC37	ICD DEC/DMX 74LS138 3-8		28465-027F
IC38	ICD DEC/DMX 74LS138 3-8		28465-027F
IC39	ICD PROM 27128 16KX8 250NS UV	!	
IC40	ICD PROM 27128 16KX8 250NS UV	!	Note (1)
IC41	ICD PROM 27128 16KX8 250NS UV	!	
IC42	ICD PROM 2764 8KX8 250NS UV	!	
IC46	ICD OR 74LS32 QUAD 2INP		28466-108U
IC47	ICD INV 74LS04 HEX		28469-171L
IC48	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC49	ICD AND 74LS08 QUAD 2INP		28466-012L
R1	RES MF 200R 1/4W 2% 100PPM		24773-256S
R2	RES MF 1K5 1/4W 2% 100PPM		24773-277U
R3	RES MF 5K1 1/4W 2% 100PPM		24773-290V
R4	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R5	RES MF 15K 1/4W 2% 100PPM		24773-301P
R6	RES MF 33K 1/4W 2% 100PPM		24773-309Z
R7	RES MF 2K4 1/4W 2% 100PPM		24773-282N
R9	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R10	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R11	RES MF 22K 1/4W 2% 100PPM		24773-305R
R12	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R13	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R14	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R15	RES MF 10K 1/4W 2% 100PPM		24773-297M
R16	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R18	RES MF 15K 1/4W 2% 100PPM		24773-301P
R20	RES MF 1K0 1/4W 2% 100PPM		24773-273A
SKAA	CON JUMP FEM 2 1 ROW		23435-990X
SKAB	CON JUMP FEM 2 1 ROW		23435-990X
SKAC	CON JUMP FEM 2 1 ROW		23435-990X
SKAD	CON JUMP FEM 2 1 ROW		23435-990X
SKFT	CON JUMP FEM 2 1 ROW		23435-990X
SKPS	CON JUMP FEM 2 1 ROW		23435-990X
TR1	TR PSI MPSL08 12V 700M - SW		28431-767E
TR2	TR NSI 2N2369 15V 500M - SW		28452-197H
TR3	TR NSI 2N2369 15V 500M - SW		28452-197H

Note (1) PROGRAMMED PROM SET ! 44533-201R

Circuit Ref	Description	Part Number
Board AD3	- Microprocessor	(Contd.)
X9	S/C ACC PAD TO18 ETC TO 0.1" GRID	28488-715L
X10	S/C ACC PAD TO18 ETC TO 0.1" GRID	28488-115L
X11	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X12	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X13	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X20	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
X21	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
X22	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X23	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X30	S/C ACC SKT DIL40 LOW PROFILE	28488-046J
X32	S/C ACC SKT DIL40 LOW PROFILE	28488-046J
X39	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X40	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X41	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
X42	S/C ACC SKT DIL28 LOW PROFILE	28488-045L

Circuit Ref	Description		Part Number
Board AD4	- 10 MHz calibrator		
43.	When ordering, prefix circuit reference with AD4		
	Complete unit		44828-482Y
C1	CAP ELEC 1U0 50V 20% SUBMIN		26421-106B
C2	CAP CER 1N5 63V 10% PLATE		26383-593A
C3	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C4	CAP CER 1N5 63V 10% PLATE		26383-593A
C5	CAP CER 10N 25V 20% DISC		26383-006C
C8	CAP CER 4N7 63V 10% PLATE		26383-591B
C9	CAP CER 4N7 63V 10% PLATE		26383-591B
C10	CAP CER 10N 25V 20% DISC		26383-006C
C11	CAP CER 1N5 63V 10% PLATE		26383-593A
C12	CAP CER 22N 18V 20% DISC		26383-007R
C13	CAP CER 10N 25V 20% DISC		26383-006C
C14	CAP CER 330P 63V 2% PLATE		26343-483D
C15	CAP CER 22N 18V 20% DISC		26383-007R
C16	CAP CER 22N 18V 20% DISC		26383-007R
C17	CAP CER 22N 18V 20% DISC		26383-007R
C18	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C19	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C20	CAP CER 10N 25V 20% DISC		26383-006C
C21	CAP CER 10N 25V 20% DISC		26383-006C
C22	CAP CER 10N 25V 20% DISC		26383-006C
C23	CAP CER 10P 63V 0P5 PLATE		26343-465H
C24	CAP ELEC 1U0 50V 20% SUBMIN		26421-106B
D1	DI V/CAP BB405B 3V 11.5PF		28381-101V
D2	DI H/CARR HP5082-2080 FOR SETS	!	28349-012Y
D3	DI H/CARR HP5082-2080 FOR SETS	!	28349-012Y
D4	DI SIL BA482 35V JUNC		28335-675R
D5	DI SIL BA482 35V JUNC		28335-675R
D6	DI SIL BA482 35V JUNC		28335-675R
D7	DI ZEN BZX79C5V1 5.1V 5%		28371-401U
D8	DI V/CAP BB405B 3V 11.5PF		28381-101V
D9	DI V/CAP BB405B 3V 11.5PF		28381-101V
IC1	ICD RX 75107A DUAL LINE TP		28469-198Y
IC2	ICD NAND 74LS132 QUAD 2INP SCH		28469-205N
IC3	ICA AMP TL072CP DUAL FET I/P		28461-348Z
L1	IND CHOKE 100UH 10% LAQ		23642-561W
L2	IND CHOKE 1.0UH 10% LAQ		23642-549L
L3	IND CHOKE .68UH 10% LAQ		23642-548N

Circuit Ref	Description	Part Number
Board AD4	- 10 MHz calibrator	(Contd.)
R2	RV CERM 500K LIN 0.5W 10%	25748-568D
R3	RES MF 47K 1/4W 2% 100PPM	24773-313H
R4	RES MF 47K 1/4W 2% 100PPM	24773-313H
R5	RES MF 330R 1/4W 2% 100PPM	24773-261D
R6	RES MF 470R 1/4W 2% 100PPM	24773-265M
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R10	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R12	RES MF 10K 1/4W 2% 100PPM	24773-297M
R13	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R14	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R15	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R16	RES MF 100R 1/4W 2% 100PPM	24773-249J
R17	RES MF 51R1 1/4W 1% 25PPM	24763-352Y
R18	RES MF 4R7 1/4W 2% 100PPM	24773-217J
R19	RES MF 4R7 1/4W 2% 100PPM	24773-217J
R20	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R21	RES MF 2K0 1/4W 1% 25PPM	24763-353N
R22	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R23	RES MF 51R1 1/4W 1% 25PPM	24763-352Y
R24	RES MF 1K5 1/4W 1% 25PPM	24763-354L
R25	RV CERM 500R LIN .5W 10% HORZ	25711-637F
R26	RES MF 100K 1/4W 2% 100PPM	24773-321L
R27	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R28	RES MF 11K 1/4W 2% 100PPM	24773-298C
R29	RES MF 13K 1/4W 2% 100PPM	24773-300T
R30	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R31	RES MF 5K1 1/4W 2% 100PPM	24773-290V
R32	RES MF 750R 1/4W 2% 100PPM	24773-270R
R33	RES CC 47R 1/8W 5%	24331-975Y
R34	RES CC 47R 1/8W 5%	24331-975Y
R35	RES CC 47R 1/8W 5%	24331-975Y
R36	RES CC 47R 1/8W 5%	24331-975Y
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NSI BFY90 15V 1G - AMP	28452-157R
TR3	TR NSI BFY90 15V 1G - AMP	28452-157R
TR4	TR NSI BFY90 15V 1G - AMP	28452-157R
X1	OSC XTAL 10MHZ O/T PLUG-IN	28313-862L
X2	S/C ACC PAD TO18 ETC TO 0.1" GRID	28488-115L

Circuit Ref	Description	Part Number
Unit AE0	- Tracking generator tray	
44.	When ordering, prefix circuit reference with AE0	
	Complete unit	44990-452G
C1	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C11	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 22P 300V 10% L/T SOL	26333-226Z
C18	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C35	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C40	CAP FILTERCON 3N0/5N0 350V	26397-208S
C41	CAP FILTERCON 3N0/5N0 350V	26397-208S

Circuit Ref	Description	Part Number
Unit AE0	- Tracking generator tray	(Contd.)
C42	CAP FILTERCON 3N0/5N0 350V	26397-208S
C43	CAP FILTERCON 3N0/5N0 350V	26397-208S
C44	CAP FILTERCON 3N0/5N0 350V	26397-208S
C45	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C46	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C47	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C48	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C50	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C51	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C52	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C53	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C54	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C55	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C56	CAP CER 10P 300V 1P0 L/T SOL	26333-228E
C60	CAP CER 4P7 63V 0P25 P100 DIS	26343-485P
C61	CAP CER 4P7 63V 0P25 P100 DIS	26343-485P
L1	INDUCTOR CHOKE GEN	44190-036B
L2	INDUCTOR CHOKE GEN	44190-036B
L3	INDUCTOR CHOKE GEN	44190-036B
L4	INDUCTOR CHOKE GEN	44190-036B
L5	INDUCTOR CHOKE GEN	44190-036B
L6	INDUCTOR CHOKE GEN	44190-036B
L7	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR	34900-918Y
L9	INDUCTOR CHOKE GEN	44190-036B
L10	INDUCTOR CHOKE GEN	44190-036B
L11	INDUCTOR CHOKE GEN	44190-036B
L12	INDUCTOR CHOKE GEN	44190-036B
L13	INDUCTOR CHOKE GEN	44190-036B
L14	INDUCTOR CHOKE GEN	44190-036B
L15	INDUCTOR CHOKE GEN	44190-036B
L16	INDUCTOR CHOKE GEN	44190-036B
L17	INDUCTOR CHOKE GEN	44190-036B
L18	INDUCTOR CHOKE GEN	44190-036B
L19	INDUCTOR CHOKE GEN	44190-036B
L20	INDUCTOR CHOKE GEN	44190-036B
L21	INDUCTOR CHOKE GEN	44190-036B
L22	INDUCTOR CHOKE GEN	44190-036B
MP1	EYELET COAX/BULKHEAD	35902-029E
MP2	CON PART D SCREWLOCK FEM	23435-981V
MP4	CON PART MIN SKT 22-26AWG REEL	23435-178U
MP5	CON PART MIN POLARIZING KEY	23435-190G

Circuit Ref	Description	Part Number
Unit AE0	- Tracking generator tray	(Contd.)
PLB	CON RF SMC MALE 50 BKHD UT85	23444-368L
PLC	CON RF SMC MALE 50 BKHD UT85	23444-368L
PLD	CON RF SMB MALE 50 BKHD SOLDER	23444-331H
PLAA	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
PLAB	CON RF SMC MALE 50 BKHD S/TAG	23444-382T
R1	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R2	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R3	RES MF 270R 1/4W 2% 100PPM	24773-259T
X1	CABLE RIBBON 16-WAY	43129-929T
X4	CABLE MIN COAX	43129-973B
X6	TRACKING GEN TO FRONT PANEL	43129-919J
	CABLE ASSY. (AE2-AA9)	43129-920N
	CABLE ASSY. (AE4-AA7)	43129-922J

Circuit Ref	Description		Part Number
Board AE1	- 47.4 MHz crystal oscillator		
45.	When ordering, prefix circuit reference with AE1		
	Complete unit		44828-485J
C1	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C2	CAP ELEC 470U 6V 20%+ PCB		26421-126S
C3	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C4	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C5	CAP CER 47N 25V 20% DISC		26383-017U
C6	CAP CER 4N7 63V 10% PLATE		26383-591B
C7	CAP CER 47P 63V 5% PLATE		26343-473L
C8	CAP CER 68P 63V 2% PLATE		26343-475F
C9	CAP CER 100P 63V 2% PLATE		26343-477V
C10	CAP CER 15P 63V 5% PLATE		26343-467U
C11	CAP CER 4N7 63V 10% PLATE		26383-591B
C12	CAP CER 4N7 63V 10% PLATE		26383-591B
C13	CAP CER 4N7 63V 10% PLATE		26383-591B
C14	CAP CER 4N7 63V 10% PLATE		26383-591B
C15	CAP CER 1N0 63V 10% PLATE		26383-585M
C16	CAP CER 270P 63V 2% PLATE		26343-482W
C17	CAP CER 1N0 63V 10% PLATE		26383-585M
C18	CAP TANT 4U7 35V 20% BEAD		26486-219P
C19	CAP TANT 4U7 35V 20% BEAD		26486-219P
C20	CAP CER 47N 25V 20% DISC		26383-017U
C21	CAP CER 47N 25V 20% DISC		26383-017U
C22	CAP CER 4N7 63V 10% PLATE		26383-591B
C23	CAP CER 4N7 63V 10% PLATE		26383-591B
C25	CAP CER 470P 63V 10% PLATE		26383-582T
C26	CAP CER 100P 63V 2% PLATE		26343-477V
C27	CAP CER 4N7 63V 10% PLATE		26383-591B
C28	CAP CER 4N7 63V 10% PLATE		26383-591B
C29	CAP CER 4N7 63V 10% PLATE		26383-591B
C30	CAP PETP 220N 63V 10% RAD MIN		26582-430L
C31	CAP CER 4N7 63V 10% PLATE		26383-591B
C33	CAP CER 4N7 63V 10% PLATE		26383-591B
C34	CAP CER 1N0 63V 10% PLATE		26383-585M
C35	CAP CER 1N0 63V 10% PLATE		26383-585M
D1	DI V/CAP BB405B 3V 11.5PF		28381-101V
D2	DI H/CARR BAT29 5V	!	28349-014L
D3	DI H/CARR BAT29 5V	!	28349-014L
D4	DI H/CARR BAT29 5V	!	28349-014L

Circuit Ref	Description	Part Number
Board AE1	- 47.4 MHz crystal oscillator	(Contd.)
D5	DI H/CARR BAT29 5V !	28349-014L
D6	DI STEP 5082-0180	28383-998P
D7	DI H/CARR BAT29 5V	28349-014L
D8	DI SIL 1N4148 75V JUNC	28336-676J
D9	DI PIN 5082-3379 50V	28383-997T
D10	DI PIN 5082-3379 50V	28383-997T
D11	DI PIN 5082-3379 50V	28383-997T
IC1	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC2	ICA AMP UA741CN GP DIL8	28461-304T
L1	INDUCTOR ASSY.	44290-871S
L2	IND CHOKE 1.0UH 10% LAQ	23642-549L
L3	IND CHOKE .1UH 20% LAQ	23642-543Z
L4	IND CHOKE .1UH 20% LAQ	23642-543Z
L5	IND CHOKE .1UH 20% LAQ	23642-543Z
R1	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R3	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R4	RES MF 100R 1/4W 2% 100PPM	24773-249J
R5	RES MF 82R 1/4W 2% 100PPM	24773-247N
R6	RES MF 100R 1/4W 2% 100PPM	24773-249J
R7	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R8	RES MF 100R 1/4W 2% 100PPM	24773-249J
R9	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R10	RES MF 470R 1/4W 2% 100PPM	24773-265M
R11	RES MF 56R 1/4W 2% 100PPM	24773-243H
R12	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R13	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R14	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R15	RES MF 330R 1/4W 2% 100PPM	24773-261D
R16	RES MF 62R 1/4W 2% 100PPM	24773-244E
R17	RV CERM 5KO LIN .5W 10% HORZ	25711-640F
R20	RES MF 47K 1/4W 2% 100PPM	24773-313H
R21	RES MF 47K 1/4W 2% 100PPM	24773-313H
R22	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R23	RES MF 200R 1/4W 2% 100PPM	24773-256S
R24	RES MF 200R 1/4W 2% 100PPM	24773-256S
R25	RES MF 10R 1/4W 2% 100PPM	24773-225W
R26	RES MF 1KO 1/4W 2% 100PPM	24773-273A

Circuit Ref	Description	Part Number
Unit AE1	- 47.4 MHz crystal oscillator	(Contd.)
R27	RES MF 27R 1/4W 2% 100PPM	24773-235R
R28	RES MF 220R 1/4W 2% 100PPM	24773-257W
R29	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R30	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R31	RES MF 2K0 1/4W 2% 100PPM	24773-280U
R34	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R35	RES MF 68K 1/4W 2% 100PPM	24773-317N
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES MF 10K 1/4W 2% 100PPM	24773-297M
R40	RES MF 120R 1/4W 2% 100PPM	24773-251L
R41	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R42	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R43	RES MF 10K 1/4W 2% 100PPM	24773-297M
R44	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R45	RES MF 24K 1/4W 2% 100PPM	24773-306B
R48	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R49	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R50	RES MF 51R 1/4W 2% 100PPM	24773-242Z
R51	RES MF 10K 1/4W 2% 100PPM	24773-297M
R52	RES MF 4R7 1/4W 2% 100PPM	24773-217J
TR1	TR NSI BFY90 15V 1G - AMP	28452-157R
TR2	TR NSI BFY90 15V 1G - AMP	28452-157R
TR3	TR PSI 2N4959 30V - LN AMP	28433-836K
TR4	TR NSI 2N2369 15V 500M - SW	28452-197H
TR5	TR NSI BFY90 15V 1G - AMP	28452-157R
T1	TRANSFORMER ASSY.	43590-134Z
XL1	XTAL 47.401M S-	28312-085L
	S/C ACC PAD TO18 TO 0.1" GRID	28488-115L

Circuit Ref	Description	Part Number
Board AE2	- Buffer	
46.	When ordering, prefix circuit reference with AE2	
	Complete unit	44828-486F
C1	CAP CER 2P7 63V 0P5 PLATE	26343-458B
C2	CAP CER 56P 63V 2% PLATE	26343-474J
C3	CAP CER 2P7 63V 0P5 PLATE	26343-458B
C4	CAP CER 56P 63V 2% PLATE	26343-474J
C5	CAP CER 39P 63V 5% PLATE	26343-472N
C6	CAP CER 1N0 63V 10% PLATE	26383-585M
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
L2	INDUCTOR 30NH	34900-916E
L3	INDUCTOR 30NH	34900-916E
R1	RES CC 47R 1/8W 5%	24331-975Y
R2	RES CC 4K7 1/8W 5%	24331-970A
R3	RES CC 3K3 1/8W 5%	24331-948G
R4	RES CC 390R 1/8W 5%	24331-963C
R5	RES CC 68R 1/8W 5%	24331-979F
R6	RES CC 4K7 1/8W 5%	24331-970A
R7	RES CC 3K6 1/8W 5%	24331-938E
R8	RES CC 220R 1/8W 5%	24331-976N
R9	RES CC 68R 1/8W 5%	24331-979F
R10	RES CC 120R 1/8W 5%	24331-998K
R11	RES MF 10R 1/4W 2% 100PPM	24773-225W
R12	RES MF 100R 1/4W 2% 100PPM	24773-249J
R13	RES CC 62R0 1/8W 5%	24331-962M
R14	RES CC 220R 1/8W 5%	24331-976N
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR90 15V 5G - AMP	28452-167U

Circuit Ref	Description	Part Number
Unit AE3	- 502.6 MHz TG i.f. filter assembly	
47.	When ordering, prefix circuit reference with AE3	
	Complete unit	44990-442E

Circuit Ref	Description		Part Number
Board AE3a	- Narrow band mixer/buffer		
48.	When ordering, prefix circuit reference with AE3a		
	Complete unit		44828-487G
C1	CAP CER 2P7 63V 0P5 PLATE		26343-458B
C2	CAP CER 56P 63V 2% PLATE		26343-474J
C3	CAP CER 2P7 63V 0P5 PLATE		26343-458B
C4	CAP CER 56P 63V 2% PLATE		26343-474J
C5	CAP CER 3P3 63V 0P5 PLATE		26343-459K
C6	CAP CER 1N0 63V 10% PLATE		26383-585M
C7	CAP CER 39P 63V 5% PLATE		26343-472N
C8	CAP CER 5P6 63V 0P5 PLATE		26343-462K
C9	CAP CER 4N7 63V 10% PLATE		26383-591B
C10	CAP CER 1N0 63V 10% PLATE		26383-585M
C11	CAP CER 3P3 63V 0P5 PLATE		26343-459K
C12	CAP CER 5P6 63V 0P5 PLATE		26343-462K
C13	CAP CER 1N0 63V 10% PLATE		26383-585M
C14	CAP CER 1N0 63V 10% PLATE		26383-585M
L2	INDUCTOR 30NH		34900-916E
L3	INDUCTOR 20NH UHF		34900-915H
L4	IND CHOKE 1.0UH 10% LAQ		23642-549L
L5	INDUCTOR 30NH		34900-916E
R1	RES CC 47R 1/8W 5%		24331-975Y
R2	RES CC 4K7 1/8W 5%		24331-970A
R3	RES CC 3K6 1/8W 5%		24331-938E
R4	RES CC 390R 1/8W 5%		24331-963C
R5	RES CC 47R 1/8W 5%		24331-975Y
R6	RES CC 4K7 1/8W 5%		24331-970A
R7	RES CC 4K3 1/8W 5%		24331-956T
R8	RES CC 220R 1/8W 5%		24331-976N
R9	RES CC 150R 1/8W 5%		24331-990D
R10	RES MF 9K1 1/4W 2% 100PPM		24773-296X
R11	RES MF 6K2 1/4W 2% 100PPM		24773-292W
R12	RES CC 2K2 1/8W 5%		24331-983G
R13	RES CC 2K2 1/8W 5%		24331-983G
R14	RES MF 270R 1/4W 2% 100PPM		24773-259T
R15	RES MF 10R 1/4W 2% 100PPM		24773-225W
R16	RES MF 100R 1/4W 2% 100PPM		24773-249J
TR1	TR NSI BFR90 15V 5G - AMP		28452-167U
TR2	TR NSI BFR96 15V 5G - AMP		28452-171Y
TR3	TR NMF SD306DE 20V 500M DG	!	28459-043S

Circuit Ref	Description	Part Number
Unit AE4	- TG buffer	
49.	When ordering, prefix circuit reference with AE4	
	Complete unit	44828-488V
C1	CAP CER 2P7 63V 0P5 PLATE	26343-458B
C2	CAP CER 56P 63V 2% PLATE	26343-474J
C3	CAP CER 2P7 63V 0P5 PLATE	26343-458B
C4	CAP CER 56P 63V 2% PLATE	26343-474J
C5	CAP CER 39P 63V 5% PLATE	26343-472N
C6	CAP CER 1N0 63V 10% PLATE	26383-585M
C7	CAP CER 1N0 63V 10% PLATE	26383-585M
L2	INDUCTOR 30NH	34900-916E
L3	INDUCTOR 30NH	34900-916E
R1	RES CC 47R 1/8W 5%	24331-975Y
R2	RES CC 4K7 1/8W 5%	24331-970A
R3	RES CC 3K3 1/8W 5%	24331-948G
R4	RES CC 390R 1/8W 5%	24331-963C
R5	RES CC 68R 1/8W 5%	24331-979F
R6	RES CC 4K7 1/8W 5%	24331-970A
R7	RES CC 3K6 1/8W 5%	24331-938E
R8	RES CC 220R 1/8W 5%	24331-976N
R9	RES CC 68R 1/8W 5%	24331-979F
R10	RES CC 120R 1/8W 5%	24331-998K
R11	RES MF 10R 1/4W 2% 100PPM	24773-225W
R12	RES MF 100R 1/4W 2% 100PPM	24773-249J
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR90 15V 5G - AMP	28452-167U

Circuit Ref	Description	Part Number
Unit AE5	- TG output filter	
50.	When ordering, prefix circuit reference with AE5	
	Complete unit	44990-435K
C1	CAP VAR AIR 9PO 1PO TRIM	26814-502R
C2	CAP CER 12P 63V 5% PLATE	26343-466E
C3	CAP CER 12P 63V 5% PLATE	26343-466E
C4	CAP VAR AIR 9PO 1PO TRIM	26814-502R
L1	INDUCTOR	34900-920U
L2	INDUCTOR	34900-921Y
L3	INDUCTOR	34900-921Y
L4	INDUCTOR	34900-921Y
L5	INDUCTOR	34900-921Y
MP1	CHASSIS FILTER	35903-718D
X1	INS L/T 7/16"LG .0935"HOLE	23211-212W
X2	INS L/T 7/16"LG .0935"HOLE	23211-212W
X3	INS L/T 7/16"LG .0935"HOLE	23211-212W
X4	INS L/T 7/16"LG .0935"HOLE	23211-212W

Circuit Ref	Description	Part Number
Board AE5a	- Wideband mixer/buffer	
51.	When ordering, prefix circuit reference with AE5a	
	Complete unit	44828-489S
C1	CAP CER 1P8 63V .5PF PLATE	26343-456C
C2	CAP CER 56P 63V 2% PLATE	26343-474J
C3	CAP CER 1P8 63V .5PF PLATE	26343-456C
C4	CAP CER 56P 63V 2% PLATE	26343-474J
C6	CAP CER 2P7 63V .5PF PLATE	26343-458B
C7	CAP CER 1NO 63V 10% PLATE	26383-585M
C8	CAP CER 56P 63V 2% PLATE	26343-474J
C9	CAP CER 39P 63V 5% PLATE	26343-472N
C10	CAP CER 4P7 63V .5PF PLATE	26343-461B
C11	CAP CER 2P7 63V .5PF PLATE	26343-458B
C12	CAP CER 3P9 63V .5PF PLATE	26343-460R
C13	CAP CER 56P 63V 2% PLATE	26343-474J
C14	CAP CER 39P 63V 5% PLATE	26343-472N
C15	CAP CER 1NO 63V 10% PLATE	26383-585M
C16	CAP CER 1NO 63V 10% PLATE	26383-585M
C17	CAP CER 1NO 63V 10% PLATE	26383-585M
C18	CAP CER 1NO 63V 10% PLATE	26383-585M
L2	INDUCTOR 30NH	34900-916E
L3	COIL ASSEMBLY CHOKE UHF	44290-921B
L5	COIL ASSEMBLY CHOKE UHF	44290-921B
L7	INDUCTOR CHOKE GEN	44190-036B
L8	INDUCTOR CHOKE GEN	44190-036B
R1	RES CC 47R 1/8W 5%	24331-975Y
R2	RES CC 4K7 1/8W 5%	24331-970A
R3	RES CC 3K6 1/8W 5%	24331-938E
R4	RES CC 390R 1/8W 5%	24331-963C
R5	RES CC 68R 1/8W 5%	24331-979F
R6	RES CC 4K7 1/8W 5%	24331-970A
R7	RES CC 4K3 1/8W 5%	24331-956T
R8	RES CC 220R 1/8W 5%	24331-976N
R10	RES MF 11K 1/4W 2% 100PPM	24773-298C
R11	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R12	RES CC 1K5 1/8W 5%	24331-959M
R13	RES MO 330R 1/2W 2% 250PPM	24573-061U
R14	RES MO 330R 1/2W 2% 250PPM	24573-061U

Circuit Ref	Description	Part Number
Board AE5a	- Wideband mixer/buffer	(Contd.)
R15	RES CC 220R 1/8W 5%	24331-976N
R19	RES CC 47R 1/8W 5%	24331-975Y
R20	RES CC 4K7 1/8W 5%	24331-970A
R21	RES CC 3K6 1/8W 5%	24331-938E
R22	RES CC 200R 1/8W 5%	24331-999A
R23	RES CC 62R0 1/8W 5%	24331-962M
R24	RES CC 10R 1/8W 5%	24331-974U
R25	RES CC 10R 1/8W 5%	24331-974U
TR1	TR NSI BFR90 15V 5G - AMP	28452-167U
TR2	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R
TR4	TR NSI BFR96 15V 5G - AMP	28452-171Y
TR5	TR NSI BFR90 15V 5G - AMP	28452-167U
X1	MOD RF SRA-2H DBL BAL MXR H/L	28531-006U

Circuit Ref	Description	Part Number
Board AE6	- Amplifier/leveller	
52.	When ordering, prefix circuit reference with AE6	
	Complete unit	44828-490G
C1	CAP PETP 22N 63V 10% RAD MIN	26582-431J
C2	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C4	CAP CER 12P 63V 5% PLATE	26343-466E
C5	CAP CER 10P 63V .5PF PLATE	26343-465H
C8	CAP VAR CER 13P 3P5 TRIM	26847-112K
C10	CAP CER 18P 63V 5% PLATE	26343-468Y
C11	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C13	CAP PETP 22N 63V 10% RAD MIN	26582-431J
C15	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C16	CAP CER 22N 18V 20% DISC	26383-007R
C17	CAP ELEC 1UO 50V 20% SUBMIN	26421-106B
C18	CAP ELEC 1UO 50V 20% SUBMIN	26421-106B
C19	CAP ELEC 470U 6V 20%+ PCB	26421-126S
C24	CAP CER 4N7 63V 10% PLATE	26383-591B
C25	CAP ELEC 470U 6V 20%+ PCB	26421-126S
C26	CAP CER 220N 50V 20% CHIP	26386-761E
C28	CAP CER 220N 50V 20% CHIP	26386-761E
C30	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C33	CAP ELEC 1UO 50V 20% SUBMIN	26421-106B
C35	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C36	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C37	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C38	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C44	CAP ELEC 1UO 50V 20% SUBMIN	26421-106B
C45	CAP CER 47P 63V 5% PLATE	26343-473L
C46	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C47	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C48	CAP PETP 22N 63V 10% RAD MIN	26582-431J
C49	CAP CER 1NO 63V 10% PLATE	26383-585M
C50	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C52	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C53	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C54	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C55	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C60	CAP CER 10N 25V 20% DISC	26383-006C
C61	CAP CER 10N 25V 20% DISC	26383-006C
C62	CAP CER 10N 25V 20% DISC	26383-006C

Circuit Ref	Description		Part Number
Board AE6	- Amplifier/leveller		(Contd.)
C63	CAP CER 10N 25V 20% DISC		26383-006C
C64	CAP CER 10N 25V 20% DISC		26383-006C
C65	CAP CER 10N 25V 20% DISC		26383-006C
C66	CAP CER 10N 25V 20% DISC		26383-006C
C67	CAP CER 22N 18V 20% DISC		26383-007R
C68	CAP CER 22N 18V 20% DISC		26383-007R
C69	CAP CER 10N 25V 20% DISC		26383-006C
C70	CAP CER 10N 25V 20% DISC		26383-006C
C71	CAP PETP 470N 63V 10% RAD MIN		26582-427L
C72	CAP CER 220P 400V 20% DISC		26383-134W
D1	DI SIL BA482 35V JUNC		28335-675R
D3	DI SIL BA482 35V JUNC		28335-675R
D5	DI PIN 5082-3379 50V		28383-997T
D6	DI PIN 5082-3379 50V		28383-997T
D7	DI PIN 5082-3379 50V		28383-997T
D8	DI PIN 5082-3379 50V		28383-997T
D9	DI H/CARR HP5082-2811	!	28349-008U
D10	DI H/CARR HP5082-2826	!	28349-011U
D11	DI H/CARR HP5082-2826	!	28349-011U
D12	DI SIL 1N4148 75V JUNC		28336-676J
D13	DI SIL BA482 35V JUNC		28335-675R
D15	DI SIL BA482 35V JUNC		28335-675R
D17	DI PIN 5082-3379 50V		28383-997T
D18	DI PIN 5082-3379 50V		28383-997T
D19	DI PIN 5082-3379 50V		28383-997T
D20	DI PIN 5082-3379 50V		28383-997T
D21	DI SIL 1N4148 75V JUNC		28336-676J
D22	DI SIL 1N4148 75V JUNC		28336-676J
D23	DI SIL 1N4148 75V JUNC		28336-676J
D24	DI ZEN BZX79C3V9 3.9V 5%		28371-242D
D25	DI SIL 1N4148 75V JUNC		28336-676J
D26	DI ZEN BZX79C3V9 3.9V 5%		28371-242D
D27	DI SIL 1N4148 75V JUNC		28336-676J
D31	DI ZEN BZX79C5V6 5.6V 5%		28371-417X
D32	DI ZEN BZX79C4V7 4.7V 5%		28371-371F
D33	DI ZEN BZX79C6V2 6.2V 5%		28371-481D
IC1	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC2	ICA SW 4066 QUAD BI	!	28469-383S
IC3	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC4	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC5	ICA AMP LM348N QUAD GP DIL14		28461-321E
IC6	ICA AMP TL072CP DUAL FET I/P		28461-348Z

Circuit Ref	Description	Part Number
Board AE6	- Amplifier/leveller (Contd.)	
IC7	ICA COMP LM339N QUAD	28461-693H
IC9	ICA AMP TL074CN QUAD FET I/P	28461-349H
IC10	ICD MONO 74LS123 DUAL RETR	28468-309B
IC11	ICD NOR 4001 QUAD 2INP BI !	28466-207Z
IC12	ICD NAND 74LS132 QUAD 2INP SCH	28469-205N
IC13	ICD NOR 4001 QUAD 2INP BI !	28466-207Z
L1	IND	34900-914Z
L2	IND CHOKE 470UH 10% LAQ	23642-565X
R1	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R2	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R4	RES MF 62R 1/4W 2% 100PPM	24773-244E
R5	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES CC 56R 1/8W 5%	24331-944N
R7	RES MF 39R 1/4W 2% 100PPM	24773-239Z
R8	RES CC 68R 1/8W 5%	24331-979F
R9	RES CC 12R 1/8W 5%	24331-986W
R10	RES CC 24R 1/8W 5%	24331-937H
R11	RES MF 10R 1/4W 2% 100PPM	24773-225W
R12	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R13	RES CC 22R 1/8W 5%	24331-988T
R14	RES CC 4R7 1/8W 5%	24331-985S
R16	RES CC 68R 1/8W 5%	24331-979F
R17	RES CC 20R0 1/8W 5%	24331-929R
R19	RES CC 22R 1/8W 5%	24331-988T
R20	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R21	RES CC 39R 1/8W 5%	24331-994M
R22	RES CC 20R0 1/8W 5%	24331-929R
R23	RES MF 160R 1/4W 2% 100PPM	24773-254G
R24	RES MF 47K 1/4W 2% 100PPM	24773-313H
R25	RES MF 75K 1/4W 2% 100PPM	24773-318L
R30	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R31	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R32	RES CC 10K 1/8W 5%	24331-972H
R33	RES CC 100R 1/8W 5%	24331-997B
R34	RES MG 6M8 1/4W 5%	24321-883V
R35	RV CERM 200R LIN 1/2W 10%	25748-567W
R38	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R40	RES MG 2M2 1/4W 5%	24321-877J

Circuit Ref	Description	Part Number
Board AE6	- Amplifier/leveller	(Contd.)
R42	RES MG 2M2 1/4W 5%	24321-877J
R43	RES CC 100R 1/8W 5%	24331-997B
R44	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R45	RES MF 20K 1/4W 2% 100PPM	24773-304C
R46	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R47	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R48	RES MF 10K 1/4W 2% 100PPM	24773-297M
R50	RV CERM 20KO LIN 10%	25748-565V
R51	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R52	RES MF 43K 1/4W 2% 100PPM	24773-312Z
R53	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R54	RES MF 16K 1/4W 2% 100PPM	24773-302X
R55	RV CERM 5KO LIN 1/2W 10%	25748-563F
R56	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R58	RES MF 130K 1/4W 2% 100PPM	24773-324G
R59	RES MF 27K 1/4W 2% 100PPM	24773-307K
R60	RV CERM 2KO LIN 1/2W 10%	25748-562J
R61	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R62	RES MF 56K 1/4W 2% 100PPM	24773-315U
R67	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R68	RES MF 20K 1/4W 2% 100PPM	24773-304C
R69	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R70	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R71	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R74	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R76	RES NET 6K8 5% 9SIP	24681-602J
R77	RES MF 100K 1/4W 2% 100PPM	24773-321L
R78	RES MF 91K 1/4W 2% 100PPM	24773-320N
R79	RES MF 75K 1/4W 2% 100PPM	24773-318L
R80	RES MF 10K 1/4W 2% 100PPM	24773-297M
R81	RES MF 150K 1/4W 2% 100PPM	24773-325V
R82	RES MF 10K 1/4W 2% 100PPM	24773-297M
R83	RES MF 220K 1/4W 2% 100PPM	24773-329T
R84	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R85	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R86	RES MF 27K 1/4W 2% 100PPM	24773-307K
R87	RES MF 12K 1/4W 2% 100PPM	24773-299R
R88	RES MF 47R 1/4W 2% 100PPM	24773-241A
R89	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R90	RES CC 2K2 1/8W 5%	24331-983G
R91	RES MF 2K7 1/4W 2% 100PPM	24773-283L

Circuit Ref	Description		Part Number
Board AE6	- Amplifier/leveller		(Contd.)
R92	RES CC 470R 1/8W 5%		24331-964R
R93	RES MF 22K 1/4W 2% 100PPM		24773-305R
R94	RES MF 1MO 1/4W 2% 100PPM		24773-346E
R95	RES MF 1K2 1/4W 2% 100PPM		24773-275H
R96	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R97	RES CC 680R 1/8W 5%		24331-984V
R98	RES CC 6R8 1/8W 5%		24331-957P
R99	RES CC 82R 1/8W 5%		24331-996R
R100	RES MF 10K 1/4W 2% 100PPM		24773-297M
R101	RES MF 390R 1/4W 2% 100PPM		24773-263P
R102	RES MF 100K 1/4W 2% 100PPM		24773-321L
R103	RES MF 10K 1/4W 2% 100PPM		24773-297M
R104	RES MF 1K5 1/4W 2% 100PPM		24773-277U
R105	RES MF 6K2 1/4W 2% 100PPM		24773-292W
R106	RES MF 62K 1/4W 2% 100PPM		24773-316Y
R107	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R108	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R109	RES MF 10K 1/4W 2% 100PPM		24773-297M
R110	RES CC 1KO 1/8W 5%		24331-967A
R112	RES MF 10K 1/4W 2% 100PPM		24773-297M
R113	RES MF 47K 1/4W 2% 100PPM		24773-313H
R114	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R115	RES MF 1MO 1/4W 2% 100PPM		24773-346E
R116	RES MF 1MO 1/4W 2% 100PPM		24773-346E
R118	RES MF 36K 1/4W 2% 100PPM		24773-310K
R119	RES MF 91K 1/4W 2% 100PPM		24773-320N
R120	RES MF 9K1 1/4W 2% 100PPM		24773-296X
R122	RV CERM 5K LIN 1/2W 10% HORZ		25711-640F
TR1	TR NSI BFR90 15V 5G - AMP		28452-167U
TR2	TR NSI BFR90 15V 5G - AMP		28452-167U
TR3	TR NSI BFR96 15V 5G - AMP		28452-171Y
TR4	TR NMF VN10KM 60V 5R0 - VMOS	!	28459-046T
TR6	TR NSI BC208B 20V 150M - GEN		28452-781A
TR7	TR NSI MPS6531 40V 390M - AMP		28454-749A
TR8	TR PSI BC308B 20V 130M - GEN		28433-455R
TR9	TR NSI BC208B 20V 150M - GEN		28452-781A
TR10	TR NMF VN10KM 60V 5R0 - VMOS	!	28459-046T

Circuit Ref	Description	Part Number
Board AE7	- Switch	
53.	When ordering, prefix circuit reference with AE7	
	Complete unit	44828-491V
C1	CAP CER 10N 25V 20% DISC	26383-006C
C2	CAP CER 10N 25V 20% DISC	26383-006C
C5	CAP CER 4N7 63V 10% PLATE	26383-591B
C6	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C8	CAP CER 220N 50V 20% CHIP	26386-761E
C10	CAP CER 220N 50V 20% CHIP	26386-761E
C11	CAP CER 10N 25V 20% DISC	26383-006C
C12	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C14	CAP CER 1N0 63V 10% PLATE	26383-585M
C15	CAP CER 1N0 63V 10% PLATE	26383-585M
D1	DI SIL BA482 35V JUNC	28335-675R
D3	DI SIL BA482 35V JUNC	28335-675R
D5	DI PIN 5082-3379 50V	28383-997T
D6	DI PIN 5082-3379 50V	28383-997T
D7	DI PIN 5082-3379 50V	28383-997T
D8	DI PIN 5082-3379 50V	28383-997T
D9	DI H/CARR HP5082-2811	28349-008U
D10	DI H/CARR HP5082-2826	28349-011U
D12	DI H/CARR HP5082-2826	28349-011U
IC1	ICA AMP LM348N QUAD GP DIL14	28461-321E
IC2	ICA AMP TL071CP FET I/P DIL8	28461-347A
R1	RES MF 82K 1/4W 2% 100PPM	24773-319J
R2	RES MF 10K 1/4W 2% 100PPM	24773-297M
R3	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R6	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R9	RES CC 100R 1/8W 5%	24331-997B
R10	RES CC 130R 1/8W 5%	24331-954W
R11	RES MG 6M8 1/4W 5%	24321-883V
R12	RV CERM 200R LIN 1/2W 10% *	25748-567W
R14	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R15	RES MG 2M2 1/4W 5%	24321-877J
R16	RES MG 2M2 1/4W 5%	24321-877J
R17	RES CC 130R 1/8W 5%	24331-954W
R19	RES CC 470R 1/8W 5%	24331-964R
R20	RES CC 1K0 1/8W 5%	24331-967A

Circuit Ref	Description	Part Number
Unit AF0	- Front panel	
54.	When ordering, prefix circuit reference with AF0	
	Complete unit	44990-468A
	KNOB ASSEMBLY Ø 32.0 6.0 I/D	41149-067C
	KNOB ASSEMBLY Ø 31.0 4.0 I/D	41149-068R
	KNOB ASSEMBLY Ø 31.0 4.0 I/D	41149-068R
	KNOB CAP	37590-282D
	CABLE ASSEMBLY AE6 - TG SKT	43129-919J
	FRONT PANEL KEYBOARD AF1	44828-494D
	FRONT PANEL LOGIC AF2	44828-495T
	ENCODER ASSEMBLY AZ1	44990-455W
	SWEEP SPAN SWITCH AZ2	44828-498W

Circuit Ref	Description	Part Number
Board AF1	- Front panel keyboard	
55.	When ordering, prefix circuit reference with AF1	
	Complete unit	44828-494D
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
D1	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D2	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D3	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D4	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D5	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D6	LAMP LED HLMP 1401 2.4V YELLOW	28624-137D
D7	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D8	LAMP LED HLMP 1401 2.4V YELLOW	28624-137D
D9	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D10	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D11	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D12	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D13	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D14	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D15	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D16	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D17	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D18	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D19	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D20	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D21	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D22	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D23	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D24	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D25	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D26	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D27	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D28	LAMP LED HLMP 1503 3.0V GRN	28624-138T
D29	LAMP LED OPL271 2.7V GRN	28624-120A
IC1	ICA COMP LM339N QUAD	28461-693H
IC2	ICA COMP LM339N QUAD	28461-693H
IC3	ICD ENCOD 74LS148 8INP PRIOR	28465-024N
IC4	ICD ENCOD 74LS148 8INP PRIOR	28465-024N
IC5	ICD NAND 74LS00 QUAD 2INP	28466-345H

Circuit Ref	Description	Part Number
Board AF1	- Front panel keyboard	(Contd.)
R1	RES NET 4K7 2% 8DIL	24681-519Z
R2	RES NET 220R 2% 8DIL	24681-501F
R3	RES MF 15K 1/4W 2% 100PPM	24681-301P
R4	RES MF 220R 1/4W 2% 100PPM	24773-257W
R5	RES NET 4K7 5% 8DIL	24681-519Z
R6	RES MF 15K 1/4W 2% 100PPM	24773-301P
R7	RES MF 15K 1/4W 2% 100PPM	24773-301P
SAA	SW PUSH 1CO 24V 10MA	23465-411B
SAB	SW PUSH 1CO 24V 10MA	23465-411B
SAC	SW PUSH 1CO 24V 10MA	23465-411B
SAH	SW PUSH 1CO 24V 10MA	23465-411B
SAJ	SW PUSH 1CO 24V 10MA	23465-411B
SAL	SW PUSH 1CO 24V 10MA	23465-411B
SBA	SW PUSH 1CO 24V 10MA	23465-411B
SBB	SW PUSH 1CO 24V 10MA	23465-411B
SBC	SW PUSH 1CO 24V 10MA	23465-411B
SBD	SW PUSH 1CO 24V 10MA	23465-411B
SBE	SW PUSH 1CO 24V 10MA	23465-411B
SBH	SW PUSH 1CO 24V 10MA	23465-411B
SBJ	SW PUSH 1CO 24V 10MA	23465-411B
SCA	SW PUSH 1CO 24V 10MA	23465-411B
SCB	SW PUSH 1CO 24V 10MA	23465-411B
SCC	SW PUSH 1CO 24V 10MA	23465-411B
SCD	SW PUSH 1CO 24V 10MA	23465-411B
SCE	SW PUSH 1CO 24V 10MA	23465-411B
SCH	SW PUSH 1CO 24V 10MA	23465-411B
SCJ	SW PUSH 1CO 24V 10MA	23465-411B
SDA	SW PUSH 1CO 24V 10MA	23465-411B
SDB	SW PUSH 1CO 24V 10MA	23465-411B
SDC	SW PUSH 1CO 24V 10MA	23465-411B
SDD	SW PUSH 1CO 24V 10MA	23465-411B
SDE	SW PUSH 1CO 24V 10MA	23465-411B
SDH	SW PUSH 1CO 24V 10MA	23465-411B
SDJ	SW PUSH 1CO 24V 10MA	23465-411B
SDL	SW PUSH 1CO 24V 10MA	23465-411B
SEA	SW PUSH 1CO 24V 10MA	23465-411B
SEB	SW PUSH 1CO 24V 10MA	23465-411B
SEC	SW PUSH 1CO 24V 10MA	23465-411B
SED	SW PUSH 1CO 24V 10MA	23465-411B
SEE	SW PUSH 1CO 24V 10MA	23465-411B
SHA	SW PUSH 1CO 24V 10MA	23465-411B
SHB	SW PUSH 1CO 24V 10MA	23465-411B

Circuit Ref	Description	Part Number
Board AF1	- Front panel keyboard	(Contd.)
SHC	SW PUSH 1CO 24V 10MA	23465-411B
SJA	SW PUSH 1CO 24V 10MA	23465-411B
SJB	SW PUSH 1CO 24V 10MA	23465-411B
SJC	SW PUSH 1CO 24V 10MA	23465-411B
SJD	SW PUSH 1CO 24V 10MA	23465-411B
SJE	SW PUSH 1CO 24V 10MA	23465-411B
SJH	SW PUSH 1CO 24V 10MA	23465-411B
SJJ	SW PUSH 1CO 24V 10MA	23465-411B
SLA	SW PUSH 1CO 24V 10MA	23465-411B
SLB	SW PUSH 1CO 24V 10MA	23465-411B
SLC	SW PUSH 1CO 24V 10MA	23465-411B
SMA	SW PUSH 1CO 24V 10MA	23465-411B
X7	SW CAP RECT BK "^" (up arrow)	37590-932V
X8	SW CAP RECT BK "v" (down arrow)	37590-933S
X14	SW CAP RECT BK "REF FREQ"	37590-946K
X15	SW CAP RECT BK "INC FREQ"	37590-947A
X16	SW CAP RECT BK "REF LEVEL"	37590-927F
X17	SW CAP RECT BK "PEAK FIND"	37590-952H
X18	SW CAP RECT BK "INTMD IDENT"	37590-953E
X19	SW CAP RECT BK "A B SELECT"	37590-954U
X20	SW CAP RECT BK "A B SELECT"	37590-955Y
X21	SW CAP RECT BK "VIDEO"	37590-625W
X22	SW CAP RECT BK "EXT"	37590-626D
X23	SW CAP RECT BK "SINGLE ARM"	37590-956N
X24	SW CAP RECT BK "LINE"	37590-957L
X25	SW CAP RECT BK "AUTO"	37590-958J
X26	SW CAP RECT BK "NORM"	37590-959F
X27	SW CAP RECT BK "LOG"	37590-960L
X28	SW CAP RECT BK "2"	37590-963G
X29	SW CAP RECT BK "1"	37590-962F
X30	SW CAP RECT BK "5"	37590-964V
X31	SW CAP RECT BK "0.5"	37590-961J
X32	SW CAP RECT BK "VOLTS /DIV"	37590-966W
X33	SW CAP RECT BK "10"	37590-965S
X34	SW CAP RECT BK "TRACK GEN"	37590-967D
X35	SW CAP RECT BK "FULL SPAN"	37590-968T
X36	SW CAP RECT GRN "PRESET"	37590-969P
X37	SW CAP RECT BK "MKR1"	37590-970D
X38	SW CAP RECT BK "MKR2"	37590-971T
X39	SW CAP RECT BK "FREQ COUNT"	37590-972P
X40	SW CAP RECT BK "ZERO SPAN"	37590-973X
X41	SW CAP RECT BK "/DIV"	37590-974M

Circuit Ref	Description	Part Number
Board AF1	- Front panel keyboard	(Contd.)
X42	SW CAP RECT BK "AUTO TRIG"	37590-975C
X43	SW CAP RECT BK "1 2 MOVE"	37590-976R
X44	SW CAP RECT BK "START"	37590-977B
X45	SW CAP RECT BK "METER"	37590-978K
X100	CABLE RIBBON (AF1-AF2)	43129-963D

Circuit Ref	Description	Part Number
Board AF2	- Front panel logic	
56.	When ordering, prefix circuit reference with AF2	
	Complete unit	44828-495T
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C17	CAP ELEC 1U0 50V 20% SUBMIN	26421-106B
C18	CAP CER 220P 63V 2% PLATE	26343-481S
C19	CAP CER 220P 63V 2% PLATE	26343-481S
C20	CAP CER 2N2 63V 10% PLATE	26383-587R
C21	CAP CER 2N2 63V 10% PLATE	26383-587R
C22	CAP ELEC 100N 50V 20% SUBMIN	26421-100T
C23	CAP ELEC 100N 50V 20% SUBMIN	26421-100T
C24	CAP CER 1N0 63V 10% PLATE	26383-585M
IC1	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC2	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC3	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC4	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC5	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC6	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC7	ICD ENCOD 74LS348 8INP PRTY TS	28465-028G
IC8	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC9	ICD MONO 74LS221 DUAL	28468-404D
IC10	ICD MONO 74LS221 DUAL	28468-404D
IC11	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC12	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC13	ICD MONO 74LS123 DUAL RETR	28468-309B

Circuit Ref	Description	Part Number
Board AF2	- Front panel logic	(Contd.)
IC14	ICD XOR 74LS86 QUAD 2INP	28466-406C
IC15	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
R1	RES MF 15K 1/4W 2% 100PPM	24773-301P
R2	RES MF 15K 1/4W 2% 100PPM	24773-301P
R3	RES MF 15K 1/4W 2% 100PPM	24773-301P
R4	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R5	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R6	RES MF 360R 1/4W 2% 100PPM	24773-262T
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 360R 1/4W 2% 100PPM	24773-262T
R9	RES MF 10K 1/4W 2% 100PPM	24773-297M
R10	RES NET 100R 2% 8SINGLE DIL	24681-515R
R11	RES NET 100R 2% 8SINGLE DIL	24681-515R
R12	RES NET 100R 2% 8SINGLE DIL	24681-515R
R13	RES MF 15K 1/4W 2% 100PPM	24773-301P
R15	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R16	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R20	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R21	RES MF 560R 1/4W 2% 100PPM	24773-267R
R22	RES MF 560R 1/4W 2% 100PPM	24773-267R
R23	RES NET 100R 2% 8SINGLE DIL	24681-515R
R24	RES WW 120R 1.5W 5%	25123-052F

Circuit Ref	Description	Part Number
Unit AR0	- Rear panel	
57.	When ordering, prefix circuit reference with AR0	
	Complete unit	44990-469Z
IC1 (1)	ICA VREG LM337T PROG 1A5	28461-727Z
IC2 (1)	ICA VREG LM337T PROG 1A5	28461-727Z
IC3 (1)	ICA VREG LM317T PROG 1A5	28461-726A
LS1	LOUDSPEAKER ROUND 75R 2.25"	23646-105A
MP1	FAN AX 24V DC BRUSHLESS 119MM	23535-123X
MP2	FAN ACC FILTER FOR 23535-123	23535-110L
R1	RV CERM 10K LIN 2W 10% +SWITCH	25737-003S
R2	RV CERM 10K LIN 2W 10% SINGLE	25737-002V
SKV	CON RF BNC FEM 50 BKHD RG178	23443-548H
SKW	CON RF BNC FEM 50 BKHD RG178	23443-548H
SKX	CON RF BNC FEM 50 BKHD RG178	23443-548H
	CABLE ASSEMBLY AD2-SKA TO 'EXT TRIG'	43130-247B

(1) IC1-3 APPEAR IN CCT.DRG, FOR AR2

Circuit Ref	Description	Part Number
Board AR1	- Signal interface board	
58.	When ordering, prefix circuit reference with AR1	
	Complete unit	44828-496P
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
D1	DI CUR REG J505 - 1 MA TO92	28383-986L
IC1	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC2	ICD BUFF 74LS126A QUAD 3ST	28469-101U
IC3	ICD AND 74LS08 QUAD 2INP	28466-012L
IC4	MOD OPTO TIL113 ISOL	28625-006U
IC5	MOD OPTO CNX38 ISOL 1K5V	28625-007Y
R1	RES MF 180K 1/4W 2% 100PPM	24773-327W
R2	RES MF 820R 1/4W 2% 100PPM	24773-271B
R5	RES MF 10K 1/4W 2% 100PPM	24773-297M
R6	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R7	RES MF 39K 1/4W 2% 100PPM	24773-311A
R8	RES MF 4K7 1/4W 2% 100PPM	24773-289W
SKS	CON D FEM 25 FXD PCB STRT	23435-508P
SKT	CON D FEM 25 FXD PCB STRT	23435-508P
TR1	TR NSI BC237A 45V 150M - GEN	28455-421X
TR2	TR NSI BC237A 45V 150M - GEN	28455-421X
X1	CON PART D SCREWLOCK FEM	23435-981V
X2	CON PART D SCREWLOCK FEM	23435-981V
X3	CON PART D SCREWLOCK FEM	23435-981V
X4	CON PART D SCREWLOCK FEM	23435-981V
X5	S/C ACC PAD TO18 ETC TO .1"GRID	28488-115L

Circuit Ref	Description	Part Number
Board AR2	- Power supply interface	
59.	When ordering, prefix circuit reference with AR2	
	Complete unit	44828-497X
C1	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C2	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C3	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C4	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C5	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C6	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C7	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C8	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C9	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C10	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C11	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C12	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C14	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C15	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C16	CAP PETP 100N 63V 10% RAD MIN	26582-429F
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
D10	DI RECT 1N4004 400V	28357-028K
D11	DI SIL 1N4148 75V JUNC	28336-676J
D12	DI SIL 1N4148 75V JUNC	28336-676J
D13	DI SIL 1N4148 75V JUNC	28336-676J
FS1	FUSE Q/ACT 3.15A 20X5	23411-008L
IC1 IC2 }	SEE REAR PANEL ASSY. AR0	
IC3		
IC4	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC5	ICA COMP LM339N QUAD	28461-693H
L5	IND 320uH	44190-038A

Circuit Ref	Description	Part Number
Board AR2	- Power supply interface	(Contd.)
R1	RES MF 240R 1/4W 2% 100PPM	24773-258D
R2	RV CERM 100R LIN .5W 10% VERT	25711-608S
R3	RES MF 750R 1/4W 2% 100PPM	24773-270R
R4	RES MF 240R 1/4W 2% 100PPM	24773-258D
R5	RV CERM 500R LIN .5W 10% VERT	25711-604J
R6	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R7	RES MF 240R 1/4W 2% 100PPM	24773-258D
R8	RV CERM 500R LIN .5W 10% VERT	25711-604J
R9	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R10	RES MF 1R0 1/4W 2% 100PPM	24773-201M
R11	RES MG 10M 1/4W 5%	24321-885W
R12	RES MF 100K 1/4W 2% 100PPM	24773-321L
R13	RES MF 27K 1/4W 2% 100PPM	24773-307K
R14	RES MF 100R 1/4W 2% 100PPM	24773-249J
R18	RES MF 47K 1/4W 2% 100PPM	24773-313H
R19	RES MF 300K 1/4W 2% 100PPM	24773-332T
R20	RES MF 100K 1/4W 2% 100PPM	24773-321L
R21	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R22	RES MF 390R 1/4W 2% 100PPM	24773-263P
R23	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R24	RES MF 100K 1/4W 2% 100PPM	24773-321L
R25	RES MF 100K 1/4W 2% 100PPM	24773-321L
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R30	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R31	RES MF 18K 1/4W 2% 100PPM	24773-303M
R32	RES MF 18K 1/4W 2% 100PPM	24773-303M
R33	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R34	RES MF 100K 1/4W 2% 100PPM	24773-321L
R36	RES MF 24K 1/4W 2% 100PPM	24773-306B
R37	RES MF 12K 1/4W 2% 100PPM	24773-299R
R38	RES MF 100R 1/4W 2% 100PPM	24773-249J
R39	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R40	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R41	RES MF 11K 1/4W 2% 100PPM	24773-298C
R42	RES MF 13K 1/4W 2% 100PPM	24773-300T
R43	RES MF 100R 1/4W 2% 100PPM	24773-249J
R44	RES MF 39K 1/4W 2% 100PPM	24773-311A
R45	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R46	RES MF 100R 1/4W 2% 100PPM	24773-249J
SKN	CON JUMP FEM 2 1 ROW	23435-990X
SKP	CON D FEM 37 FXD PCB STRT	23435-509X
SKR	CON D FEM 37 FXD PCB STRT	23435-509X

Circuit Ref	Description		Part Number
Board AR2	- Power supply interface		(Contd.)
TR1	TR PSI BC307A 45V 130M - GEN		28435-227H
TR2	TR NMF VN10KM 60V 5RO - VMOS	!	28459-046T
TR3	TR NSI TIP112 100V 5M DAR		28457-822L
TR4	TR NSI BC209C 20V 150M - GEN		28452-771P
TR5	TR NSI BC209C 20V 150M - GEN		28452-771P
TR6	TR PSI BC308B 20V 130M - GEN		28433-455R
TR7	TR PSI BC308B 20V 130M - GEN		28433-455R
X1	CORE BEAD 5X.7X10LG 3S2		23635-811Z
X2	CORE BEAD 5X.7X10LG 3S2		23635-811Z
X3	CORE BEAD 5X.7X10LG 3S2		23635-811Z
X4	CORE BEAD 5X.7X10LG 3S2		23635-811Z
X5	CON PART D SCREWLOCK FEM		23435-981V
X6	CON PART D SCREWLOCK FEM		23435-981V
X7	CON PART D SCREWLOCK FEM		23435-981V
X8	CON PART D SCREWLOCK FEM		23435-981V
X9	H/W FUSE CARRIER OPEN 20X5		23416-151D
X15	S/C ACC WASHER 6BA/M3 INSUL		28488-127P
X16	S/C ACC BUSH M3 INSUL		28488-134R

Circuit Ref	Description	Part Number
Board AZ1	- Optical encoder assembly	
60.	When ordering, prefix circuit reference with AZ1	
	Complete unit	44990-455W
Board AZ2	- Sweep span switch	
61.	When ordering, prefix circuit reference with AZ2	
	Complete unit	44828-498M

MECHANICAL PARTS

Order without prefix

Fig. 1 Ref.	Description	Part Number
1	Top cover	35903-575V
2	Bottom cover	35903-576S
3	Trim front (2 off)	34900-862W
4	Front panel, marked	35903-571L
5	Rear panel	35903-500E
6	Trim, rear	34900-470E
7	Knob assembly 32.0 mm 6.0 I/D	41149-067C
8	Knob assembly 31.0 mm 4.0 I/D (2 off)	41149-068R
	Knob cap (3 off)	37590-282D
9	Panel handle	41700-382P
10	Clip (2 off)	35903-721D
	Insulator (2 off)	37490-701F
	Shouldered washer (4 off)	37590-856J
11	Foot plastic black 0.75 mm O/D (4 off)	22315-663B
12	Foot ring (2 off)	33900-913H
13	Foot rear, left hand	34900-864T
	Foot rear, right hand	34900-863D
14	Side rail (2 off)	34900-476F
15	End cap (2 off)	37590-255C
	End cap (2 off)	37590-256R
16	Handle, p.v.c. (2 off)	22315-590M
	Handle, steel (4 off)	22315-587M
	Cap (4 off)	37590-257B

(To be issued later)

Fig. 1 Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

CONTENTS

Para.
1 Circuit notes
1 Component values
3 Symbols
5 PCB layouts
6 Default settings
7 Debug operations

Fig.	Unit	Title	Comp. layout Page	Cct. drg. Page
1) 2)	2382	HT routeing and colour code diagram		(7/8 (9/10
3	AA0	AA tray interconnection		11/12
4	(AA1a (AB8	Input attenuator assembly) Overload detector)	13	13
5	+(AA2a +(AA3a	Input filter and mixer) 502.6 MHz i.f. filter and second mixer)	15	15
6	+ AA4	Sampling gate	17	17
7	+ AA5	Master v.c.o.	19	19
8	+(AA6 +(AB2 +(AB7	Divider) Interpolation oscillator) Oscillator select)	23	23
9	+ AA7	Slave v.c.o.	25	25
10	+ AA8	Master/slave phase detector	27	27
11	+(AA9 +(AA10	Second LO v.c.o.) Sampling gate)	29/30	29/30
12	AA11	Line cleaner	31/32	31/32
13	AB0	AB tray interconnection		33
14)				35/36
15)	+ AB1	D-A converter	35/36	37/38
16)				39
8	+ AB2	Interpolation oscillator	23	23
17	+(AB3 +(AB4	Master v.c.o.) Sampling gate)	41	41
18	+(AB5 +(AB6	Slave v.c.o.) Phase detector)	43/44	43/44
8	+ AB7	Oscillator select	23	23
4	AB8	Overload detector	13	13
19	AC0	AC tray interconnection		45

CONTENTS (continued)

Fig.	Unit	Title	Comp. layout Page	Cct. drg. Page
20	+(AC1 +(AC6	50 MHz crystal oscillator) Phase detector)	49/50	49/50
21	AC2	47.4 MHz i.f. amplifier	51/52	51/52
22) 23)	AC3	2.6 MHz LC filter	53/54	(53/54 (55/56
24) 25)	AC4	100 kHz i.f. crystal filter	57/58	(57/58 (59/60
26) 27)	AC5	2.6 MHz crystal filters	61/62	(61/62 (63/64
28	AD0	AD tray interconnection		65
29) 30)	+AD1	Logarithmic amplifier	67/68	(67/68 (69
31) 32) 33) 34)	+AD2	Logarithmic amplifier interface	73	(71 (73 (75 (77
35) 36) 37) 38)	+AD3	Microprocessor	79	(79 (81/82 (83/84 (85
39	+AD4	10 MHz calibrator	87/88	87/88
40	AE0	AE tray interconnection		89
41	+AE1	47.4 MHz crystal oscillator	91	91
42	+(AE2 +(AE3a	Buffer) Narrow band mixer/buffer)	93	93
43	+(AE4 +(AE5a	TG buffer) Wide band mixer/buffer)	95/96	95/96
44	+AE6	Amplifier leveller)	99/100	97
45	AE7	Switch)		99/100
46	AF0	AF front panel interconnections		101/102
47	AF1	Front panel keyboard	103/104	103/104
48) 49)	AF2	Front panel logic	105/106	(105/106 (107/108
50	AR0	Rear panel interconnections		109
51	+AR1	Signal interface board	111/112	111/112
52	AR2	Power supply interface	113/114	113/114
53	AZ1	Optical encoder		115/116
54	AZ2	Span switch board		117/118

+ = c.r.o. waveforms provided

CIRCUIT NOTES

Component values

1. Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), µ = microfarads (10^{-6}).
n = nanofarads (10^{-9}), p = picofarads (10^{-12}).

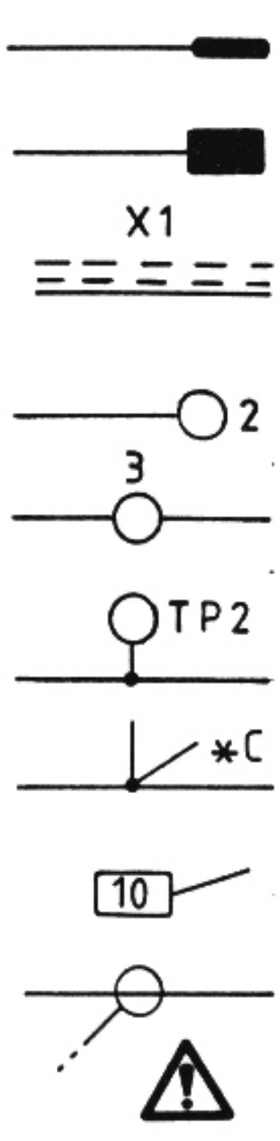
Inductors : Code letter H = henrys, m = millihenrys (10^{-3}).
µ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

SIC : value selected during test, nominal value shown.

2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys each value is placed near to its related symbol.

Symbols

3. Symbols are based on the provisions of BS 3939 with the following additions:



edge connector

on-board connector

ferrite bead

tags

test point

other point used for test

waveform no.

current probe

warning, see page (iv), Notes and Cautions

unit identification number

printed component

4. Electro-mechanical relays are all shown according to convention, in the de-energized state with all power supplies removed.

PCB layouts

5. PCB layouts are shown as viewed from the component side.

Default settings

6. The waveforms reproduced in this chapter were plotted from a digitizing c.r.o. used as a monitor on selected test points. The screen legends showed unsuppressed zeros after decimal points which were characteristic of the c.r.o. The most frequent c.r.o. settings used to obtain a c.r.o. display of a 2382/2380 under test are described in this chapter as 'default settings'. These are basic settings unless overridden by additional procedures which accompany some waveform photographs.

Sufficient information is given to go direct to a particular waveform (with reference to the Operating Manual if necessary). Attempts to curtail the procedure are likely to result in the incorrect instrument conditions.

Service engineers should be warned that a decision based on inspection of a single waveform can be misleading as the digitizing c.r.o. had a higher resolution than the models generally available to service engineers.

SCOPE SETTING [DEFAULT]
CH1 [2V/DIV]:
CH2 [OFF]:
TRIGGER [AUTO, +ve, CH1]:
MAIN TIMEBASE [ON]:
DELAY TIMEBASE [ON]:
MODE [MAIN TIMEBASE, MULTIPLE SWEEP]:

2382/2380 default setting under
PROCEDURE
1. SWITCH ON,

KEY; CH1 and CH2 are channels 1 and 2 of the c.r.o. with channel 1 displayed above channel 2 on the tube.

Debug operations

7. The terms 'debug operations mode' and 'diagnostic mode' are synonymous for the complete instrument 2382/2380.

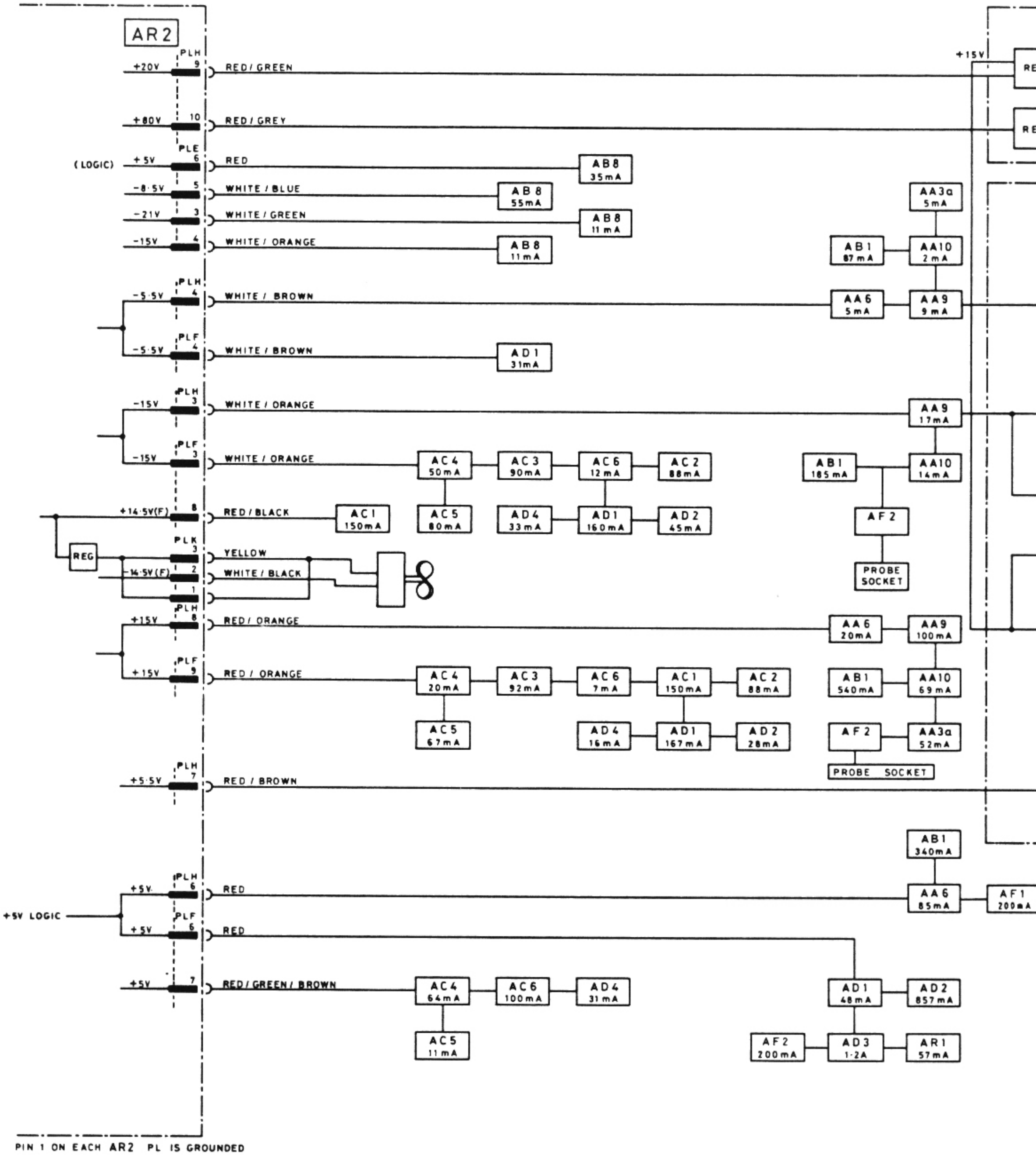
The following procedure applies in this chapter whenever the instruction 'enter debug operations mode' appears:-

On unit 2382 hold [INTMD IDENT] key in the depressed position throughout this sequence.

On unit 2380, press [2ND FUNCT], [SET TG], [2ND FUNCT], [REF LEVEL], 23.82 dB on function/data keypad.

Release [INTMD IDENT] key.

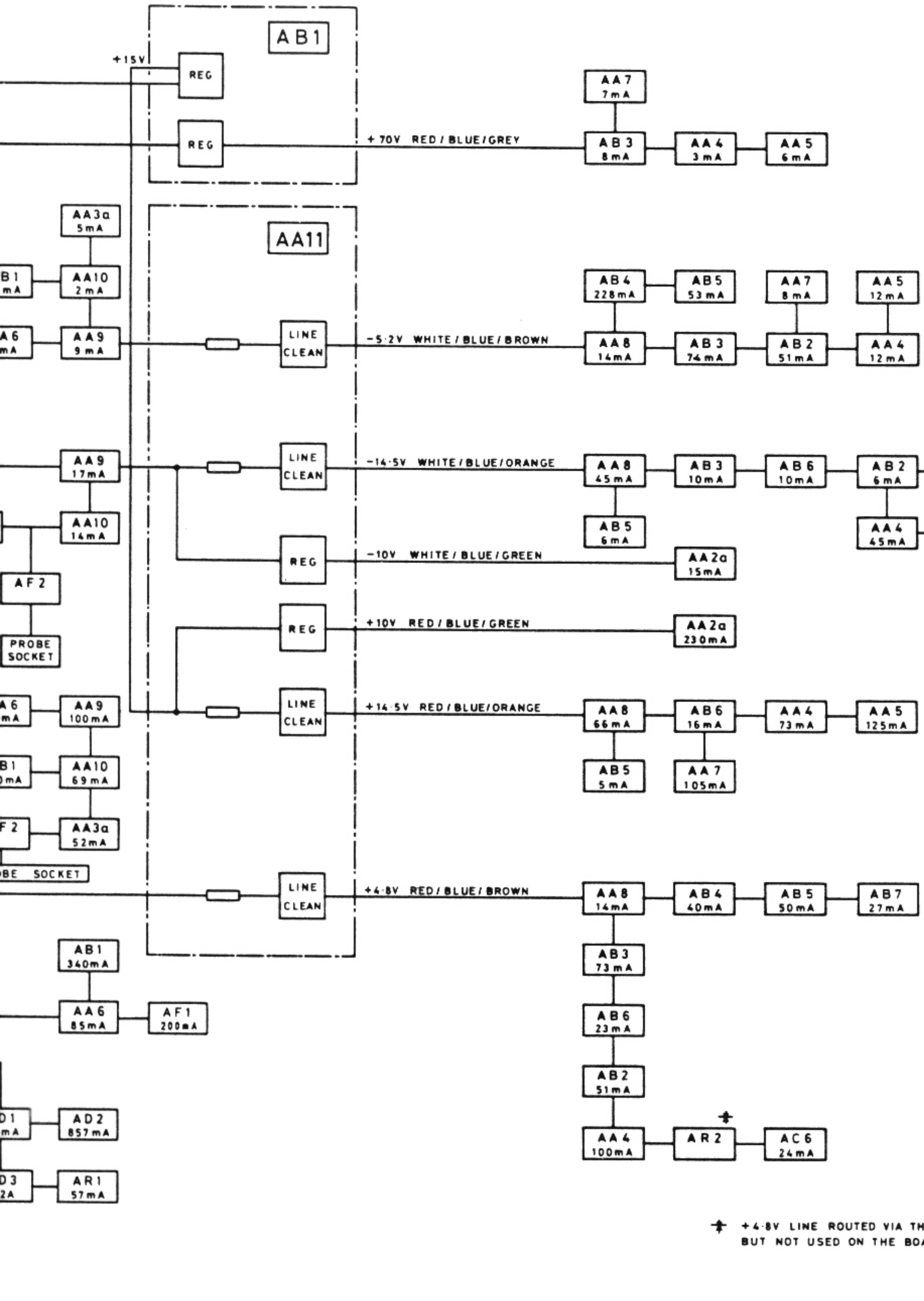
H.T. ROUTING AND COLOUR



Drg. No. Z52382-900
Sh. 1 Iss. 1

HT routing & col

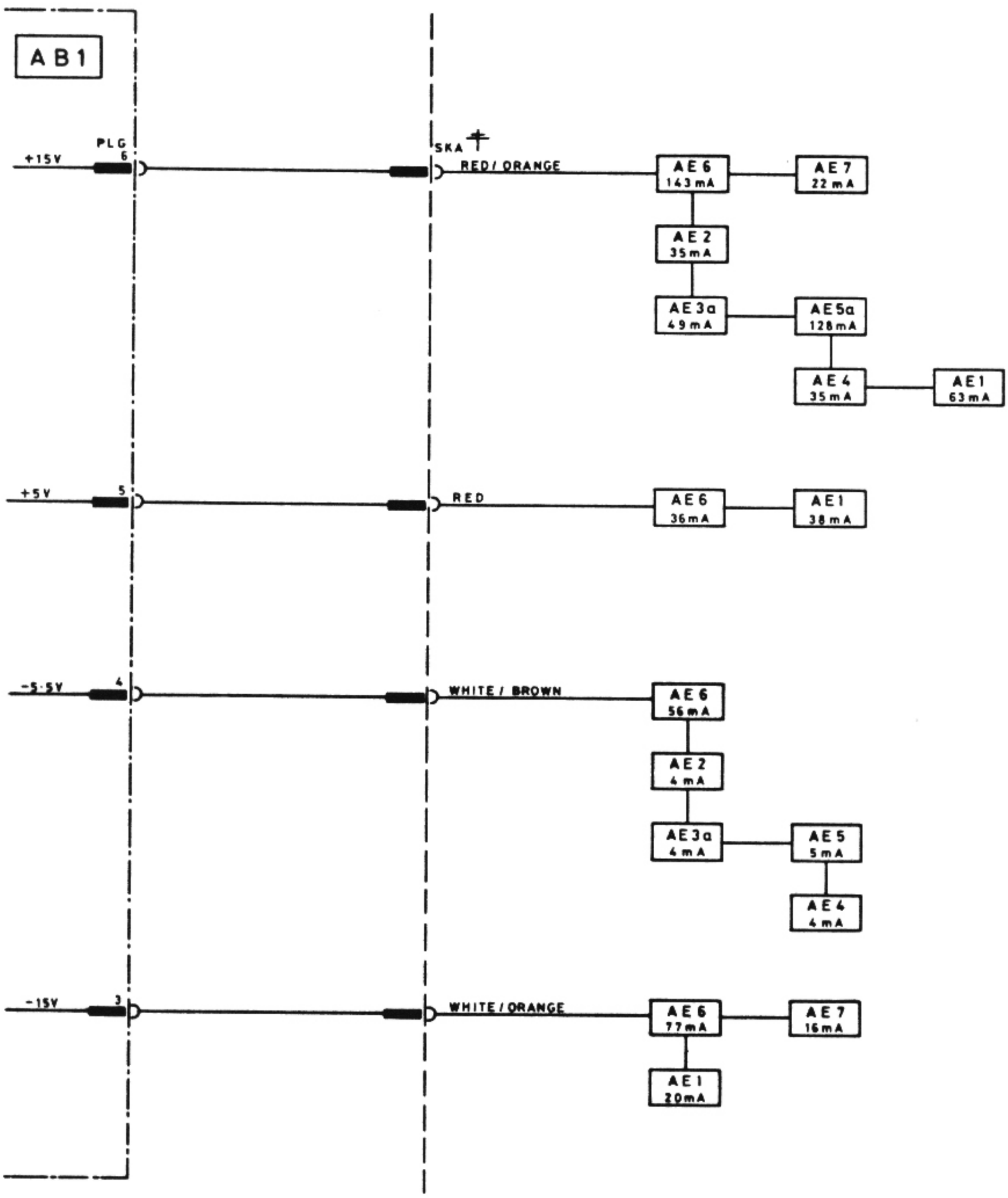
T. ROUTING AND COLOUR CODE DIAGRAM



HT routing & colour code diagram

Fig. 1
Chap. 7
Page 7/8

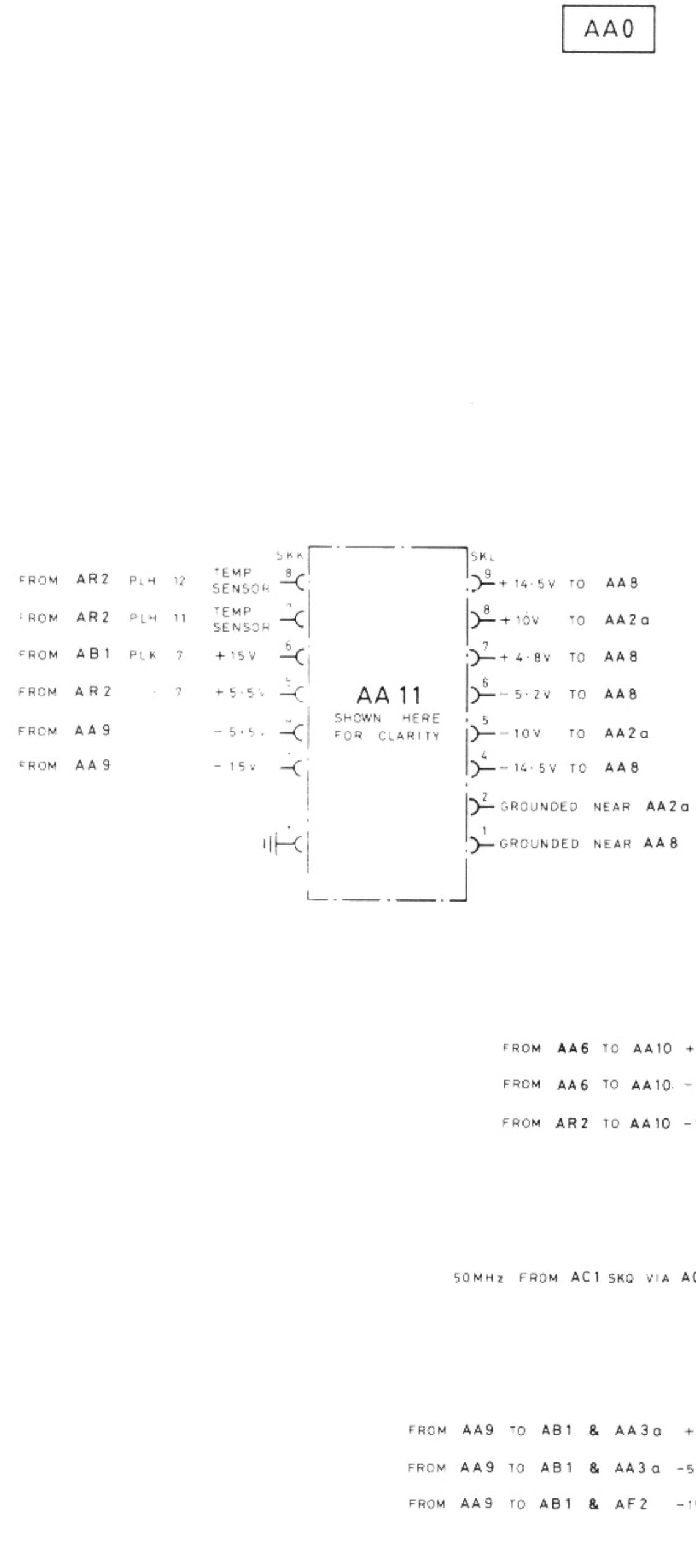
H.T. ROUTING AND COLOUR CODE DIAGRAM



Drg. No. Z52382-900
Sh. 2 Iss. 1

HT routing & colour code diagram

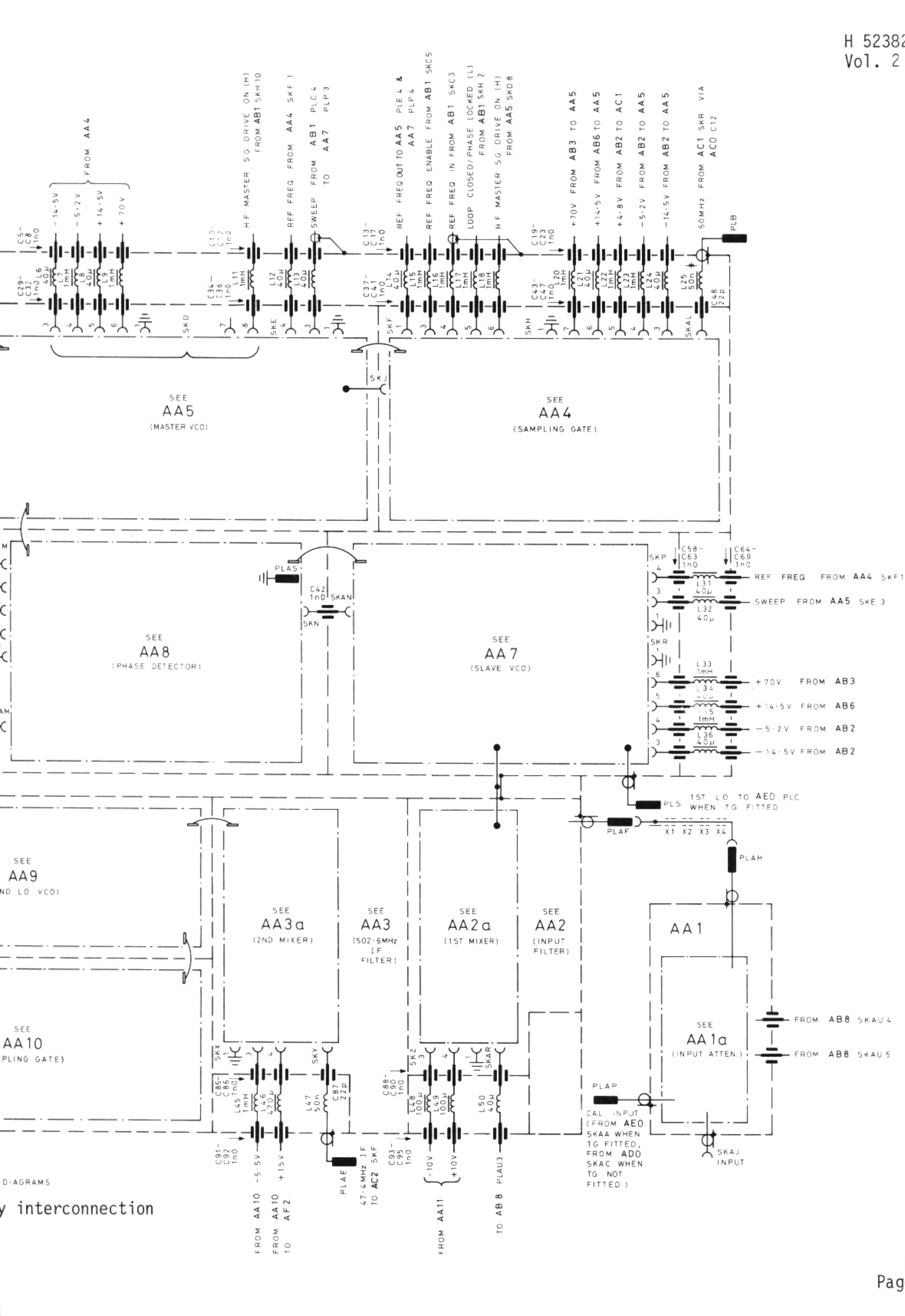
AA0



NOTE: ALL OTHER INTERBOARD CONNECTIONS ARE SHOWN ON THEIR RESPECTIVE CIRCUIT DIAGRAMS
ǂ INDUCTOR FORMED ON INNER OF COAX

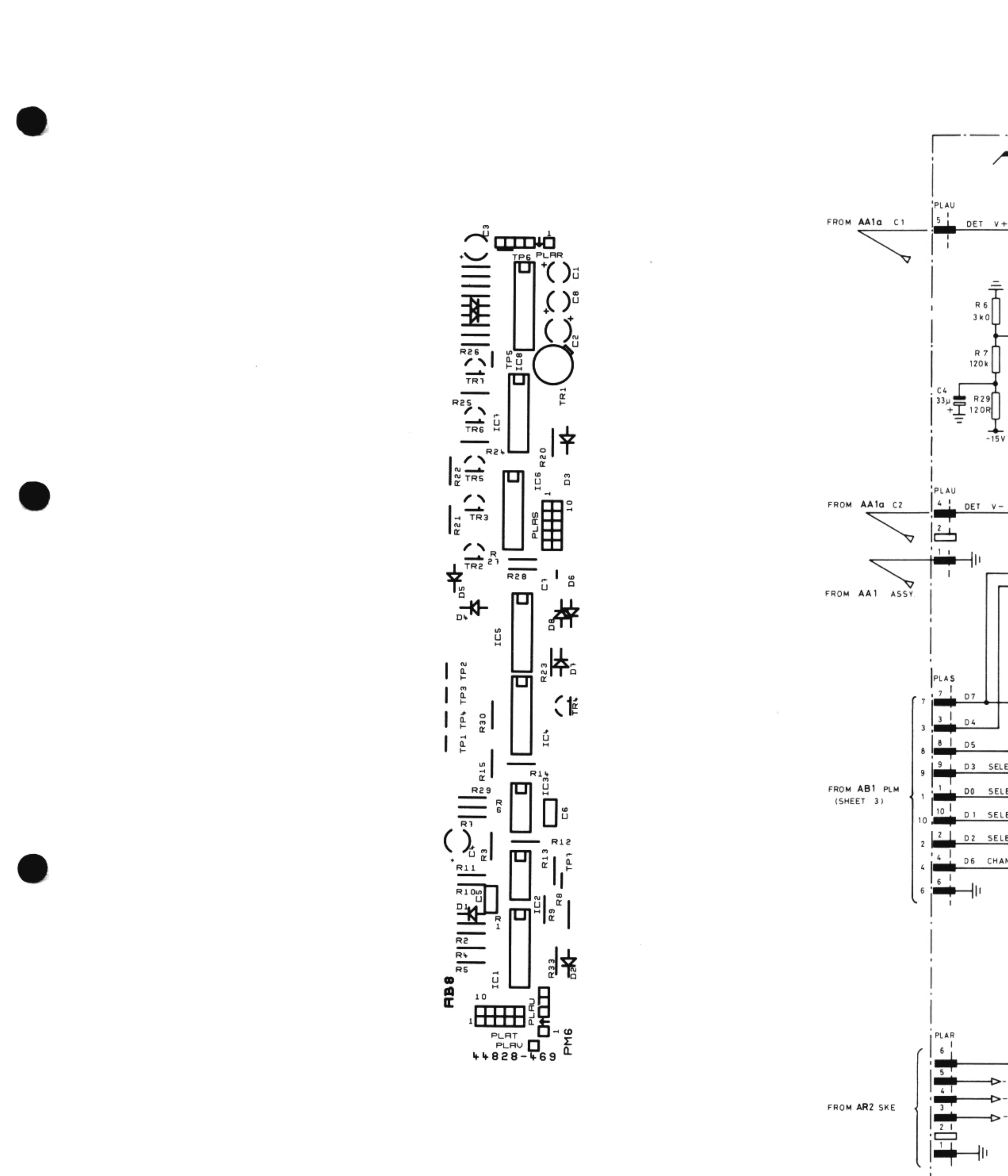
Drg.No. Z44990-450
Sh.1 Iss.3

AA0 : AA tray interconnection



DIAGRAMS

y interconnection



Drg. No. Z4
Sh. 3 Is

AB8 Component layout for AB8

Fig. 4

May 86

AB 8
44828-469B

OVERLOAD THRESHOLD

TRIP LOGIC

SOLENOID PULSER

INPUT/CAL OVERLOAD SWITCH

FROM AA1a C1

FROM AA1a C2

FROM AA1 ASSY.

FROM AB1 PLM (SHEET 3)

FROM AR2 SKE

D1 HP5082-2826

D2 HP5082-2826

D3 1N4004

D7 BAT29

D8 BAT29

D9 BAT29

D10 BAT29

IC1(a) TL074

IC1(b)

IC1(c)

IC2 LM311

IC3 LM311

IC4(a) LS132

IC4(b)

IC4(c)

IC4(d) LS132

IC5(a) LS00

IC5(b)

IC5(c)

IC5(d)

IC6(b) LM339

IC6(c) LM339

IC7(d) LM339

IC8(a) LS123

IC8(b) LS123

TR1 2N2219A

TR2 BC212B

TP1

TP2

TP3

TP4

TP5

TP6

OVERLOAD CLEAR (L)

SELECT SWITCH (A)

SELECT SWITCH (B)

D0 SELECT 10dB

D1 SELECT 20dB

D2 SELECT 30dB

D3 SELECT 3dB

D4

D5

D6 CHANGE (L)

D7

INPUT

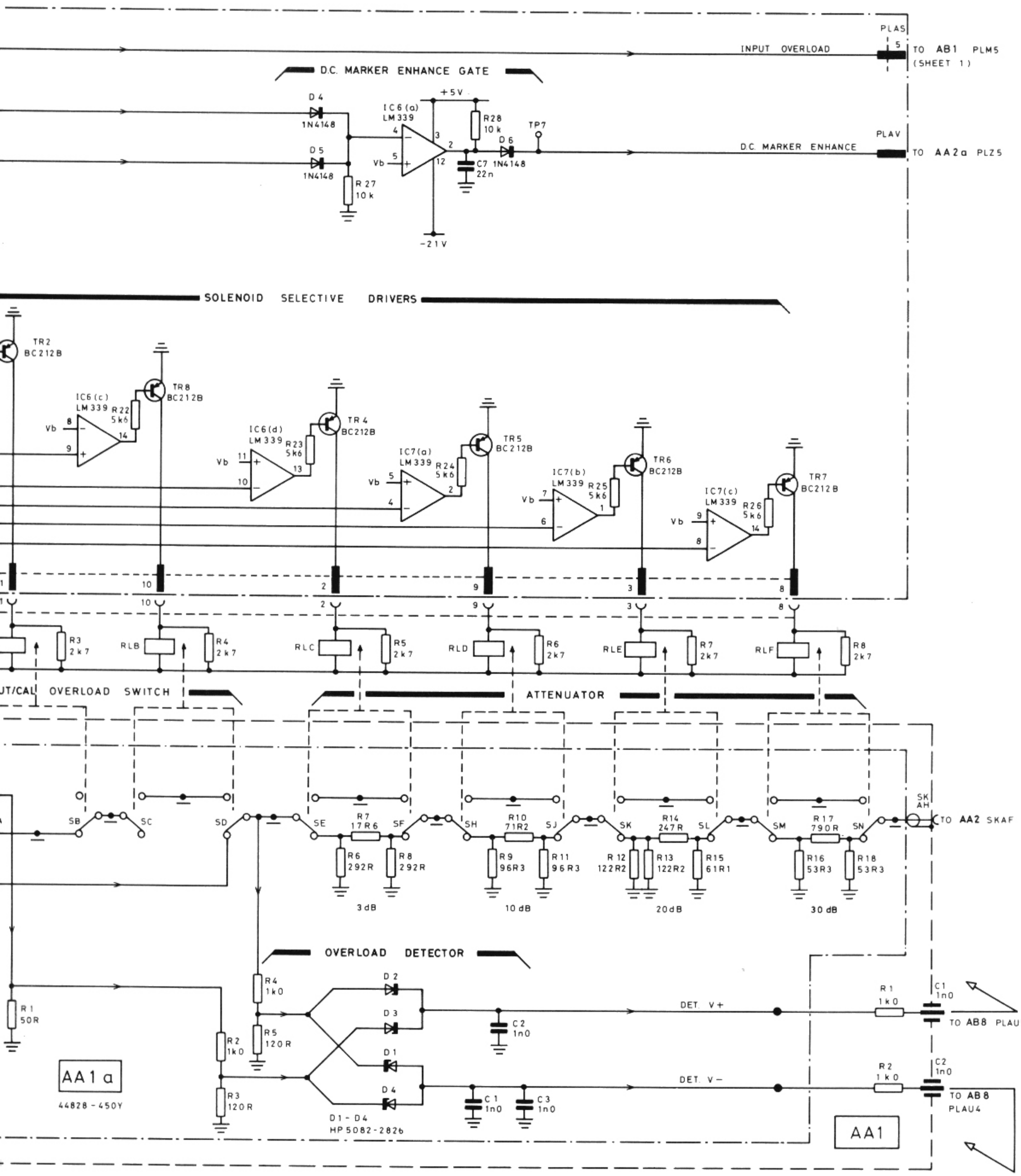
CAL INPUT (FROM AE0 SKAA WHEN TG FITTED;) FROM AC0 SKAC WHEN TG NOT FITTED.

SUPPLY LINE TABLE		
IC	+5V	GROUND
IC4	14	7
IC5	14	7
IC8	16	8

AA1a
44828-450Y

Drg.No. Z44990-450
Sh.3 Iss.3

AA1a: Input attenuator
AB8: Overload detecto

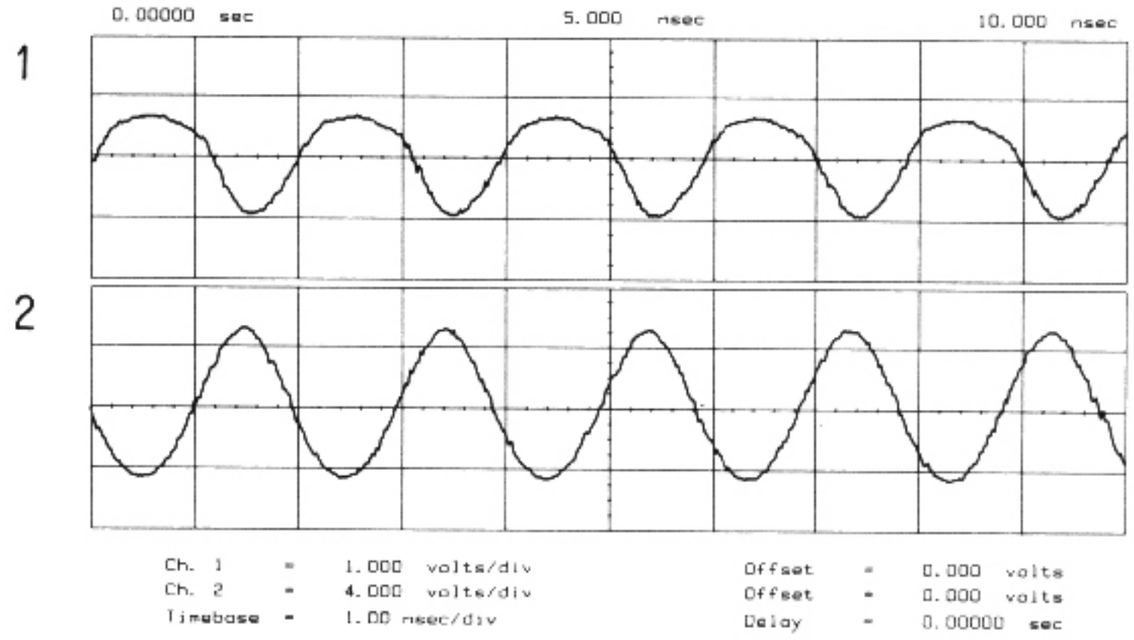


put attenuator assembly
rload detector

1
2

BOARD : AA2a

TEST POINT : pin 2 (input from AA7) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : L port of X1 for Ch. 2

PROCEDURE :

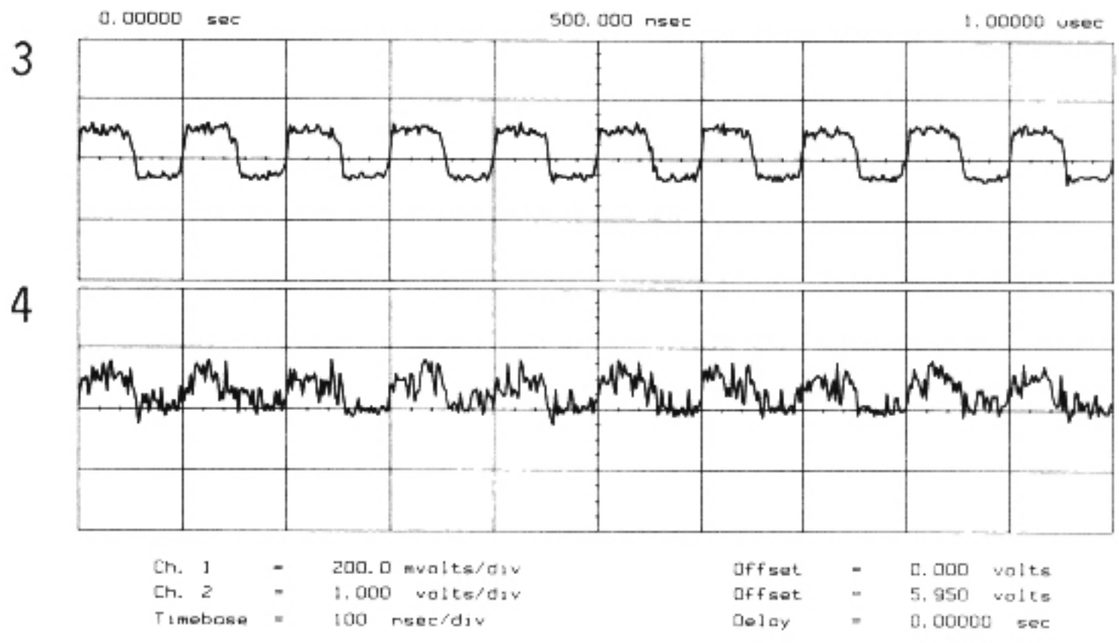
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter

3
4

BOARD : AA2a

TEST POINT : pin 1 (input from AA2) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP2 for Ch. 2

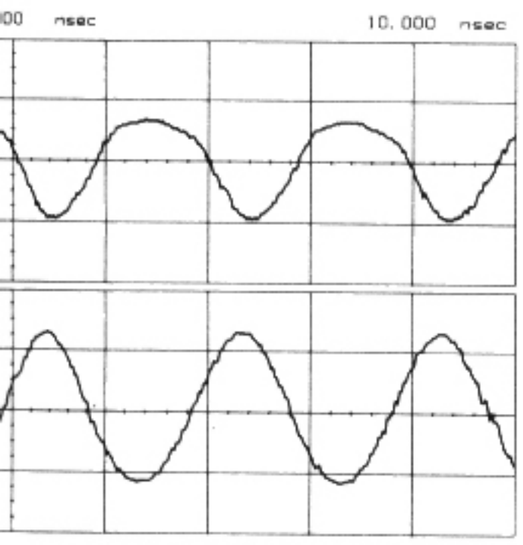
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter
Cal. signal in Ref. level	-10 dBm
Attenuation	0 dB

Waveforms for AA2a

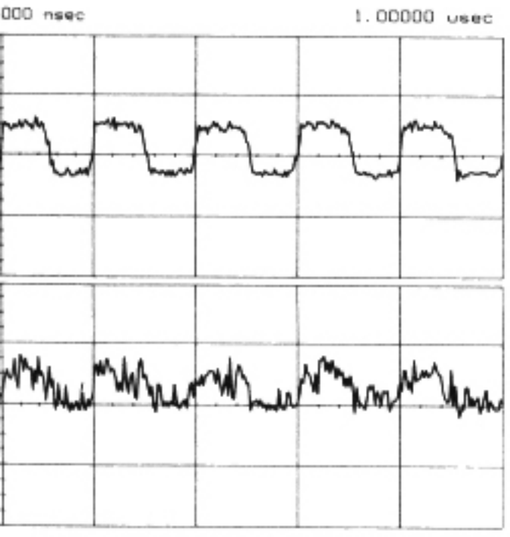
or Ch. 1



lowing 2382 settings:

z/DIV

or Ch. 1



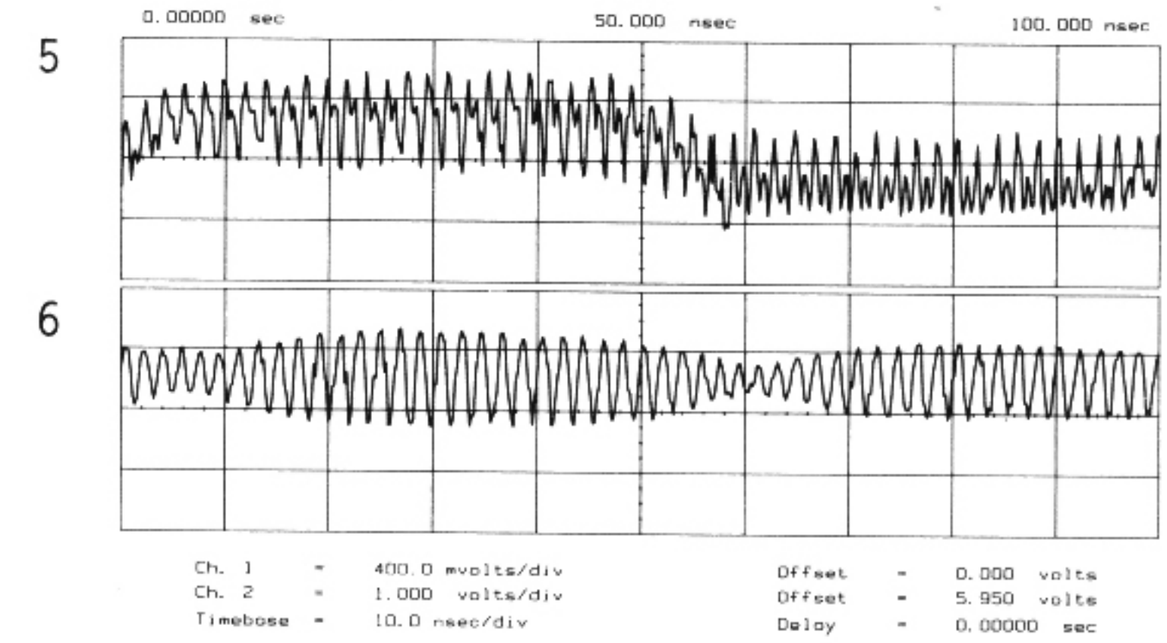
owing 2382 settings:

MHz
0 kHz/DIV
ter
0 dBm
dB

5
6

BOARD : AA2a

TEST POINT : X port of X1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : pin 3 (output to AA3)

PROCEDURE :

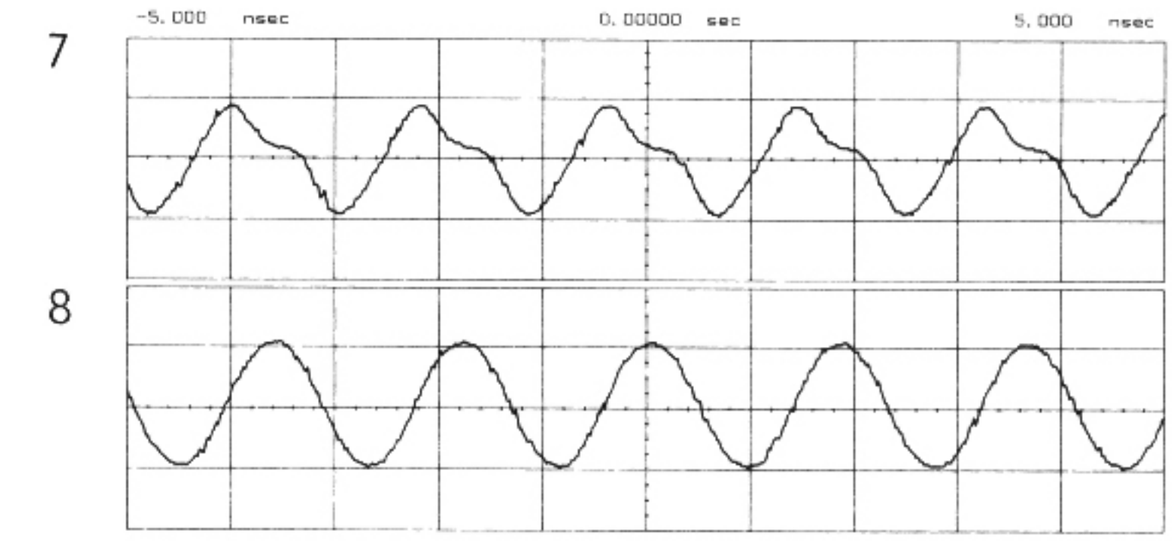
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Mode	meter
Cal. signal in Ref. level	-10 dBm
RF attenuation	0 dB

7
8

BOARD : AA3a

TEST POINT : input from AA9 for Ch. 1
SCOPE SETTING [DEFAULT]

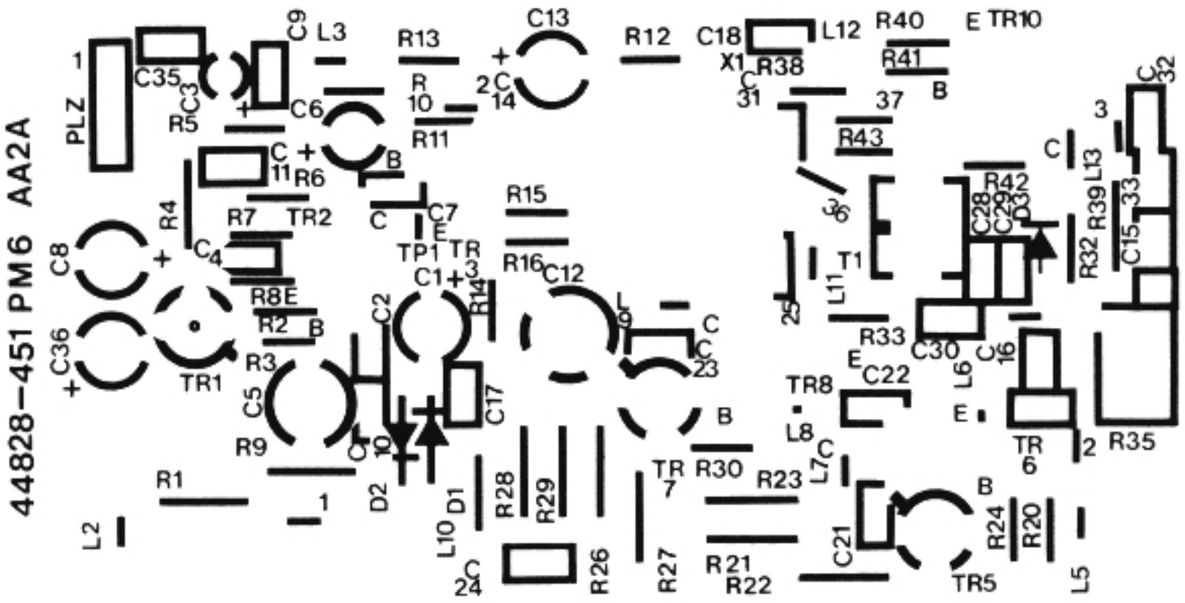


TEST POINT : junction R1/TR1 GATE 1

PROCEDURE :

1. Press PRESET.

Waveforms for AA2a

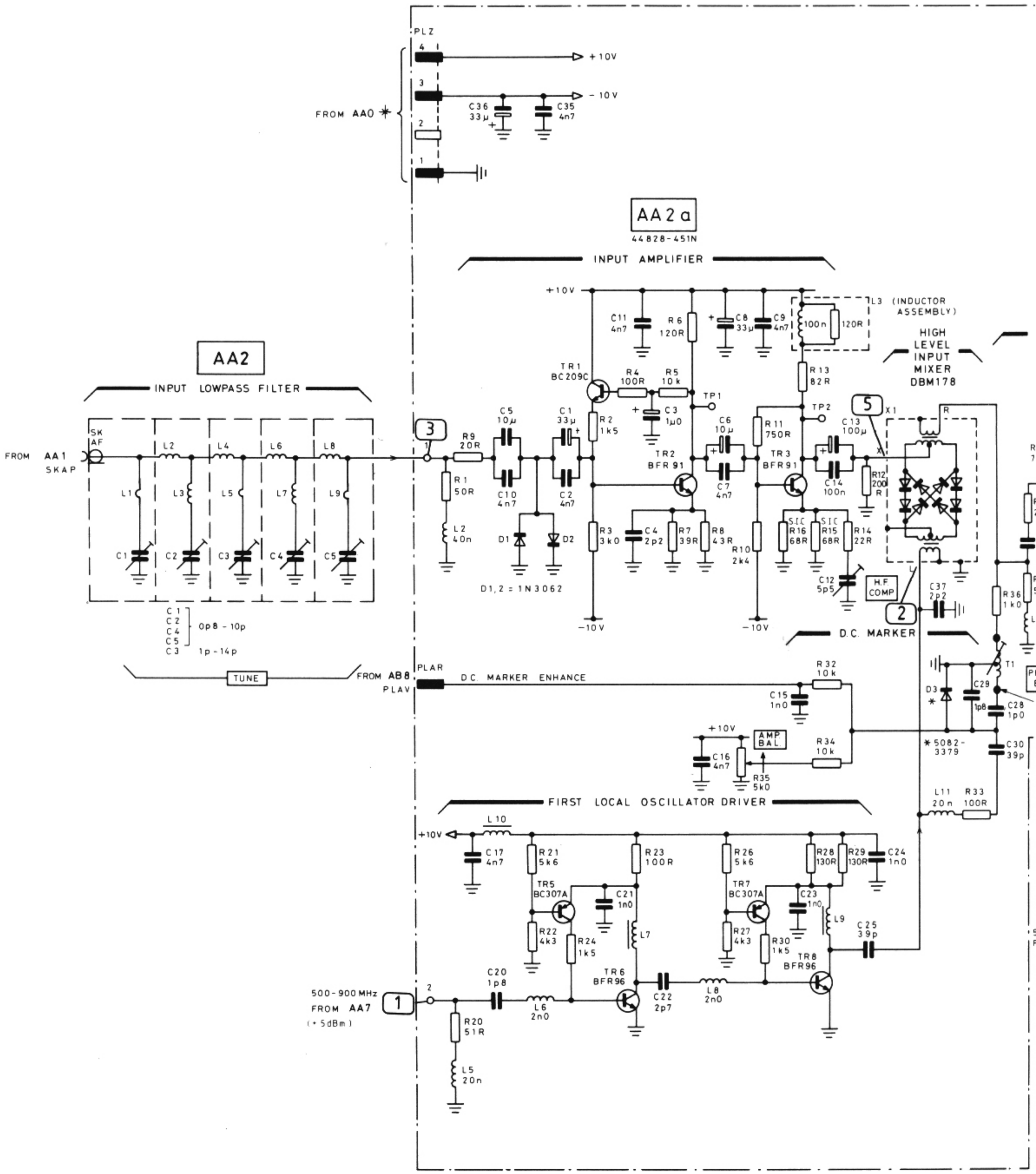


Component layout for AA2a

Component layout for AA3a

Fig. 5

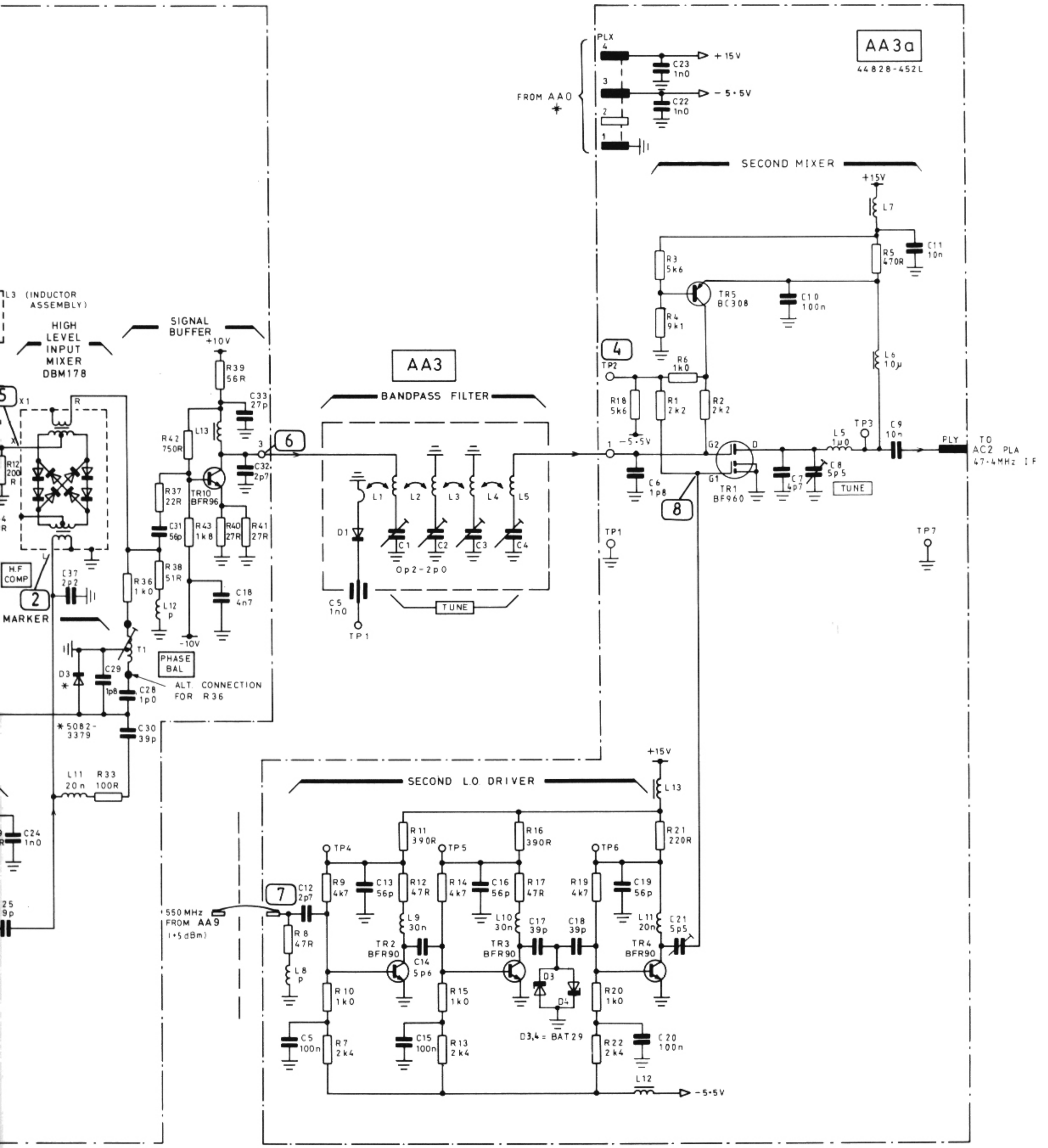
May 86



Drg.No. Z44990-450
Sh.4 Iss.9 & 1

✳ SEE CIRCUIT AA0 FOR

AA2a: Input fi
AA3a: 502.6MHz



* SEE CIRCUIT AA0 FOR CONNECTION DETAILS

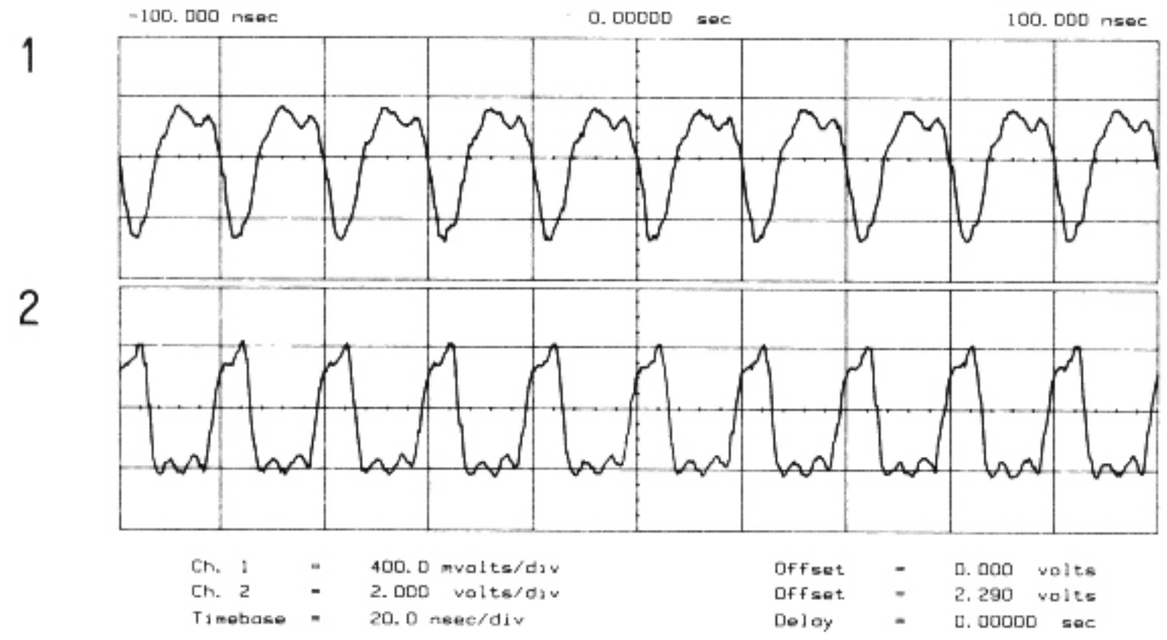
AA2a: Input filter & mixer
AA3a: 502.6MHz I.F. & second mixer

Fig. 5
Chap. 7
Page 15

1
2

BOARD : AA4

TEST POINT : PLAL for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP3 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 setting:

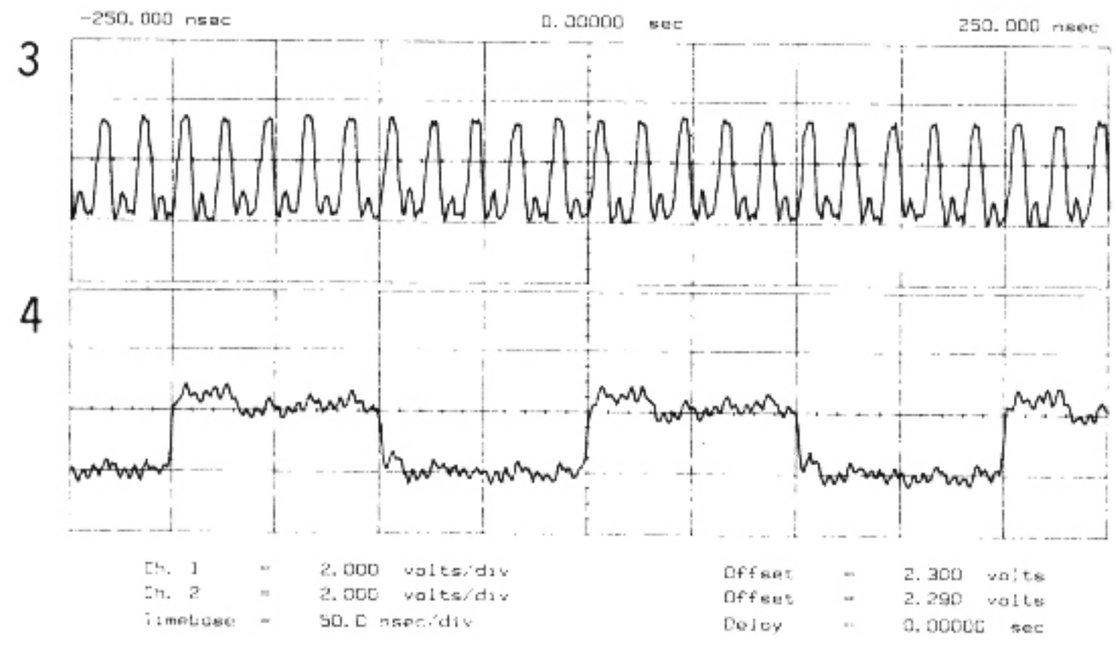
   Span 20 kHz/DIV or less

3
4

BOARD : AA4

TEST POINT : TP3 for Ch. 1

SCOPE SETTING [DEFAULT]



TEST POINT : IC3 pin 5 for Ch. 2

PROCEDURE :

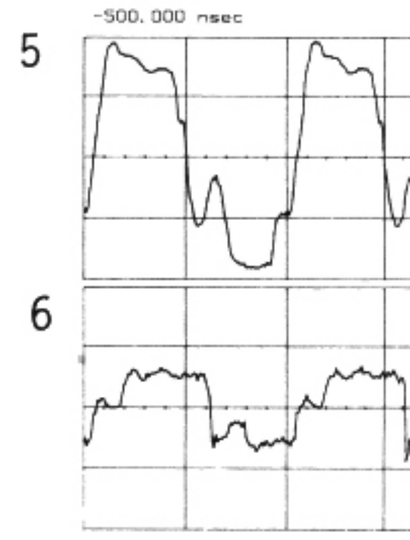
1. Press PRESET then select the following 2382 setting:

   Span 20 kHz/DIV or less

5
6

BOARD : AA4

TEST POINT : TP4 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : T2 pin 1 for Ch

PROCEDURE :

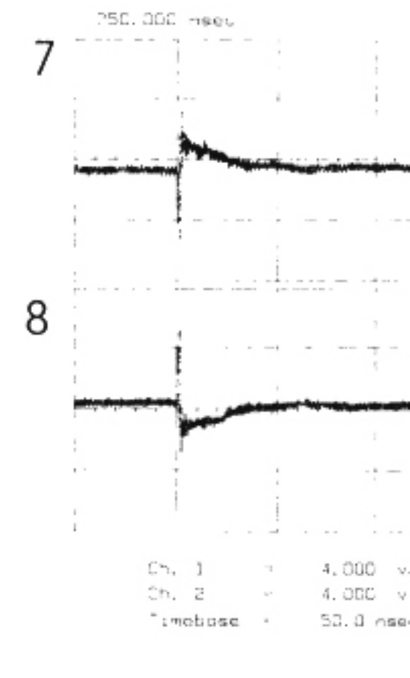
1. Press PRESET then selec

   Span 20 kHz/DI

7
8

BOARD : AA4

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]

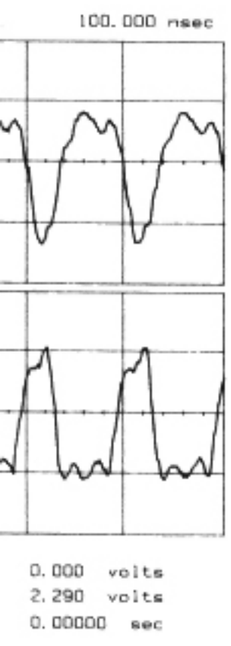


TEST POINT : TP6 for Ch. 2

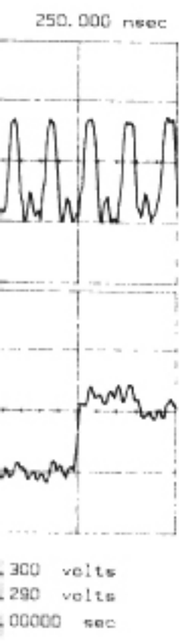
PROCEDURE :

1. Press PRESET then selec

   Span 20 kHz/DI



g:

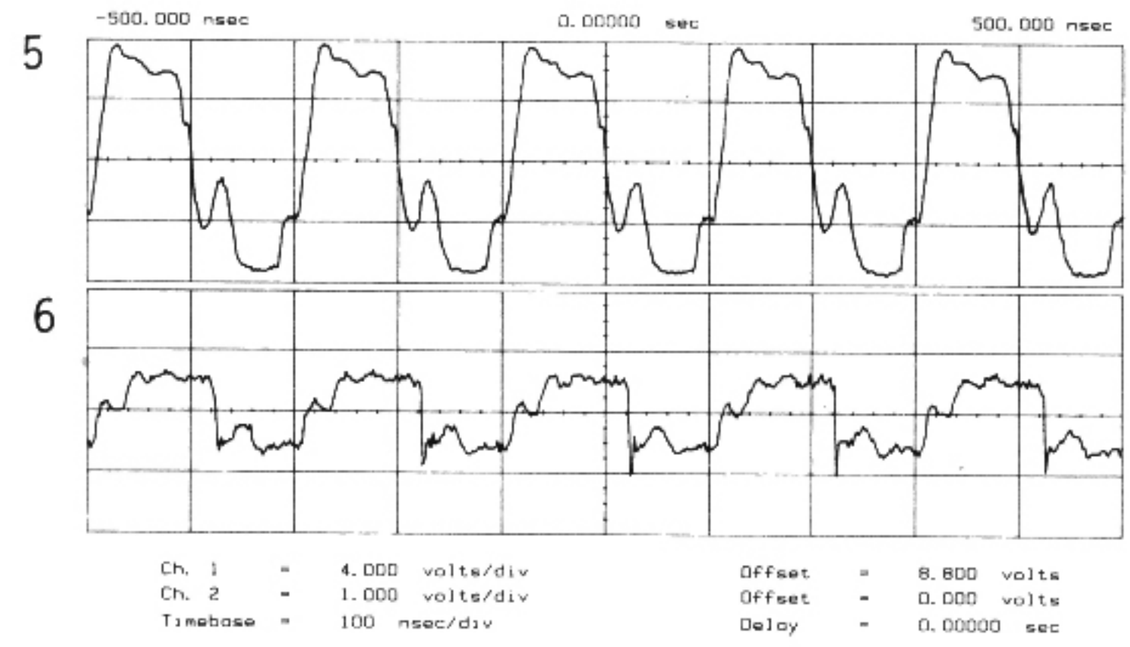


g:

5
6

BOARD : AA4

TEST POINT : TP4 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : T2 pin 1 for Ch. 2

PROCEDURE :

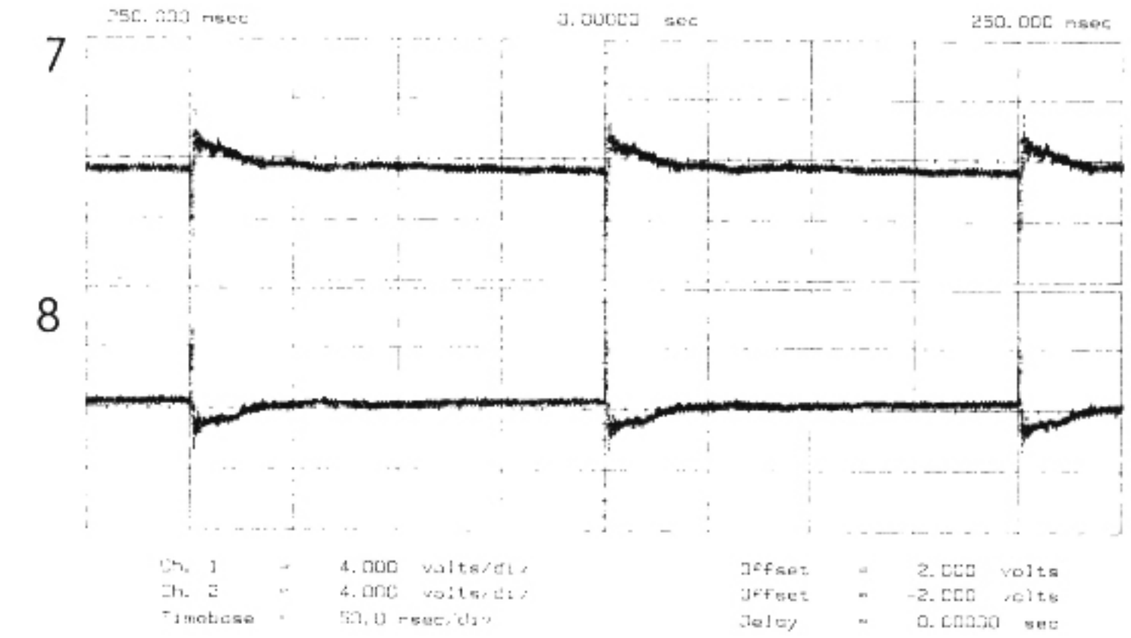
1. Press PRESET then select the following 2382 setting:

   Span 20 kHz/DIV or less

7
8

BOARD : AA4

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP6 for Ch. 2

PROCEDURE :

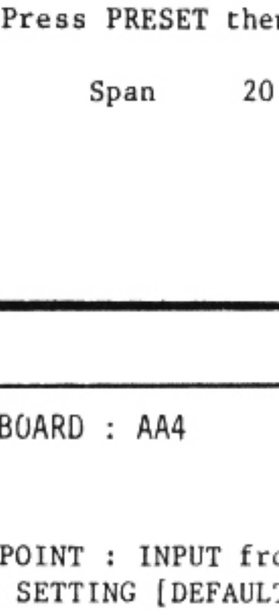
1. Press PRESET then select the following 2382 setting:

   Span 20 kHz/DIV or less

9
10

BOARD : AA4

TEST POINT : TP5 for
SCOPE SETTING [DEFAUL



TEST POINT : TP6 for

PROCEDURE :

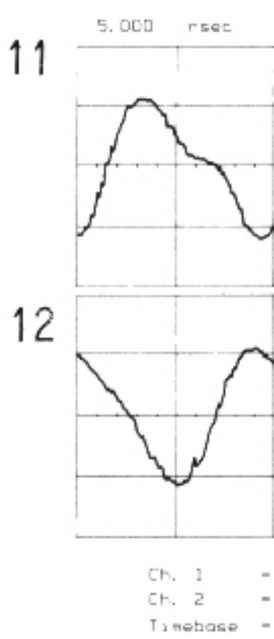
1. Press PRESET the

   Span 20

11
12

BOARD : AA4

TEST POINT : INPUT fr
SCOPE SETTING [DEFAUL

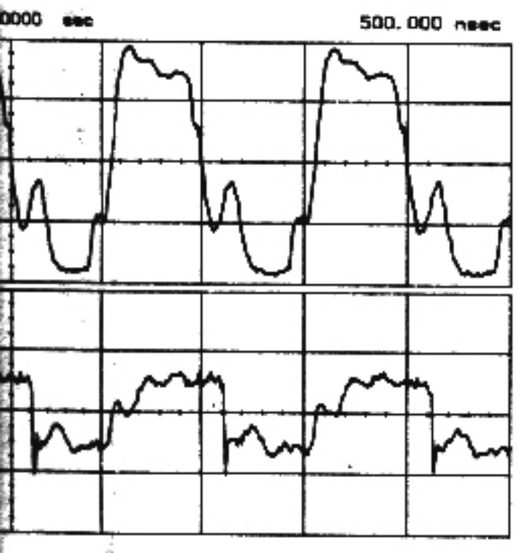


TEST POINT : junction

PROCEDURE :

1. Press PRESET the

   Span 20

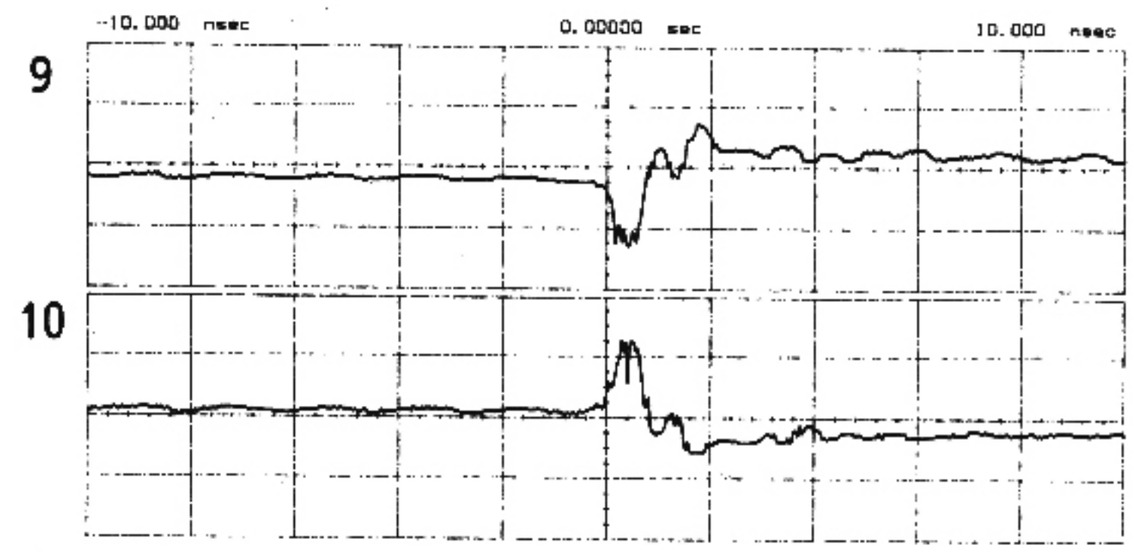


lowing 2382 setting:

9
10

BOARD : AA4

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]

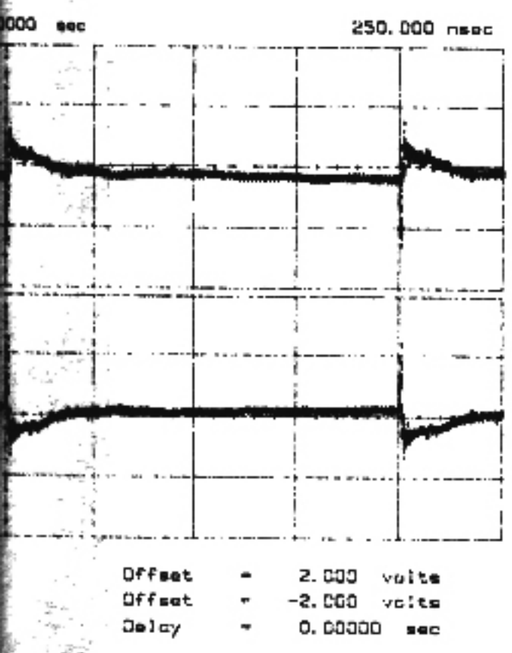


TEST POINT : TP6 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following setting:

   Span 20 kHz/DIV or less

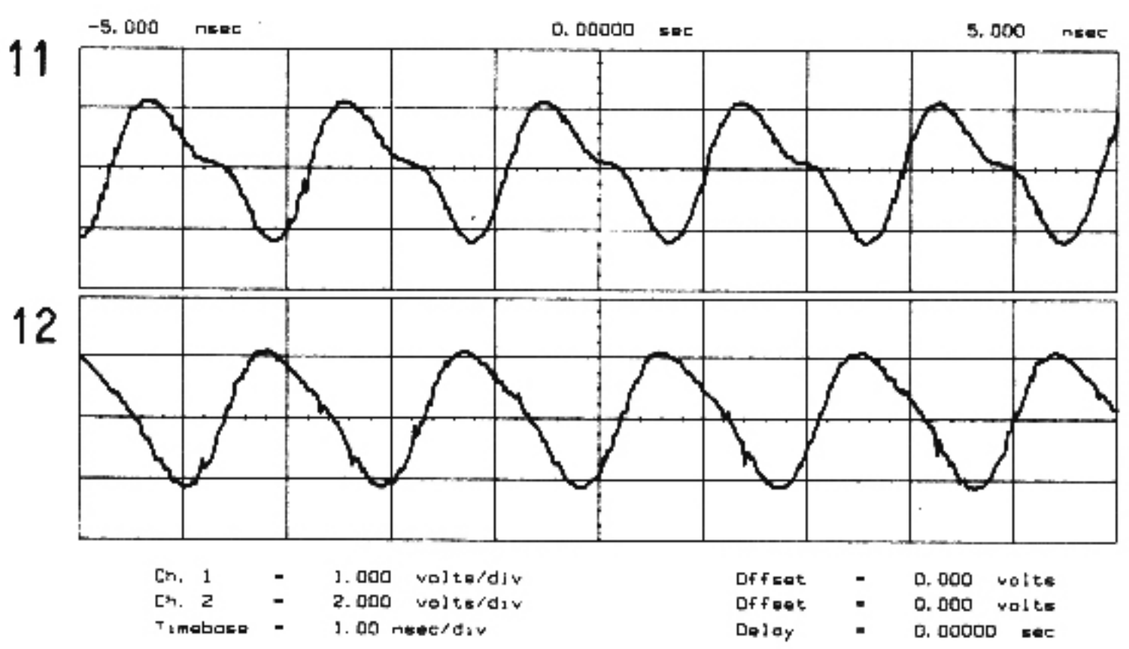


lowing 2382 setting:

11
12

BOARD : AA4

TEST POINT : INPUT from AA5 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : junction C11/L5 (input to sampling gate) for Ch. 2

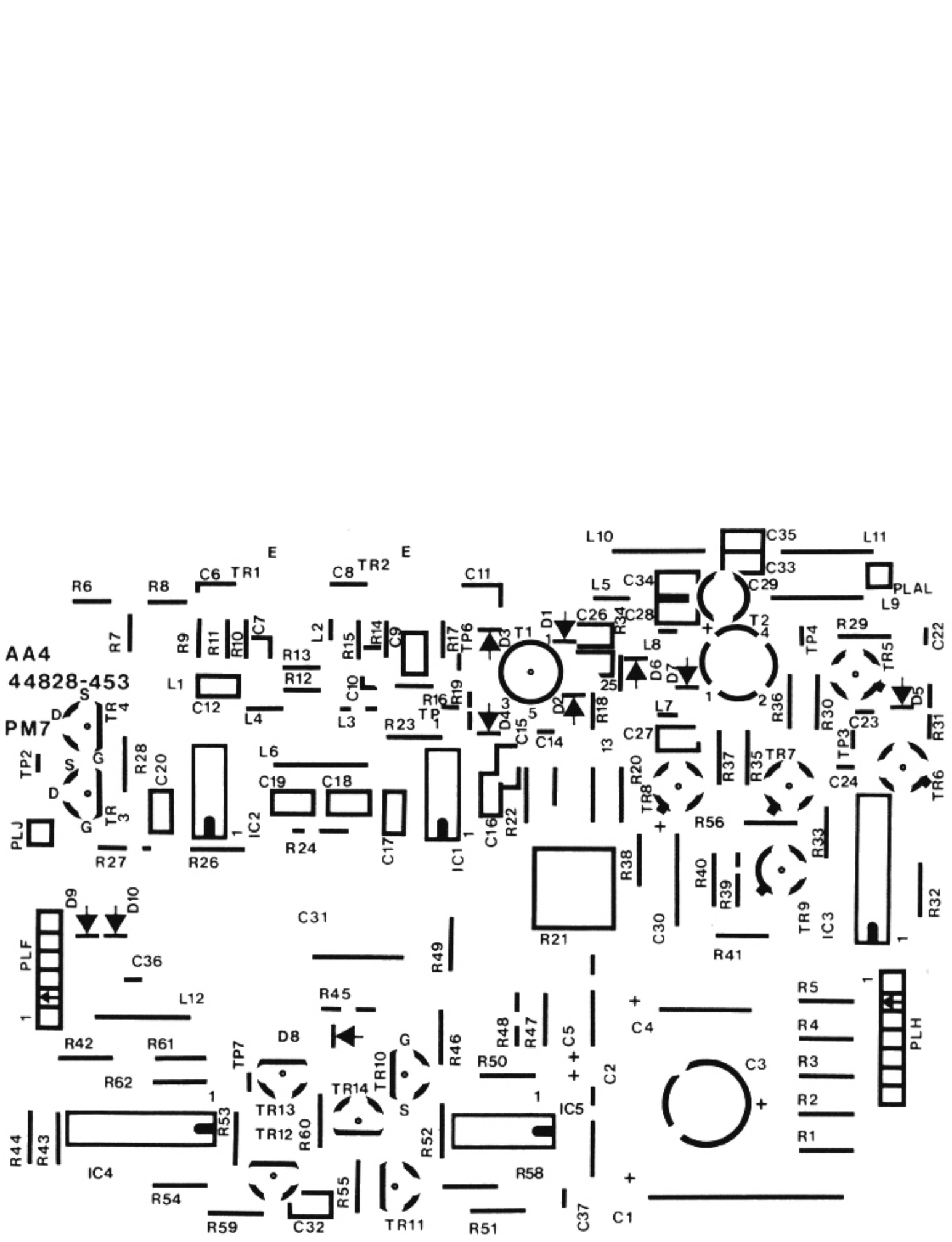
PROCEDURE :

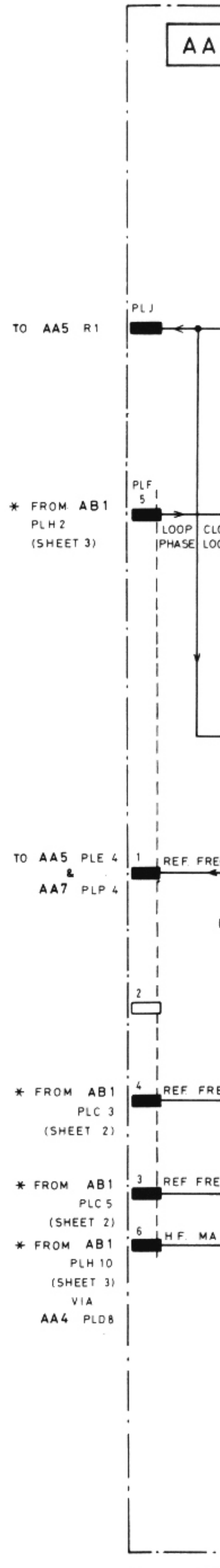
1. Press PRESET then select the following 2382 setting:

   Span 20 kHz/DIV or less

Fig. 6a

May 86





Component layout for AA4

Fig. 6

May 86

AA4 44828 453J

+14·5V

SAMPLING GATE

SAMPLE STRETCHER

X2 AMP

LOWPASS FILTER

IC1 NE5534A

IC2 NE5534A

LOOP SWITCH

TP5

R18 1k0

C13 10n

R20 10k

D2 D1 MBD102 D4 D3

TP2

PLJ

TO AA5 R1

TR4 TIS74

TR3 TIS74

C20 47p

+14·5Vd

L6 680µ

R23 1k0

TP1

C17 47p

C16 56p

C15 5p6

R21 10k

BAL.

R22 10k

C14 10n

R19 1k0

TP6

8

10

T1

3

2

R24 1k0

C19 330p

C18 330p

-14·5Vd

R27 1M0

R26 3k3

+4·8V

R43 27k

IC4(a) µA339

R62 10k

D10

R42 1k0

PLF 5

* FROM AB1 PLH 2 (SHEET 3)

LOOP CLOSED / PHASE LOCKED (L)

C36 10n

R28 1M0

R61 10k

D9

IC4(b) µA339

R44 12k

HIGH GAIN / LOW FREQ. RESPONSE AMP.

+7·0Vd

TR13 BC499

R52 75R

TP7

TO AA5 PLE 4 & AA7 PLP 4

1 REF. FREQ. OUT

L12 1µ0

R60 4k7

R53 22k

C32 1n0

TR12 BC499

TR11 BC499

TR14 BC499

R55 5k1

R54 5k6

R59 2k0

R51 9k1

R58 2k0

IC5(b) TL072

C37 1n0

R46 2k0

R50 270k

C31 1µ0

IC5(a) TL072

R49 1k0

R47 100k

R48 1k0

-14·5Vd.

2

REF. FREQ. ENABLE SWITCH

* FROM AB1 PLC 3 (SHEET 2)

4 REF FREQ IN

TR10 TIS74

R45 1M0

D8 1N4148

* FROM AB1 PLC 5 (SHEET 2)

3 REF FREQ. ENABLE

* FROM AB1 PLH 10 (SHEET 3)

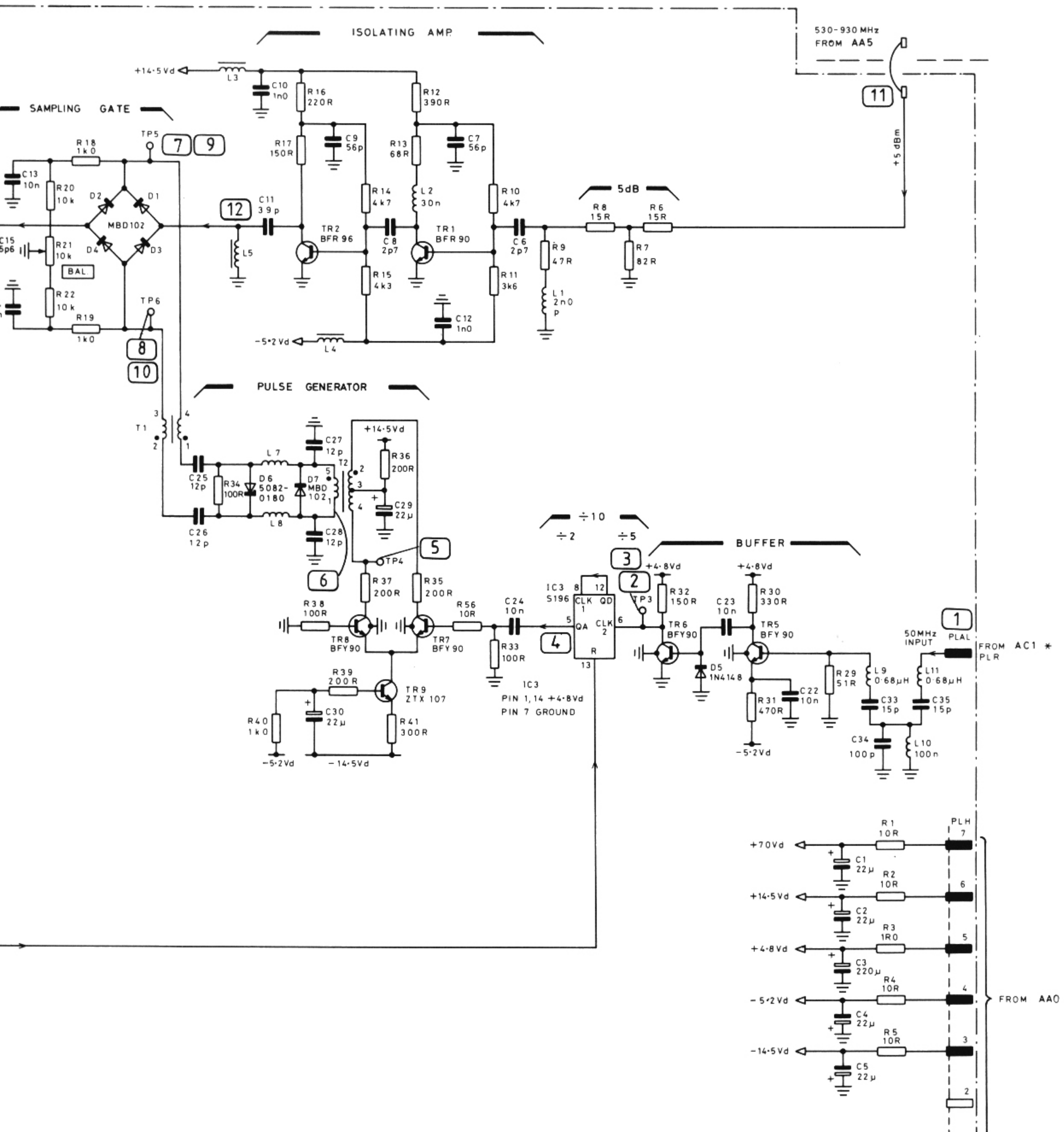
6 H.F. MASTER SG. DRIVE ON (H)

VIA AA4 PLD8

Drg. No. Z44828-453J
Sh. 1 Iss. 4

* SEE CIRCUIT AA0 FOR CONN

AA4 : Sampling ga



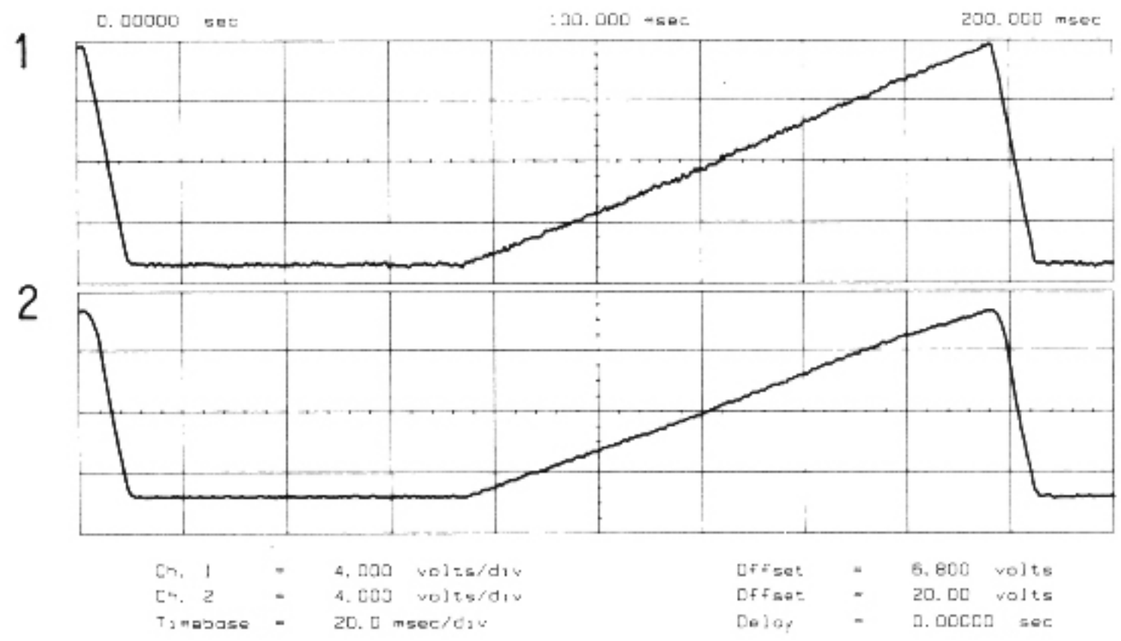
SEE CIRCUIT AA0 FOR CONNECTION DETAILS

AA4 : Sampling gate

1
2

BOARD : AA5

TEST POINT : PLE pin 3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP1 for Ch. 2

PROCEDURE :

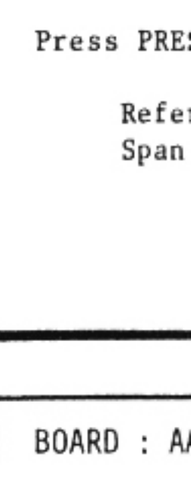
1. Press PRESET then select the following 2382 setting:

   Span 10 MHz/DIV

3
4

BOARD : AA

TEST POINT : ju
SCOPE SETTING



TEST POINT : ou

PROCEDURE :

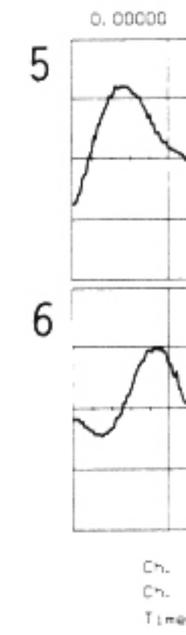
1. Press PRE

   Refe
   Span

5
6

BOARD : AA

TEST POINT : ou
SCOPE SETTING



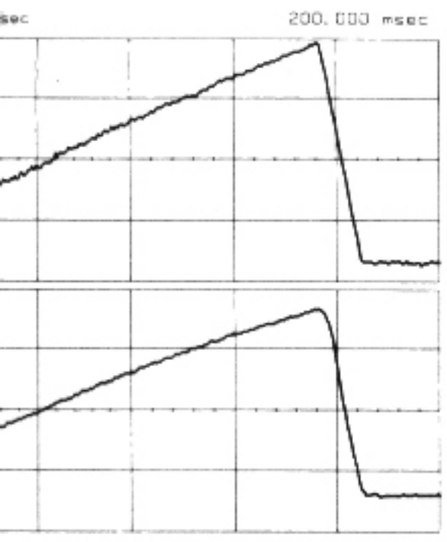
TEST POINT : ou

PROCEDURE :

1. Press PRE

   Refe
   Span

Waveforms for AA5

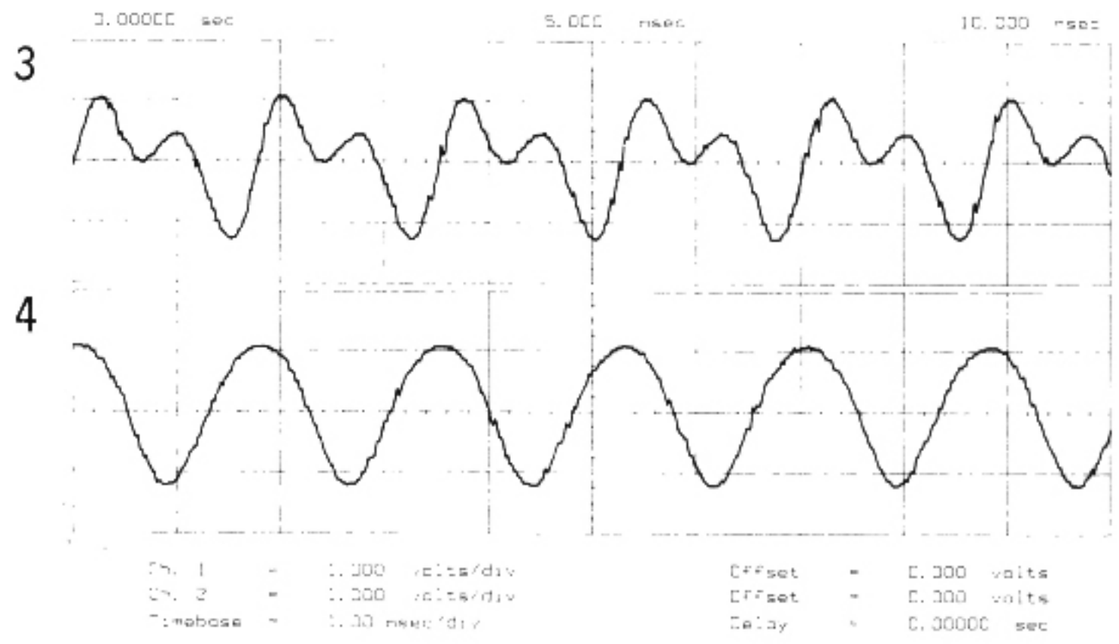


ing 2382 setting:

3
4

BOARD : AA5

TEST POINT : junction C18/T1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : output to AA4 for Ch. 2

PROCEDURE :

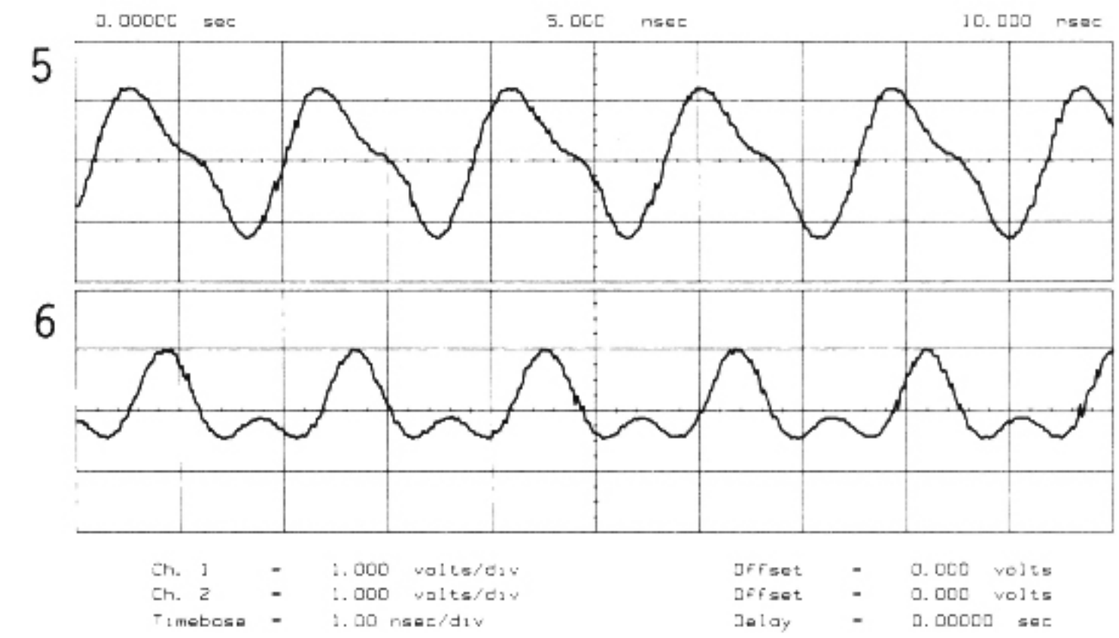
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV

5
6

BOARD : AA5

TEST POINT : output to AA6 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : output to AA8 for Ch. 2

PROCEDURE :

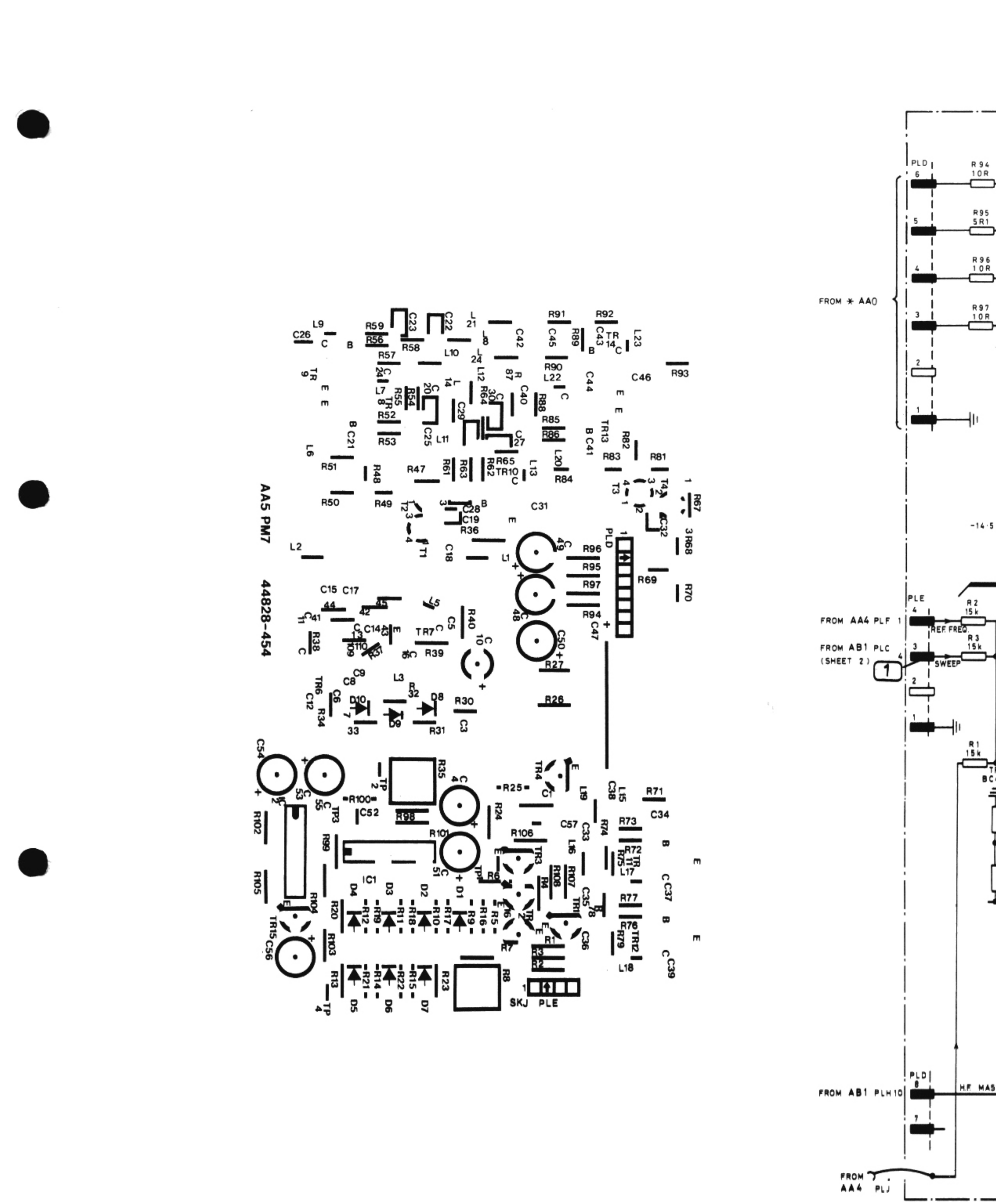
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV

Waveforms for AA5

Fig. 7a

May 86



Component layout for AA5

Fig. 7

May 86

AA5

44828-454F

FROM * AA0

PLD

REGULATOR

+70Vd — R94 10R — C47 22µ

+14·5Vd — R95 5R1 — C48 22µ

−5·2Vd — R96 10R — C49 22µ

−14·5Vd — R97 10R — C50 22µ

IC1 µA723: +14·5Vd; R100 4k7; R98 3k0; R101 12k; C51 10µ; C52 100p; R99 10R; TP3; C53 22µ; +10V

REGULATOR

IC2 µA723: R102 3k0; R104 2k2; R103 2k0; C54 10µ; R105 4k7; TP4; C55 100p; C56 22µ; TR15 BC 307A; −14·5Vd; −10V

SUMMER AND SHAPER

PLE

FROM AA4 PLF 1 — REF FREQ — R2 15k

FROM AB1 PLC (SHEET 2) — SWEEP — R3 15k

R106 12k; R5 75k; TR3 BC449; C57 1n0; TR1 BC449; TR2 BC449; R1 15k; R6 10k; R7 15k; R8 10k; SET HIGH FREQ.; R107 6k2; TR16 BC237A; R108 3k6; R4 2k0; −10V

+70Vd; R16 20k; FILTERS; TP1; R24 10k; R30 1k0; R25 62R; C1 470n; TR4 BC449

R9 2k0 D1; R10 7k5 D2; R11 18k D3; R12 27k D4; R13 39k D5; R14 43k D6; R15 68k D7; D1-D7 IN4148

R17 330R; R18 510R; R19 4k7; R20 200R; R21 220R; R22 100R; R23 100R

SET LOW FREQ.; TP2; R35 2k0; C4 10µ; R36 10k; R34 1k0; C7 1n0

530-930MHz CLAPP VCO

OUTPUT BUFFER

+10V — L2

PRESET FREQ.; L3; C6 1n0; R33 100k; D10; R32 100k; D9; R31 100k; D8; C3 1n0

C9 2p2; R37 1k0; R109 10R; TR6 BFR90; R38 220R; C11 1n0; C12 1n0

C8 3p9; C STRAYS

C13 1p8; R41 68R; C14 2p7; L4; R39 910R; R40 110R; C10 10µ

C15 1n0; C17 56p; R42 3k3; L5 30n; R44 390R; R45 68R; TR7 BFR90; R43 6k2

C18 39p; T1

L1 — −10V; C5 1n0; C16 1n0

FROM AB1 PLH 10 — H.F. MASTER SIG. DRIVE ON (H) — R27 9k1 — R26 2k0

FROM AA4 PLJ

* SEE CIRCUIT AA0 FOR CONNECTION DETAILS.

AA5
44828-454F

OUTPUT BUFFER

C15 1n0
R44 390 R
C17 56p
R45 68R
R42 3k3
L5 30n
C14 2p7
TR7 BFR90
R43 6k2
C18 39p
3
POWER SPLITTER
T1
T2
C19 3p9
R47 120R

ISOLATING AMP
L8
+14 5Vd
R54 470R
C22 1n0
R58 270R
C20 56p
R55 47R
C23 56p
R59 47R
R52 4k7
L7 30n
R56 4k7
L9 30n
12dB
R49 30R
R48 30R
C21 2p7
TR8 BFR90
C24 2p7
TR9 BFR90
C26 39p
6
AA8
530-930MHz
(-5 dBm)
R50 27R
R51 47R
L6 p
R53 3k3
R57 3k6
C25 1n0
L10
-5·2Vd

ISOLATING AMP
L16
+14·5Vd
R74 330R
C35 1n0
R78 200R
C33 56p
R75 47R
C36 56p
R79 47R
R72 4k7
L17 30n
R76 4k7
L18 30n
TR11 BFR90
C37 2p7
TR12 BFR90
C39 39p
5
AA4
530-930MHz
(+5dBm)
R68 10R
R70 10R
C34 2p7
R69 150R
R71 47R
L15 p
R73 3k3
R77 3k6
C38 1n0
L19
-5·2Vd

BUFFER AMP.
L12
+14·5Vd
C30 1n0
R64 270R
C27 56p
R65 47R
L13 30n
C28 5p6
R62 4k7
TR10 BFR90
C31 39p
T3
T4
R67 120R
R61 47R
L11 p
R63 3k3
C32 3p9
C29 1n0
L14
-5·2Vd

ISOLATING AMP
L21
+14·5Vd
R87 330R
C42 1n0
R91 200R
C40 56p
R88 47R
C43 56p
R92 47R
3dB
R81 10R
R83 10R
C41 2p7
R85 4k7
L22 30n
R89 4k7
L23 30n
TR13 BFR90
C44 2p7
TR14 BFR90
C46 39p
R93 120R
R82 150R
R84 47R
L20 p
R86 3k3
R90 3k6
C45 1n0
L24
-5·2Vd
4
AA6
530-930MHz
(+5dBm)

AA5

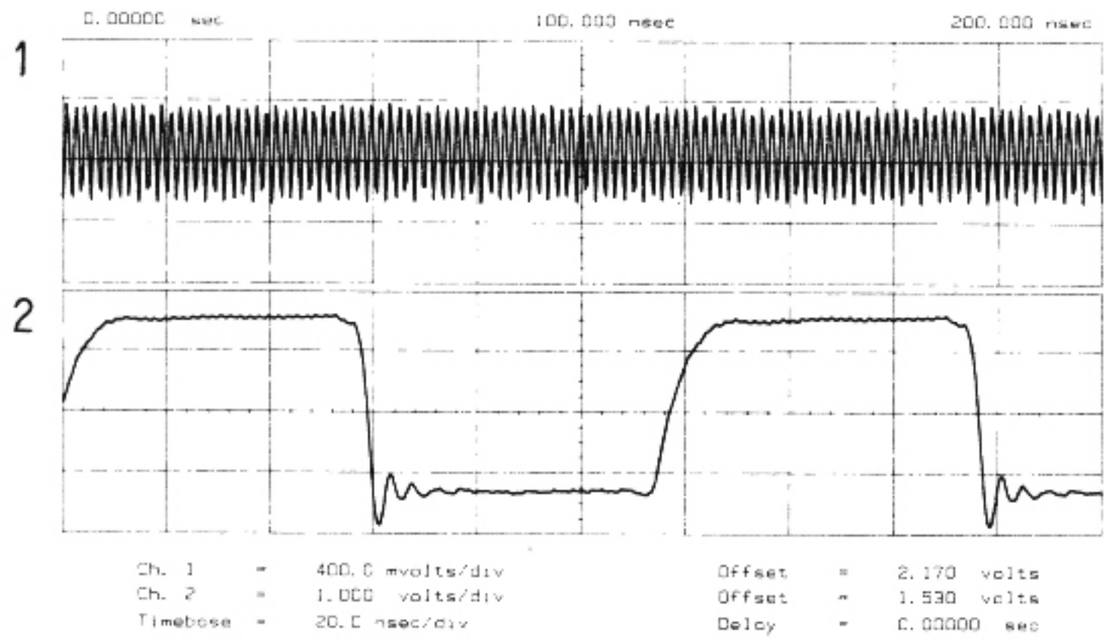
LS.

AA5 : Master VCO

1
2

BOARD : AA6

TEST POINT : IC1 pin 10 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP1 for Ch. 2

PROCEDURE :

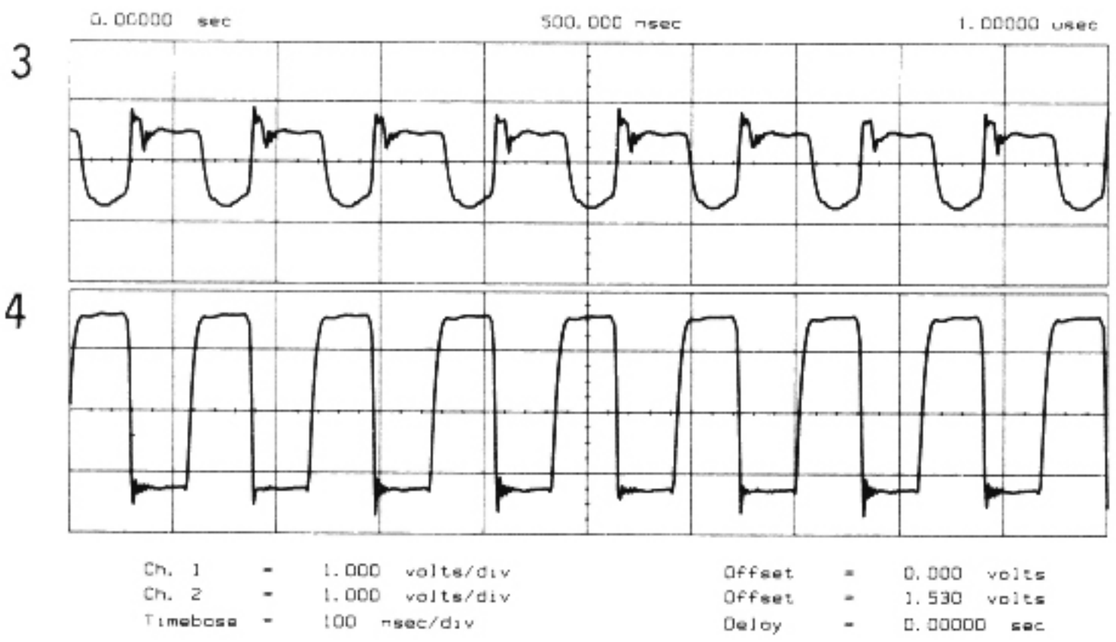
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV

3
4

BOARD : AA6

TEST POINT : PLAK for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP1 for Ch. 2

PROCEDURE :

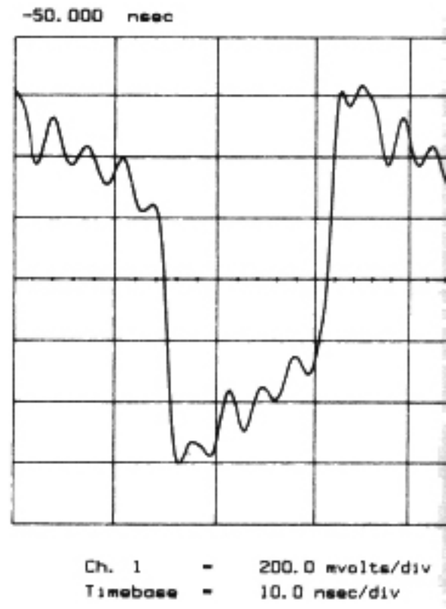
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV

5

BOARD : AB2

TEST POINT : TP2
SCOPE SETTING [DEFAULT]



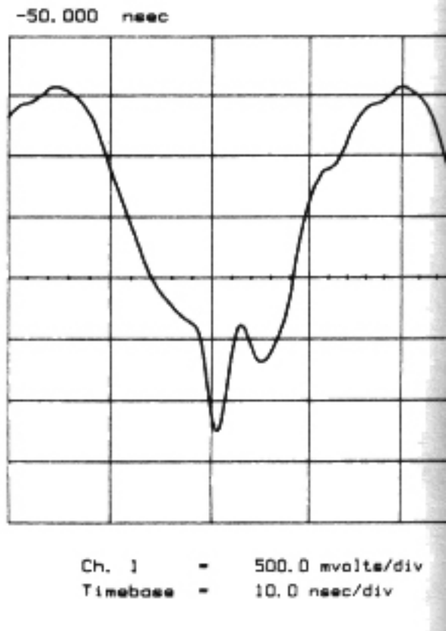
PROCEDURE :

1. Press PRESET.

6

BOARD : AB2

TEST POINT : TP3
SCOPE SETTING [DEFAULT]

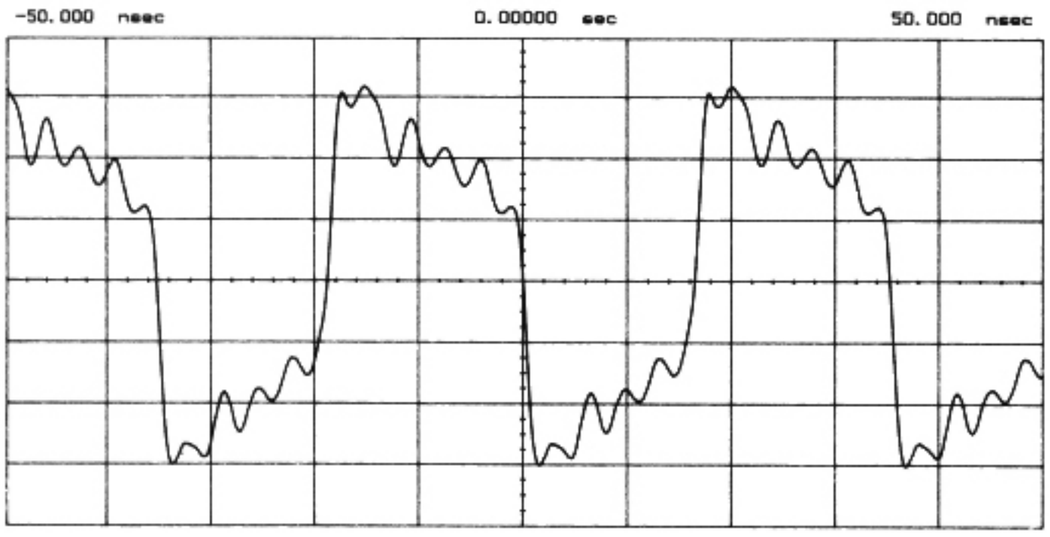


PROCEDURE :

1. Press PRESET.

5 BOARD : AB2

TEST POINT : TP2
SCOPE SETTING [DEFAULT]

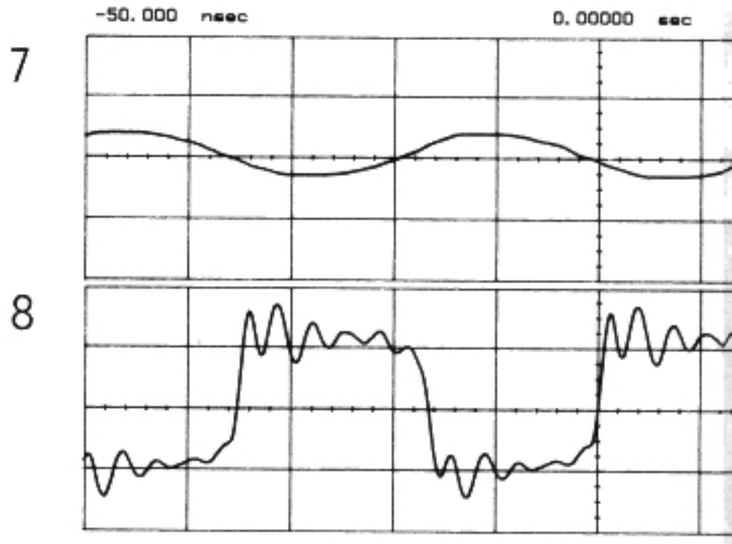


PROCEDURE :

1. Press PRESET.

7
8 BOARD : AB2

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



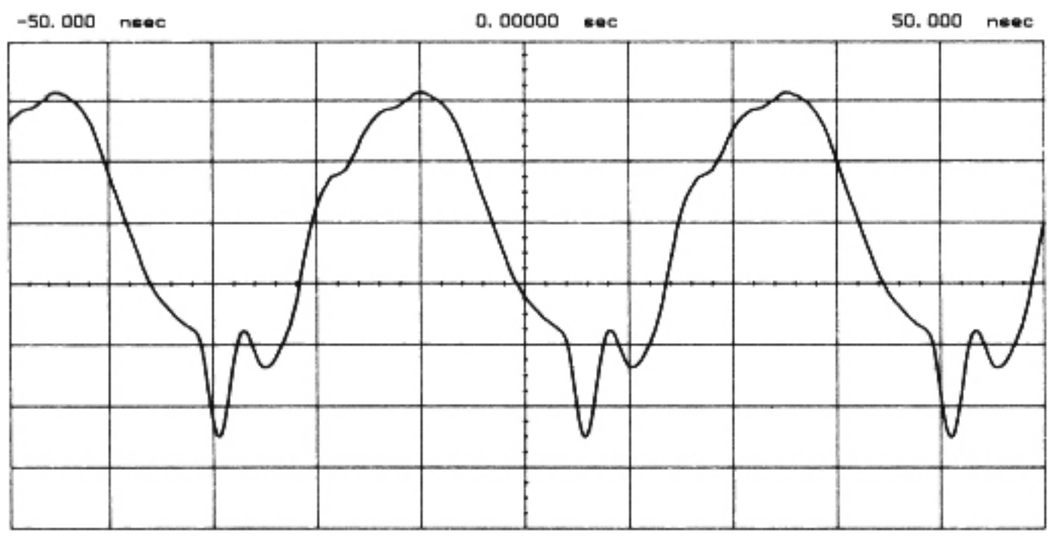
TEST POINT : TP2 for Ch. 2

PROCEDURE :

1. Press PRESET.

6 BOARD : AB2

TEST POINT : TP3
SCOPE SETTING [DEFAULT]

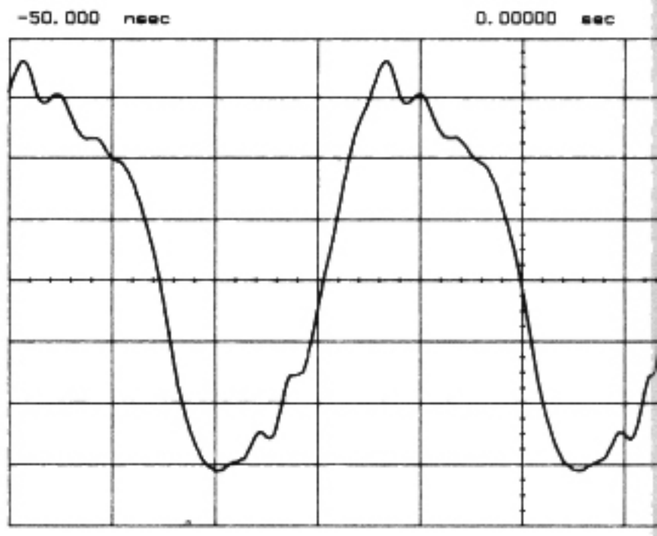


PROCEDURE :

1. Press PRESET.

9 BOARD : AB2

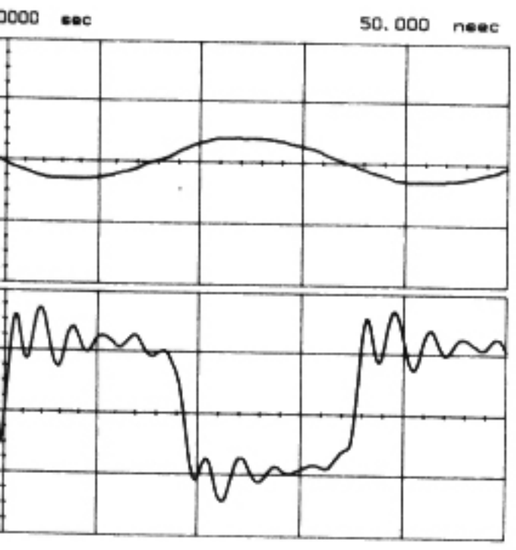
TEST POINT : TP5
SCOPE SETTING [DEFAULT]



PROCEDURE :

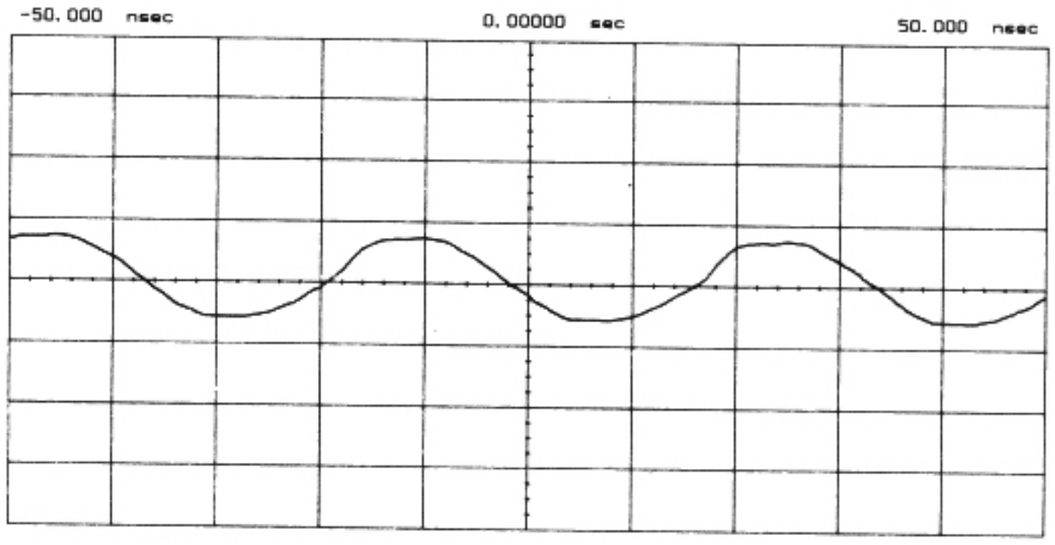
1. Press PRESET.

Waveforms for AA6, AB2 and AB7



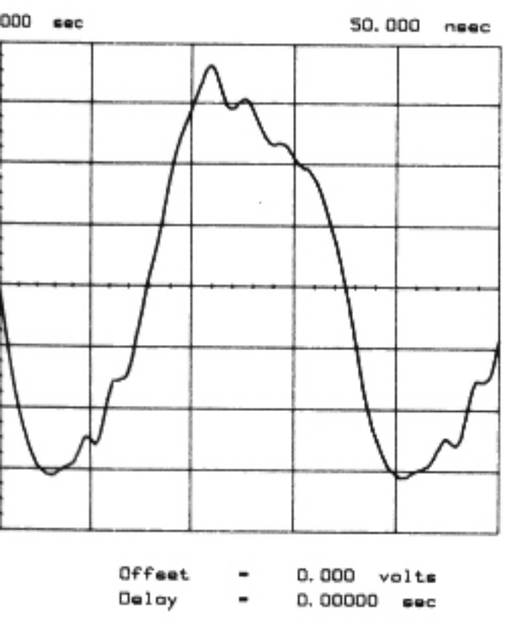
10 BOARD : AB2

TEST POINT : TP1
SCOPE SETTING [DEFAULT]



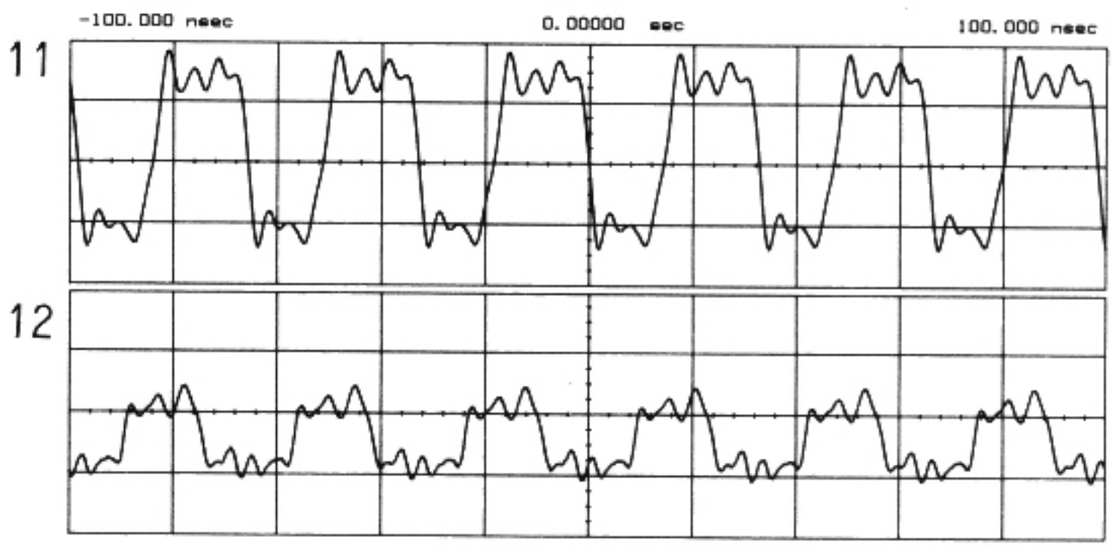
PROCEDURE :

1. Press PRESET.



11
12 BOARD : AB7

TEST POINT : TP3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP4 for Ch. 2

PROCEDURE :

1. Press PRESET. Ground AB7 C12.

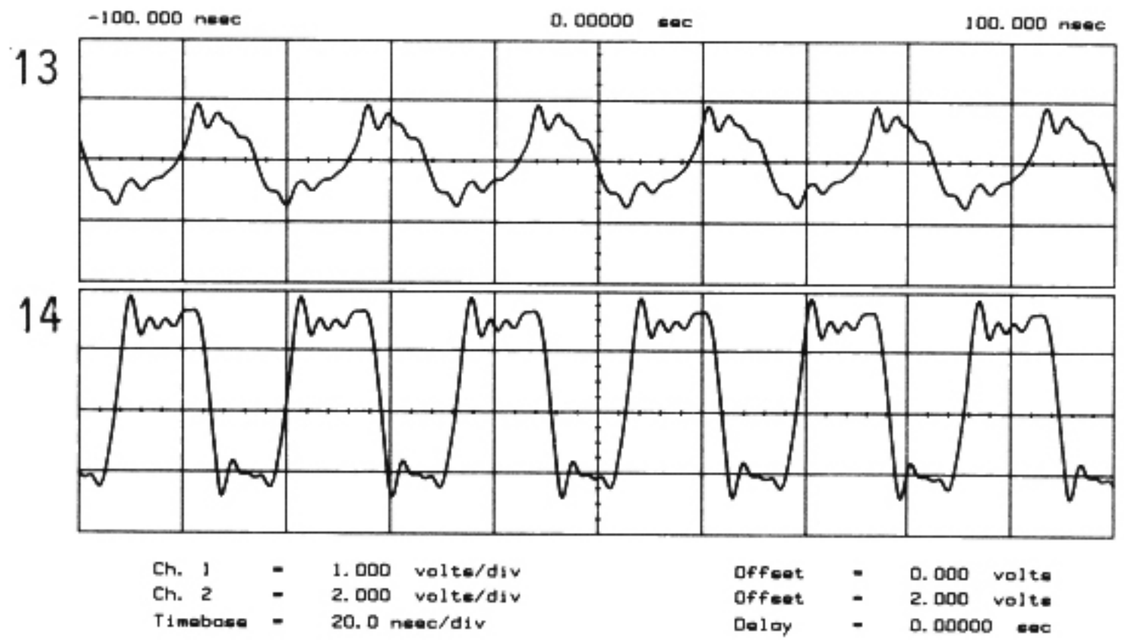
Fig. 8a

May 86

13 BOARD : AB7

14

TEST POINT : R12 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP3 for Ch. 2

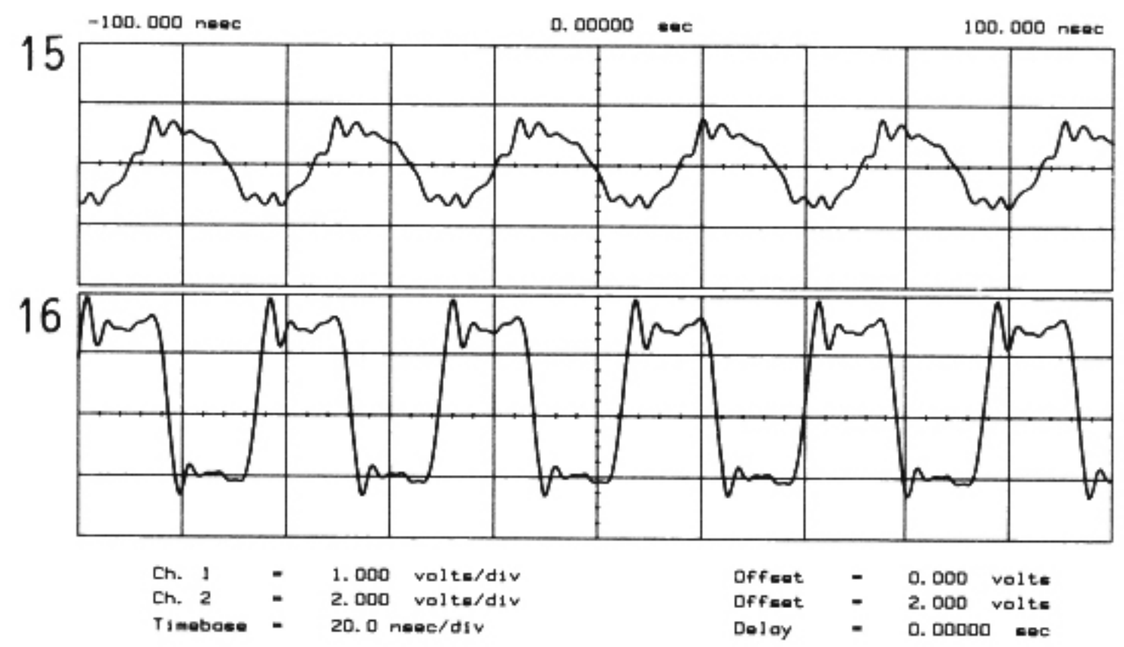
PROCEDURE :

1. Press PRESET.

15 BOARD : AB7

16

TEST POINT : R8 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP2 for Ch. 2

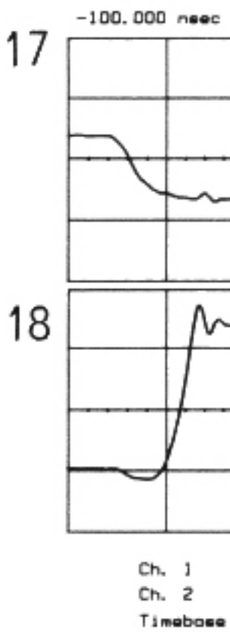
PROCEDURE :

1. Press PRESET.

BOARD : AB7

18

TEST POINT : R4 for C
SCOPE SETTING [DEFAUL

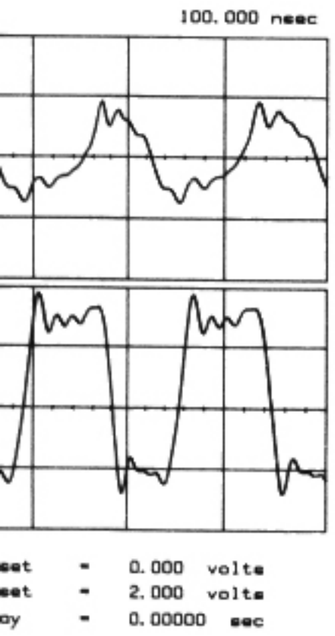


TEST POINT : TP1 for

PROCEDURE :

1. Press PRESET the

Span 20



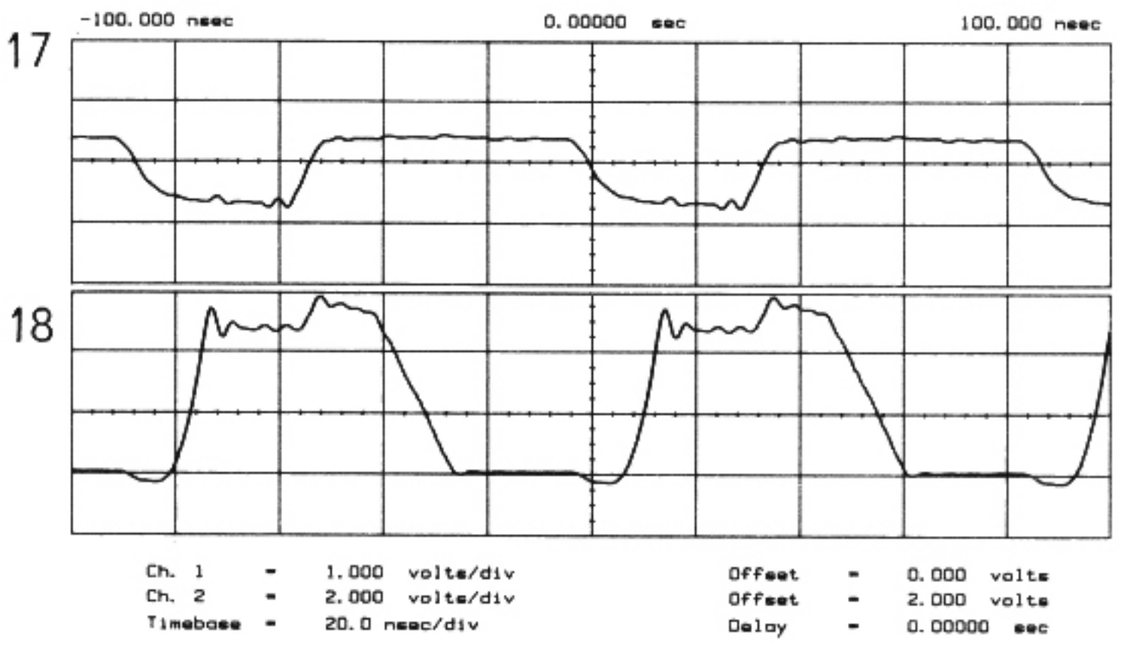
BOARD : AB7

18

TEST POINT : R4 for Ch. 1
SCOPE SETTING [DEFAULT]

17

18



TEST POINT : TP1 for Ch. 2

PROCEDURE :

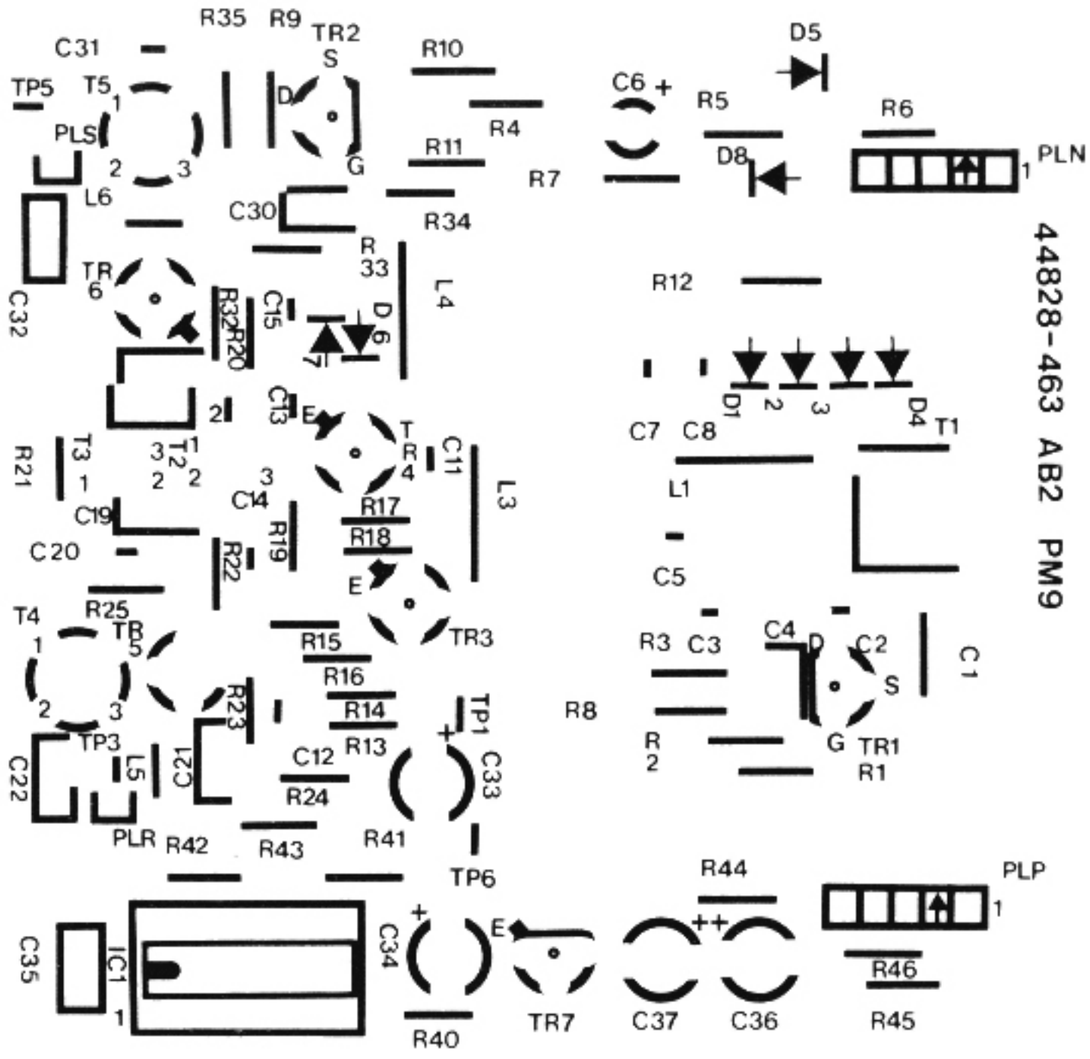
1. Press PRESET then select the following 2382 setting:

   Span 200 kHz/DIV

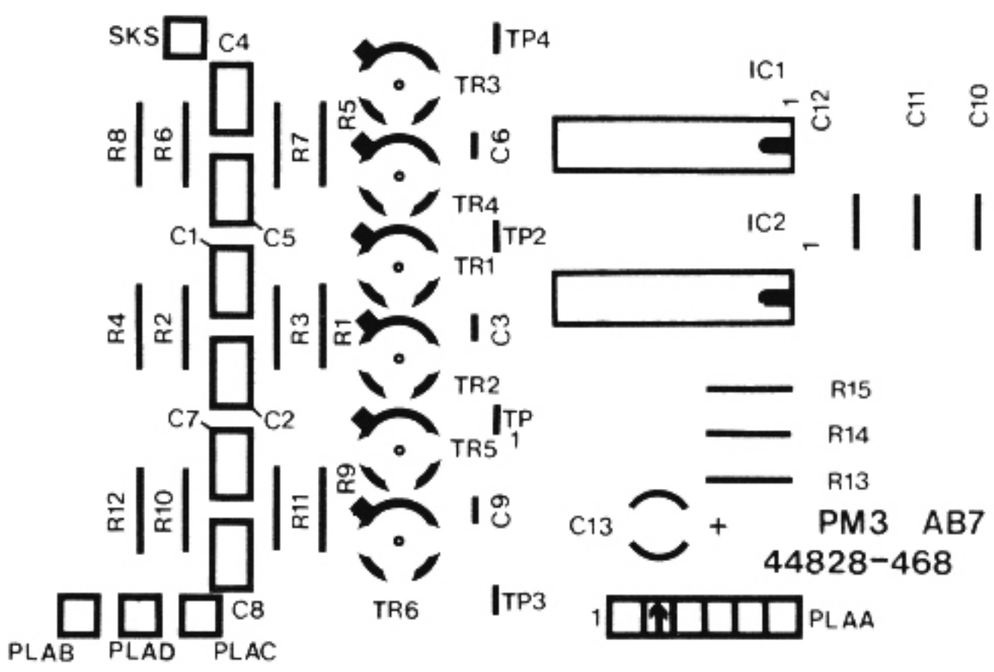
Waveforms for AA6, AB2 and AB7

Fig. 8b

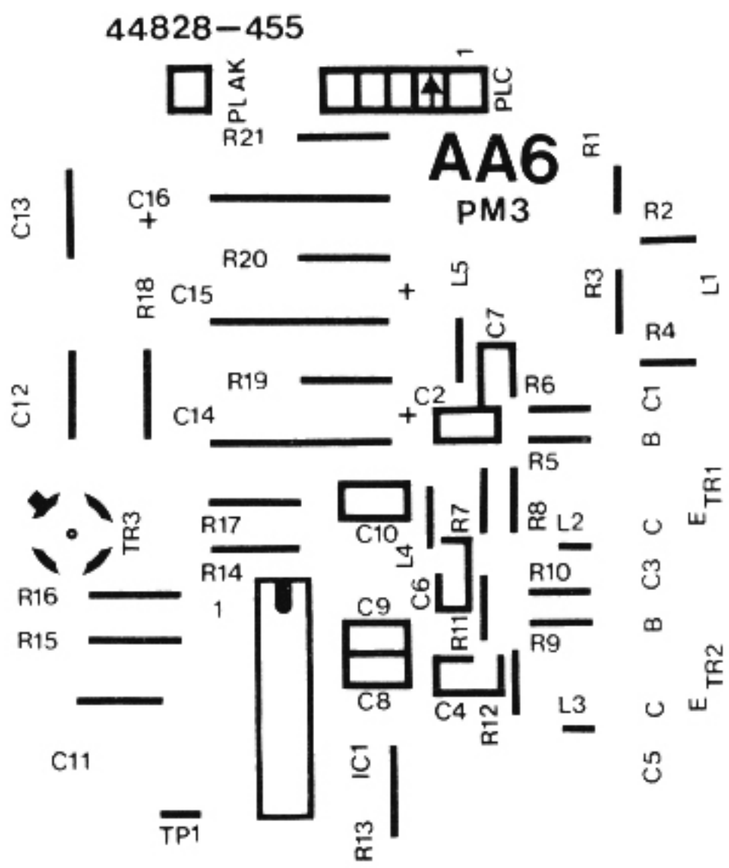
May 86



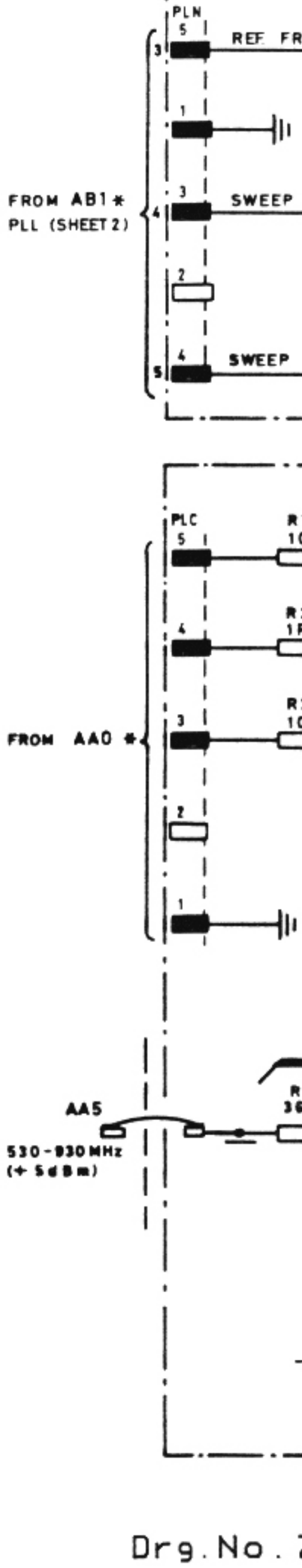
Component layout for AB2



Component layout for AB7



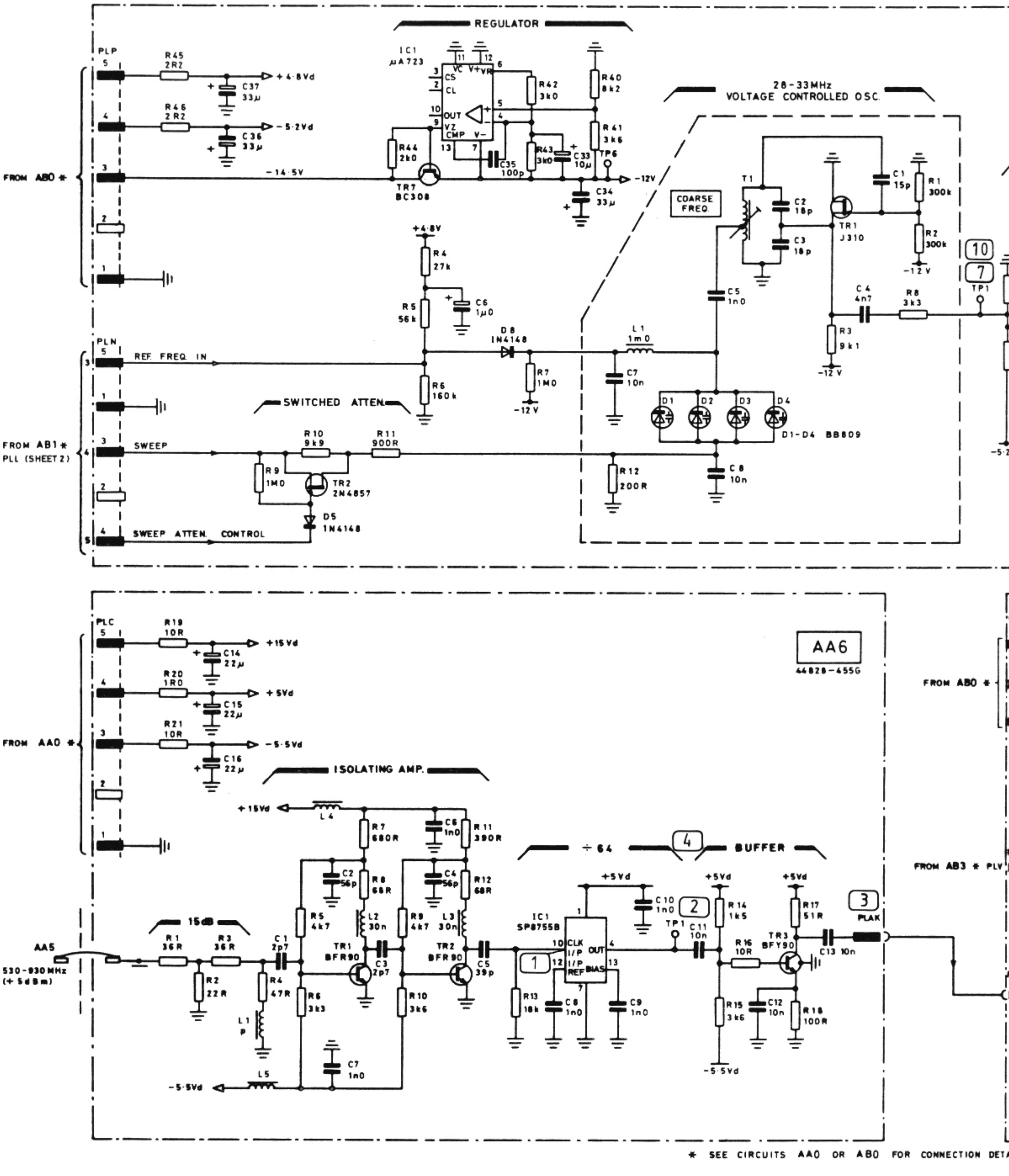
Component layout for AA6



Drg. No. 7
Sh. 5

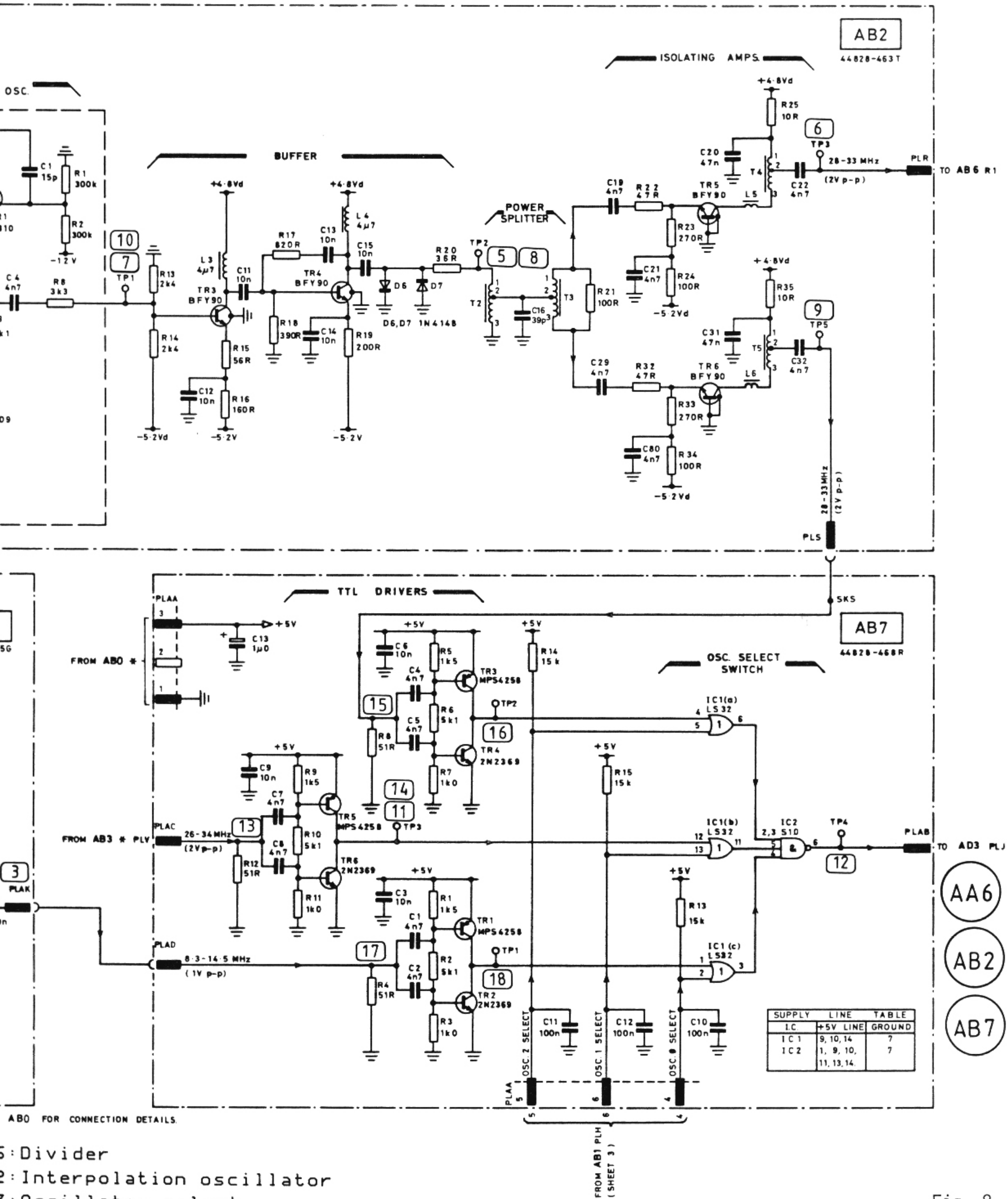
Fig. 8

May 86



Drg.No. Z44990-450
Sh.5 Iss.2

AA6: Divider
AB2: Interpolati
AB7: Oscillator



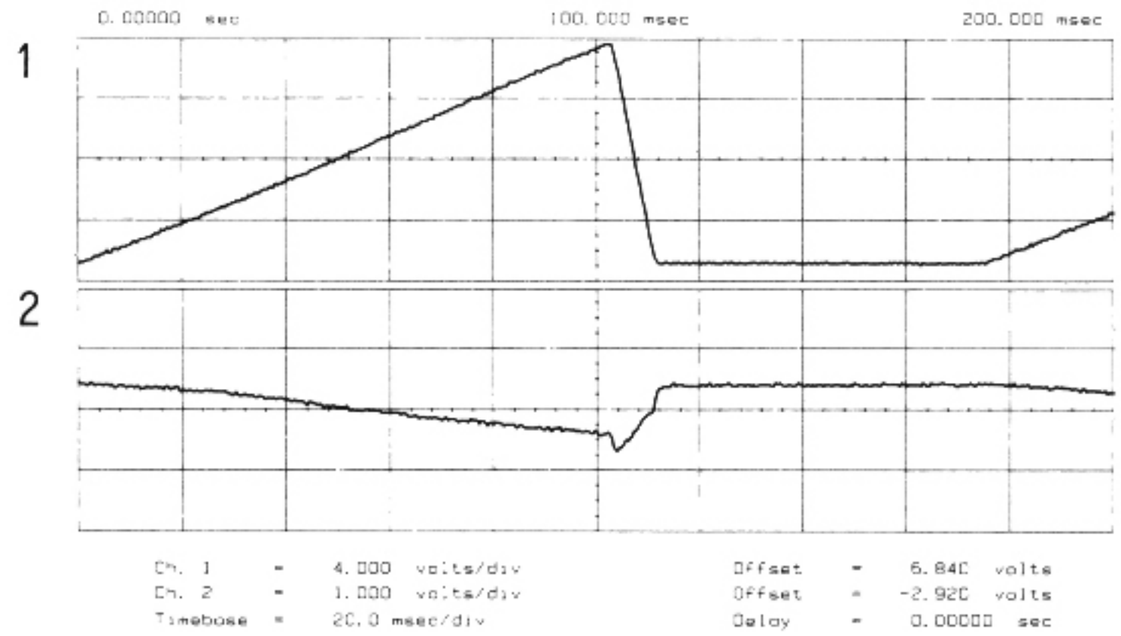
SUPPLY	LINE	TABLE
I.C.	+5V LINE	GROUND
I C 1	9, 10, 14	7
I C 2	1, 9, 10, 11, 13, 14.	7

5 : Divider
2 : Interpolation oscillator
7 : Oscillator select

1
2

BOARD : AA7

TEST POINT : PLP pin 3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : PLAN

PROCEDURE :

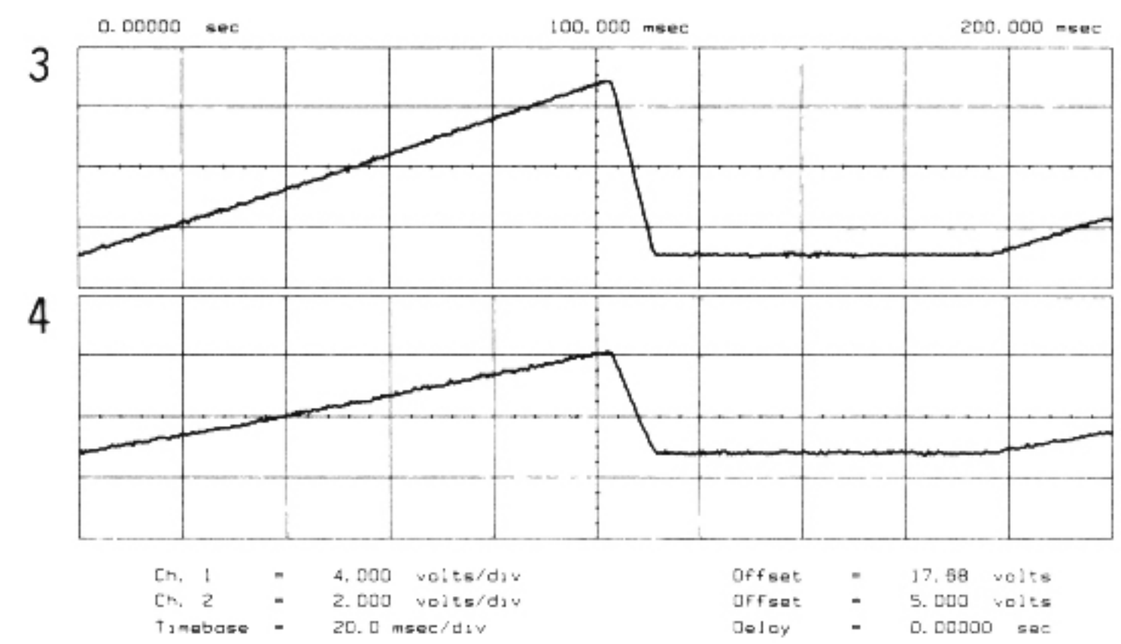
1. Press PRESET then select the following 2382 setting:

Span 10 MHz/DIV

3
4

BOARD : AA7

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : junction R7/R9

PROCEDURE :

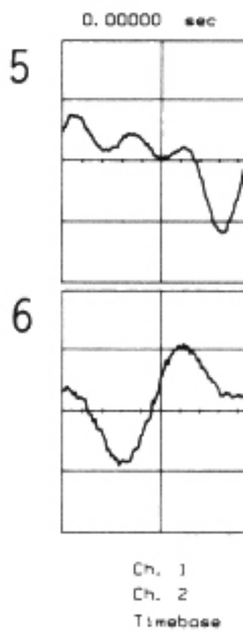
1. Press PRESET then select the following 2382 setting:

Span 10 MHz/DIV

5
6

BOARD : AA7

TEST POINT : junctio
SCOPE SETTING [DEFAU



TEST POINT : pin 1 o

PROCEDURE :

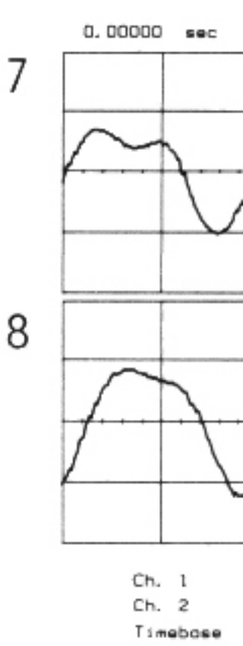
1. Press PRESET th

Reference
Span
Mode

7
8

BOARD : AA7

TEST POINT : output
SCOPE SETTING [DEFA

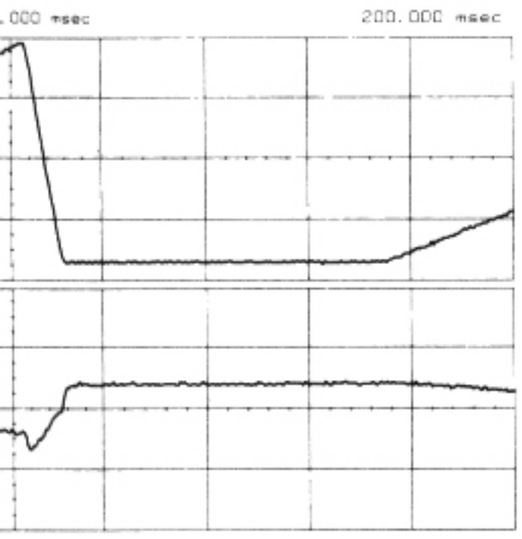


TEST POINT : pin 2

PROCEDURE :

1. Press PRESET th

Reference
Span
Mode

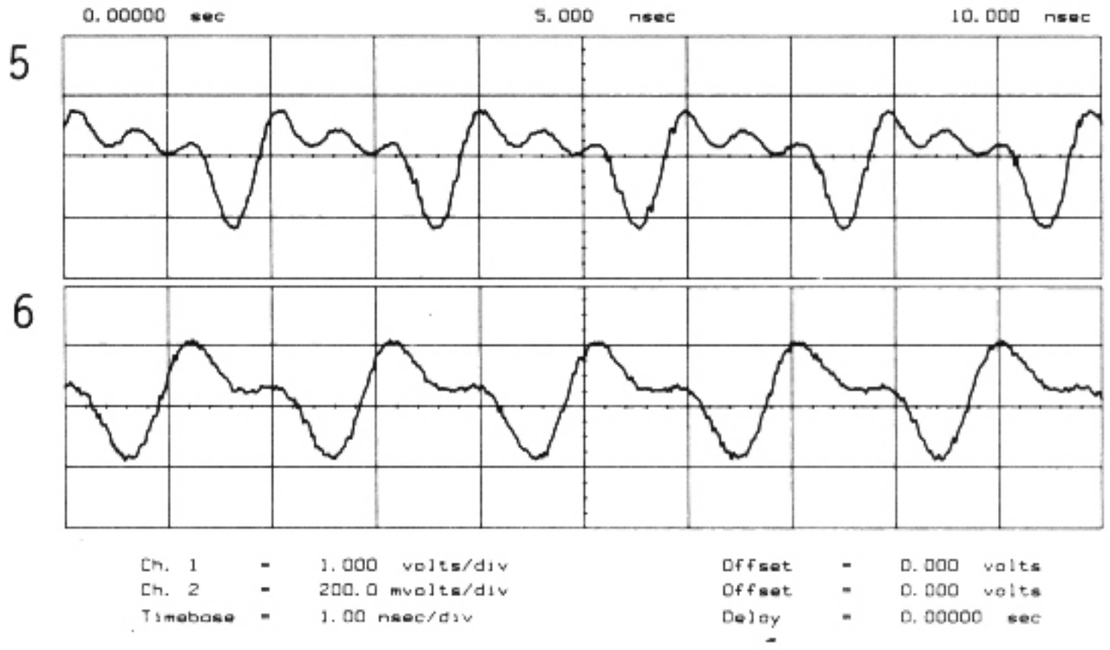


owing 2382 setting:

5
6

BOARD : AA7

TEST POINT : junction C16/T1 for Ch. 1
SCOPE SETTING [DEFAULT]

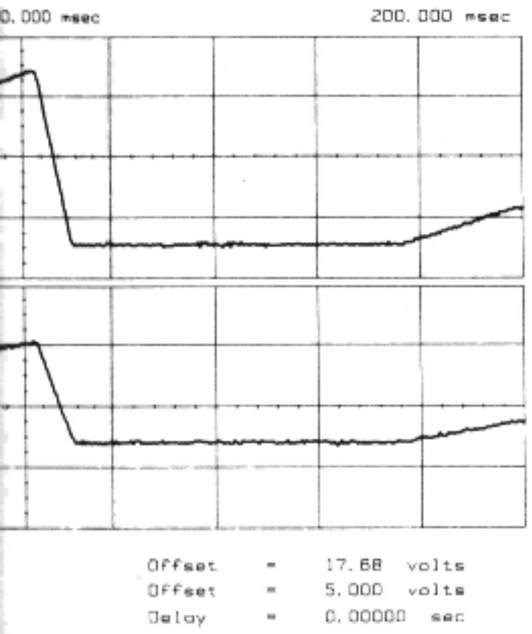


TEST POINT : pin 1 output to AE4 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter

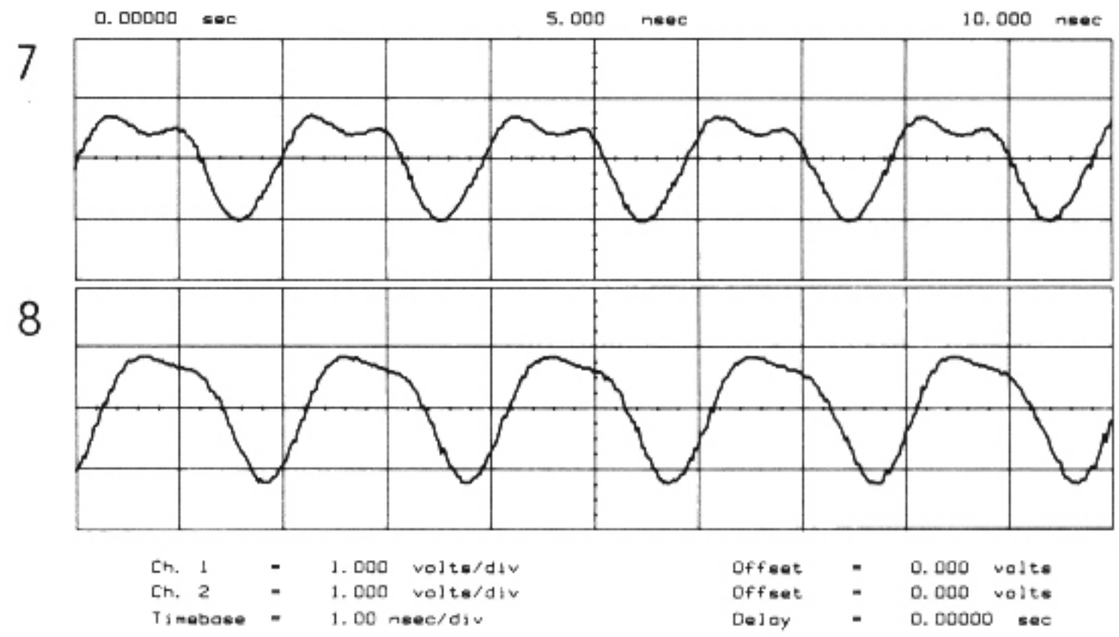


lowing 2382 setting:

7
8

BOARD : AA7

TEST POINT : output to AA8 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : pin 2 (output to AA2a) for Ch. 2

PROCEDURE :

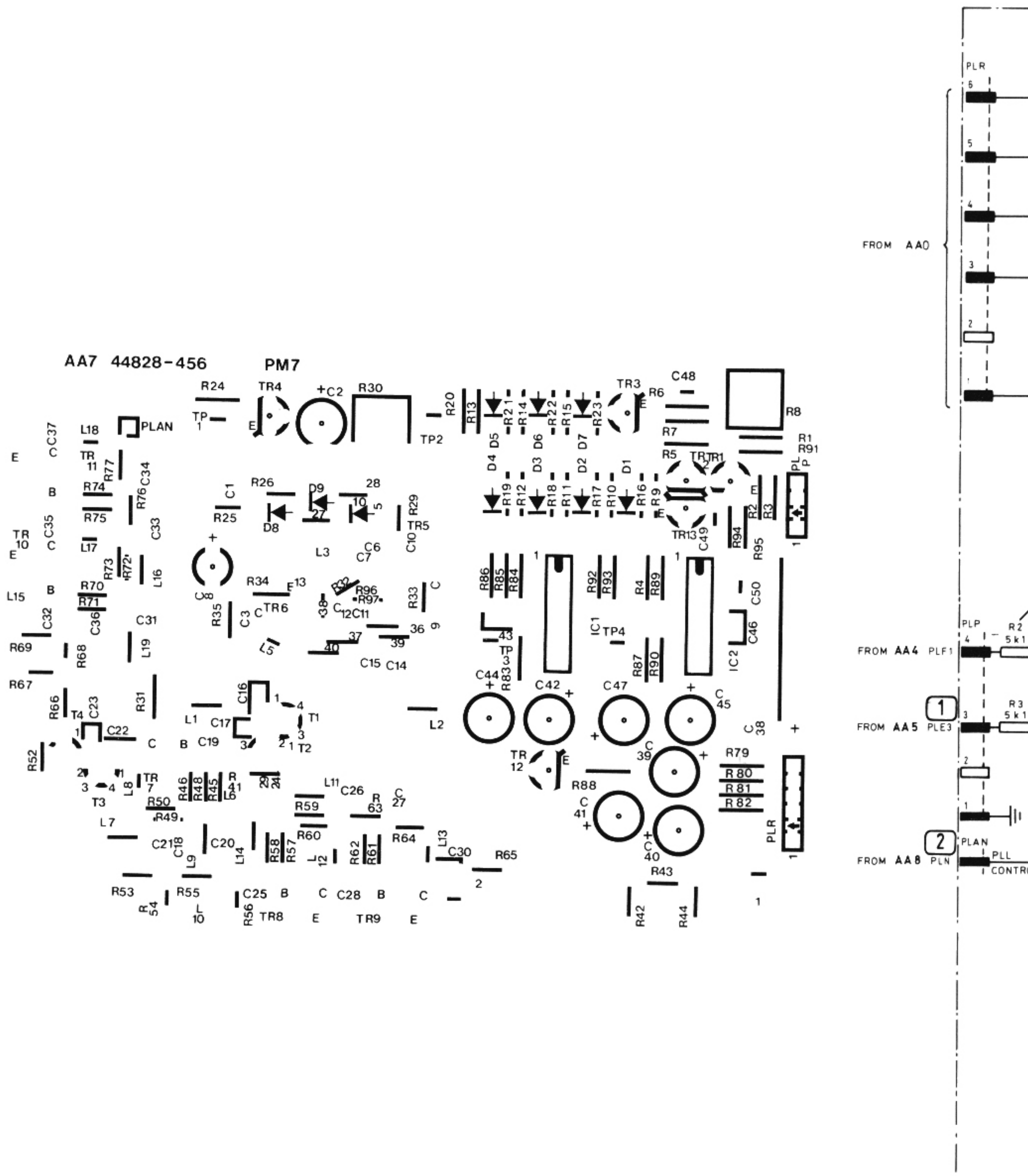
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter

Waveforms for AA7

Fig. 9a

May 86

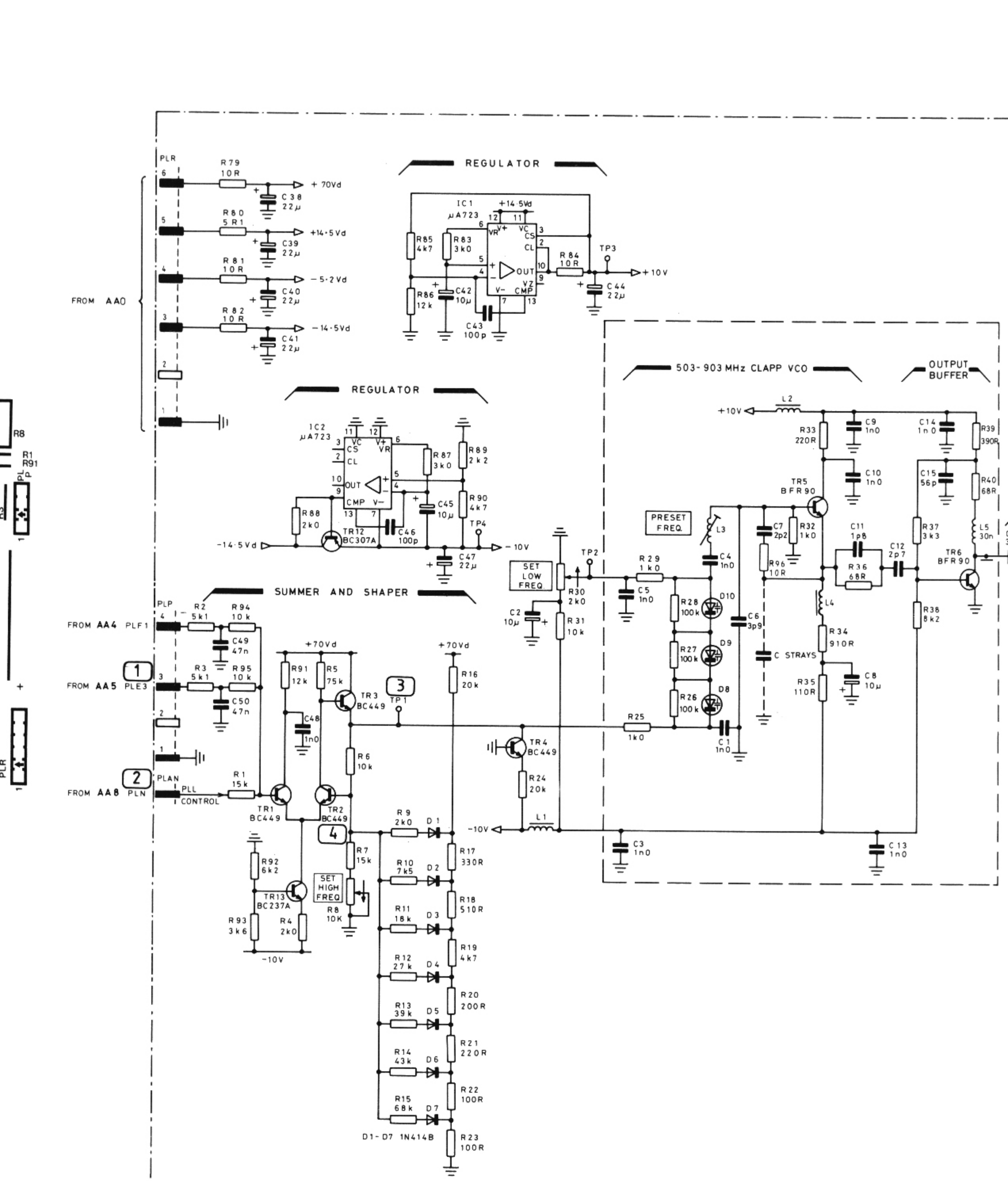


Component layout for AA7

Drg. No.
Sh. 1

Fig. 9

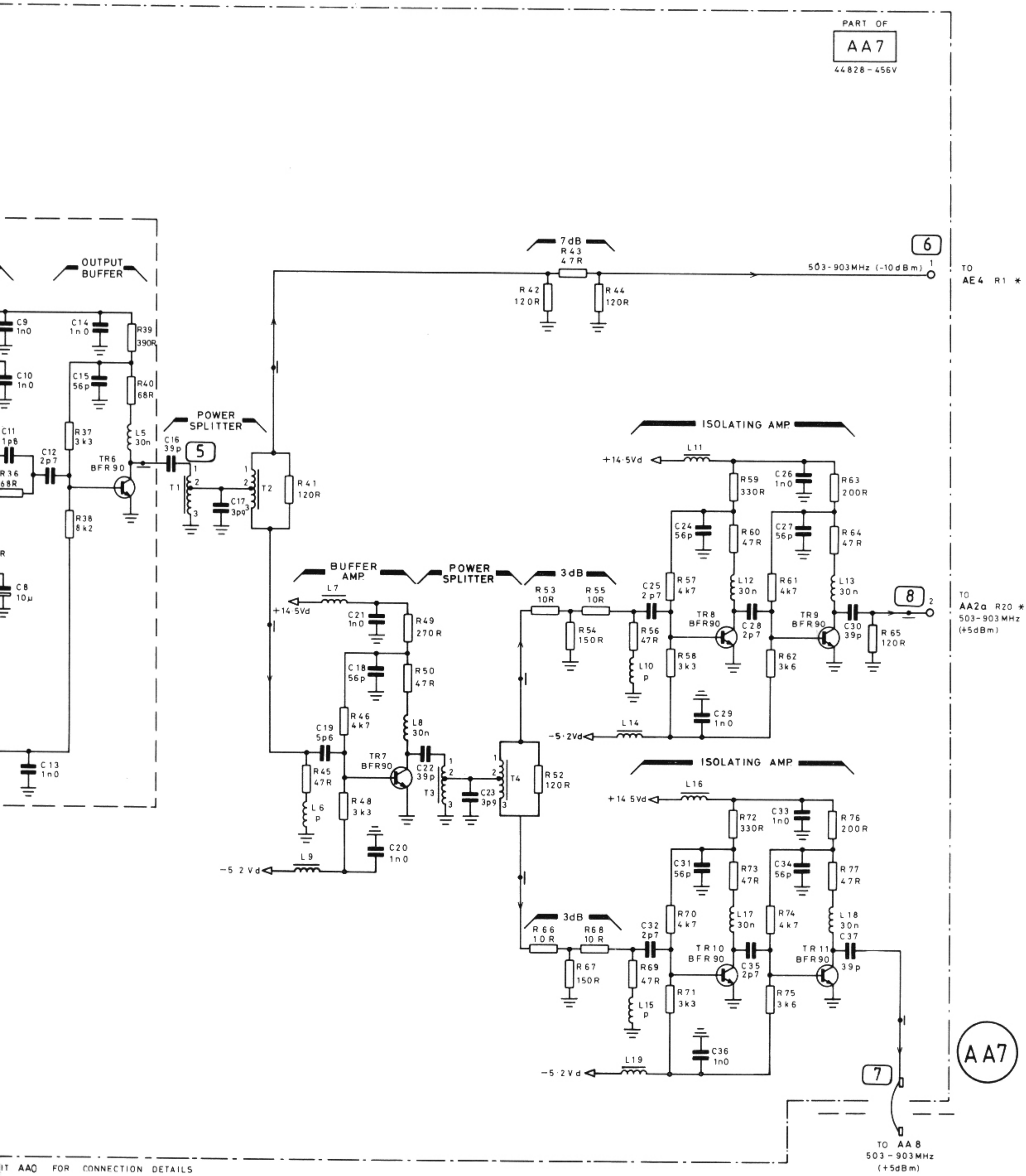
May 86



* SEE CIRCUIT AA0 FOR CONNECTION DE

Drg. No. Z44828-456V
Sh. 1 Iss. 5

AA7 : S1

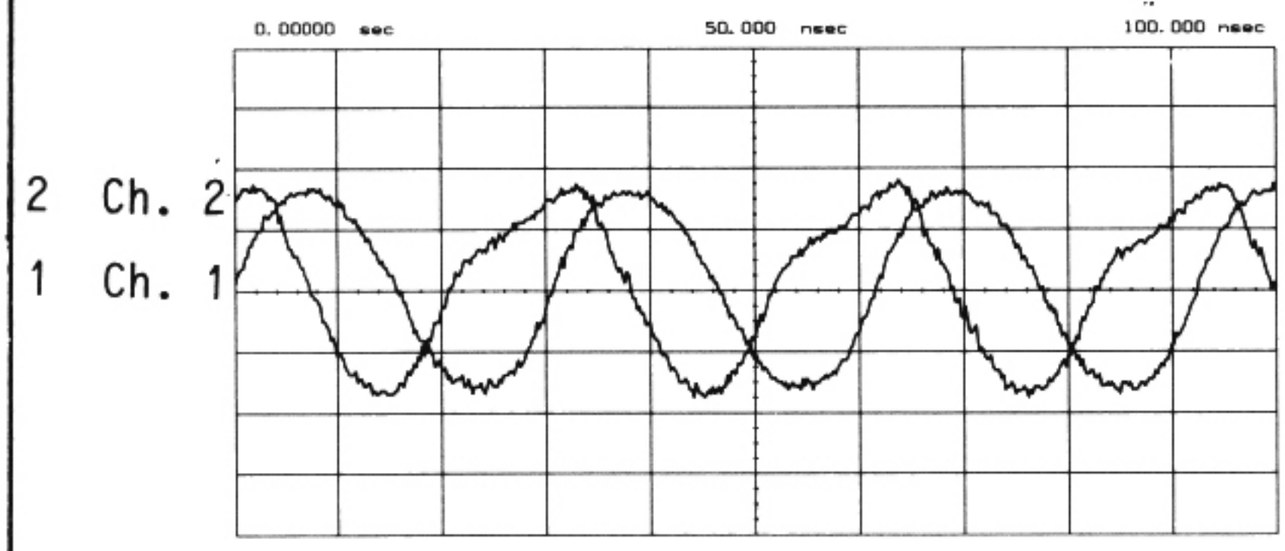


AA7 : Slave VCO

1
2

BOARD : AA8

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	500.0 mvolts/div	Offset	=	-3.500 volts
Ch. 2	=	500.0 mvolts/div	Offset	=	-3.500 volts
Timebase	=	10.0 nsec/div	Delay	=	0.00000 sec

TEST POINT : TP2 for Ch. 2

PROCEDURE:

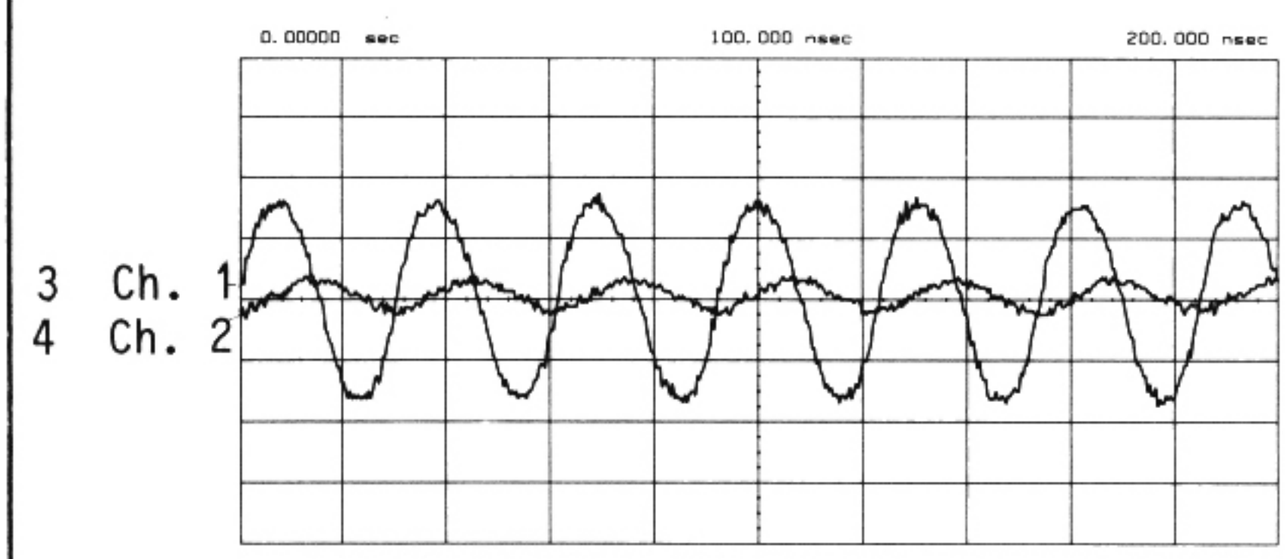
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter

3
4

BOARD : AA8

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	500.0 mvolts/div	Offset	=	-3.500 volts
Ch. 2	=	500.0 mvolts/div	Offset	=	-3.500 volts
Timebase	=	20.0 nsec/div	Delay	=	0.00000 sec

TEST POINT : TP4 for Ch. 2

PROCEDURE :

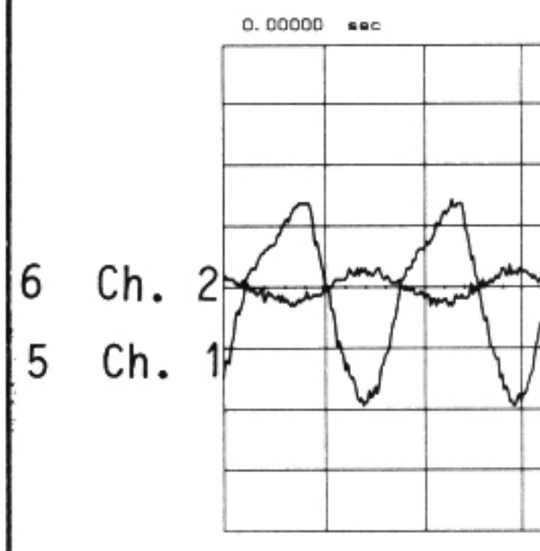
1. Press PRESET then select the following 2382 settings:

Reference frequency	10 MHz
Span	200 kHz/DIV
Mode	meter

5
6

BOARD : AA8

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	500.0 m			
Ch. 2	=	500.0 m			
Timebase	=	20.0 ns			

TEST POINT : TP3 for Ch. 2

PROCEDURE :

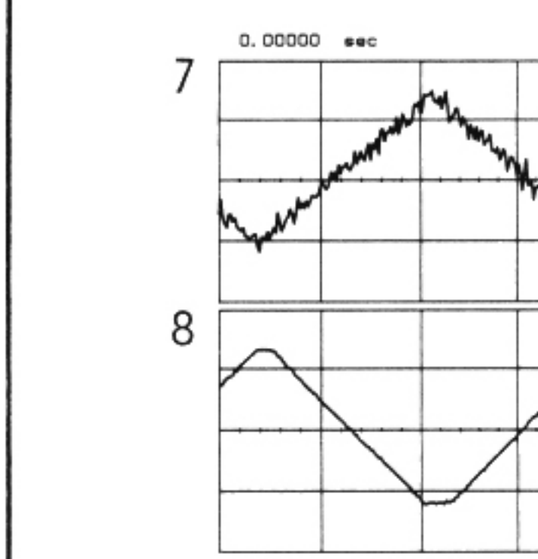
1. Press PRESET then selec

Reference frequenc	
Span	
Mode	

7
8

BOARD : AA8 search o

TEST POINT : TP7 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	400.0 m			
Ch. 2	=	10.00			
Timebase	=	50.0 ns			

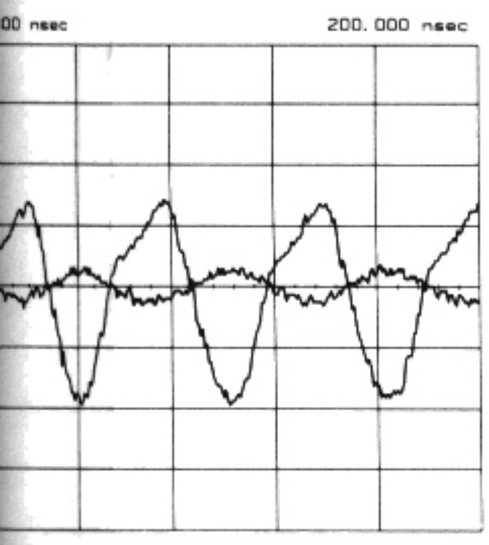
TEST POINT : PLN for Ch. 2

PROCEDURE :

1. Press PRESET then sele

Full span

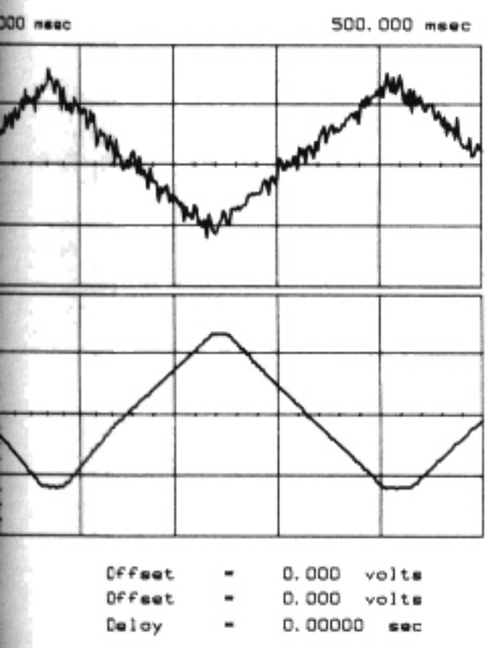
W



owing 2382 setting:

MHz
kHz/DIV
er

n SKN connected to PLAS



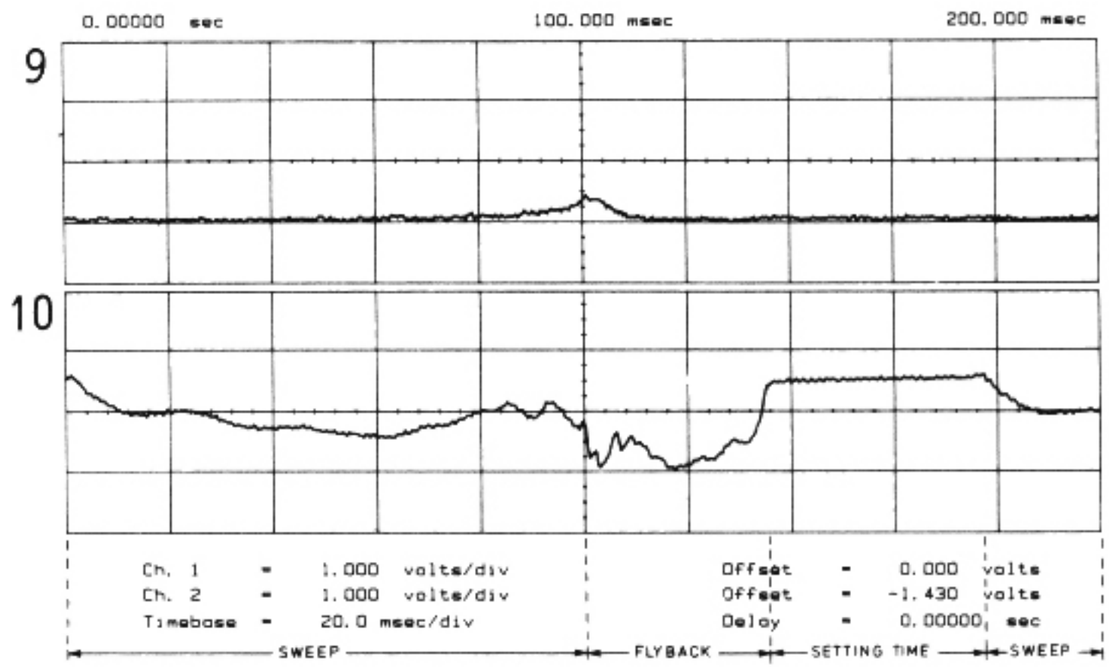
lowing 2382 setting:

s for AA8

9 BOARD : AA8

10 FUNCTION : PHASE LOCK CHECK SIGNAL.

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]



FUNCTION [10] : ERROR SIGNAL TO AA7.

TEST POINT : PLN for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 setting:

   Full span

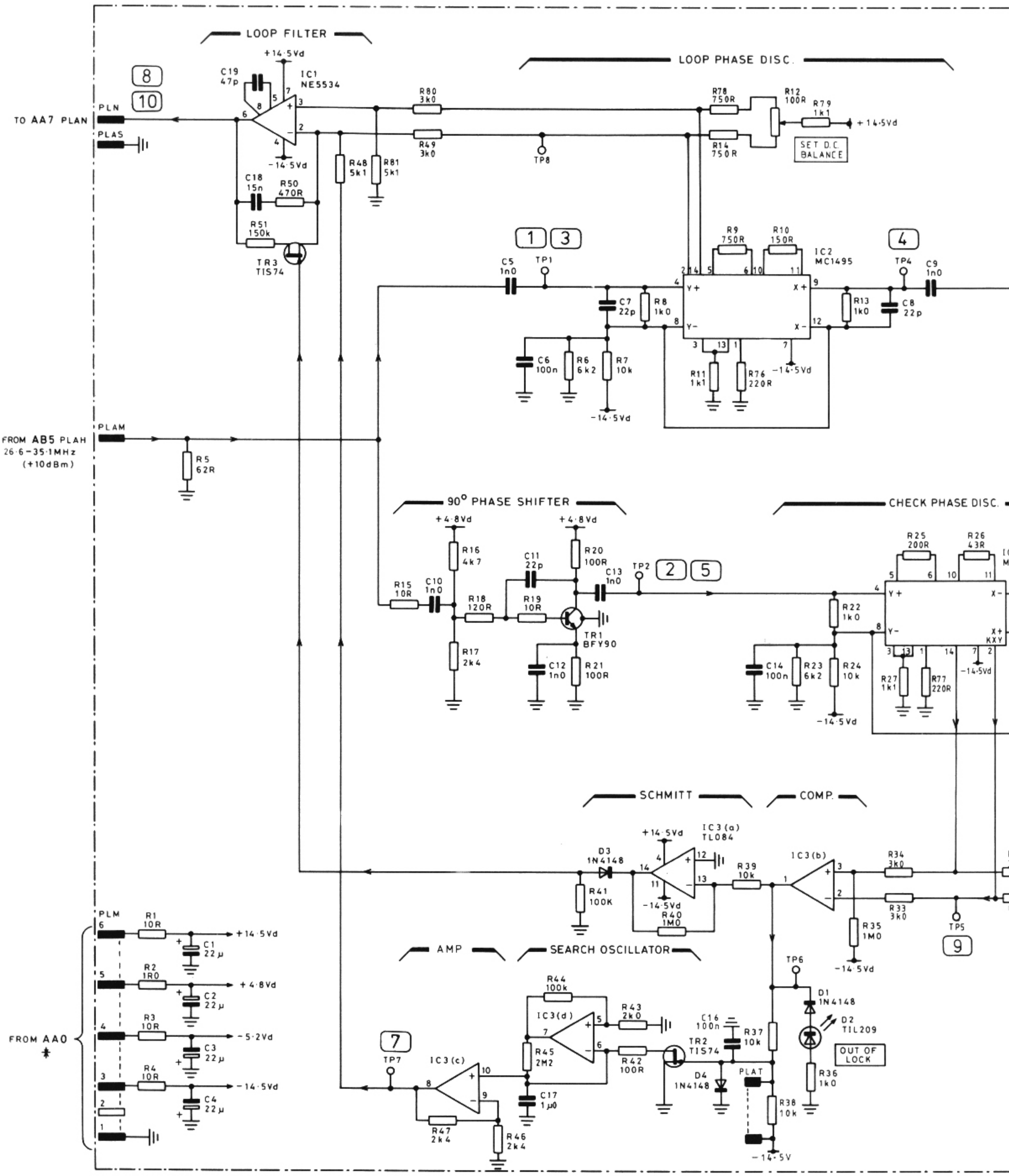
Fig. 10a

May 86

Component layout for AA8

Fig. 10

May 86



Drg. No. Z44828-457S
Sh. 1 Iss. 8

✱ SEE CIRCUIT A0 FOR CONNECTION DETAIL

AA8: Master/slave phase d

AA 8
44828-4575

ISOLATING AMP.
+14·5Vd
L3
R62 220R
C24 1n0
R58 390R
R63 150R
C25 56p
R59 68R
C21 56p
R60 4k7
R56 4k7
C26 39p
L2
TR5 BFR96
C23 2p7
TR4 BFR90
C20 2p7
R54 24R
R52 24R
R55 47R
R53 36R
R57 3k6
L1 p
R61 4k3
C22 1n0
L4
-5·2Vd

FROM AA7 503-903MHz (+5dBm)

10dB

DOWN MIXER

X1 SBL-1X

R59 200R

4

TP4
C9 1n0
R13 1k0
C8 22p

CHECK PHASE DISC.

6

TP3
C15 1n0
IC4 MC1495
R25 200R
R26 43R
R29 1k0
R22 1k0
R24 10k
R27 1k1
R77 220R
-14·5Vd

ISOLATING AMP.
+14·5Vd
L8
R74 270R
C31 1n0
R70 470R
R75 68R
C32 56p
R71 68R
C28 56p
R72 4k7
R68 4k7
C33 39p
L7 30n
L6 30n
TR7 BFR90
C30 2p7
TR6 BFR90
C27 2p7
R66 36R
R64 36R
R67 47R
R65 22R
R69 3k3
L5 p
R73 3k6
C29 1n0
L9
-5·2Vd

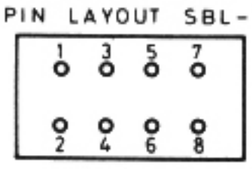
15dB

FROM AA5 503-903MHz (-5 dBm)

R34 3k0
R32 3k0
R28 200R
+14·5Vd
R33 3k0
R31 3k0
SET D.C. BALANCE
R35 1MΩ
TP5
9
14·5Vd

148
D2
TIL209
OUT OF LOCK

PIN LAYOUT SBL-1X



BOTTOM VIEW

A0 FOR CONNECTION DETAILS

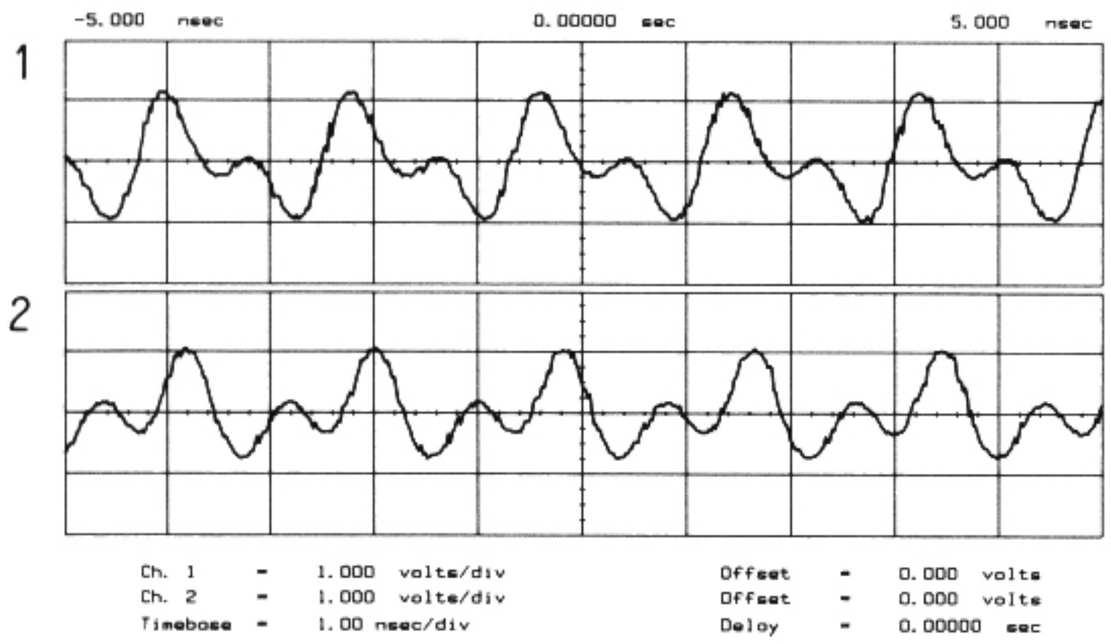
slave phase detector

Fig. 10
Chap. 7
Page 27

1 BOARD : AA9

2 FUNCTION : 550 MHz OUTPUT.

TEST POINT : junction G16/T1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : tag 1, terminated into 50 Ω, for Ch. 2

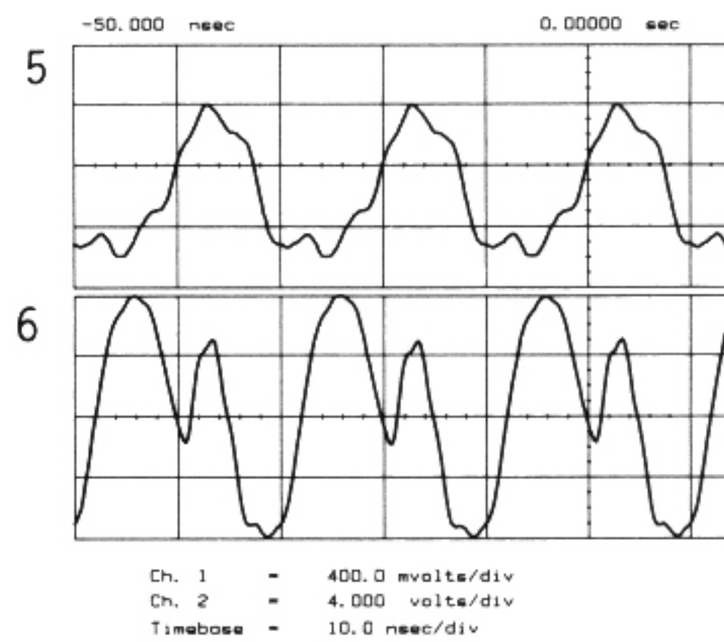
PROCEDURE :

1. Press PRESET.

5 BOARD : AA10

6 FUNCTION : 50 MHz INPUT AC1

TEST POINT : PLAC for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT TP2 for Ch. 2

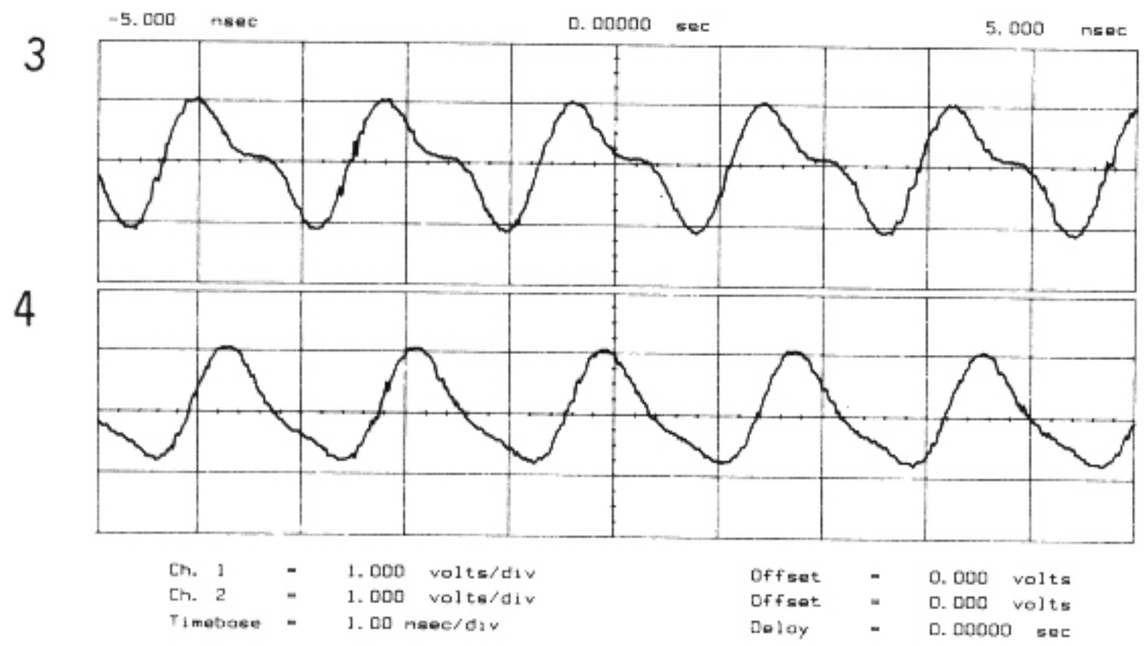
PROCEDURE :

1. Press PRESET.

3 BOARD : AA9

4

TEST POINT : 550 MHz output to AA3a
SCOPE SETTING [DEFAULT]



TEST POINT : 550 MHz output to AA10

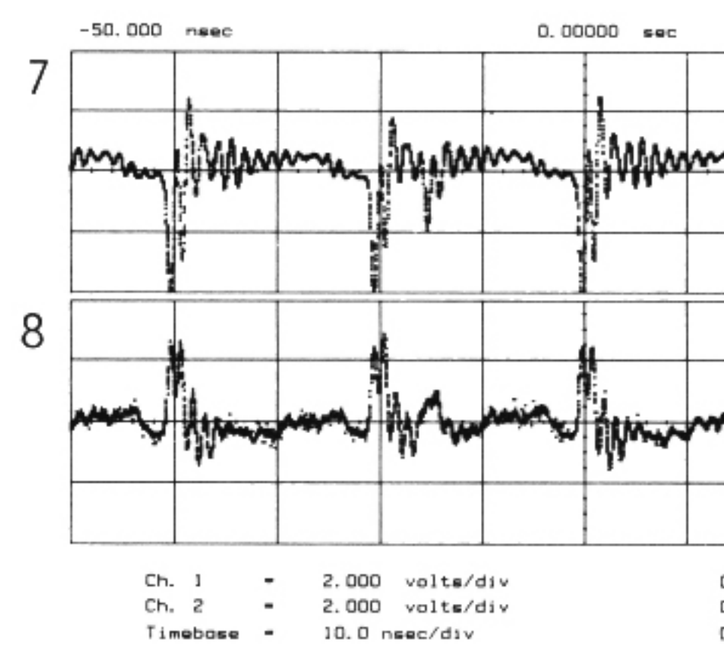
PROCEDURE :

1. Press PRESET.

7 BOARD : AA10

8 FUNCTION : SAMPLING GATE DRIVE

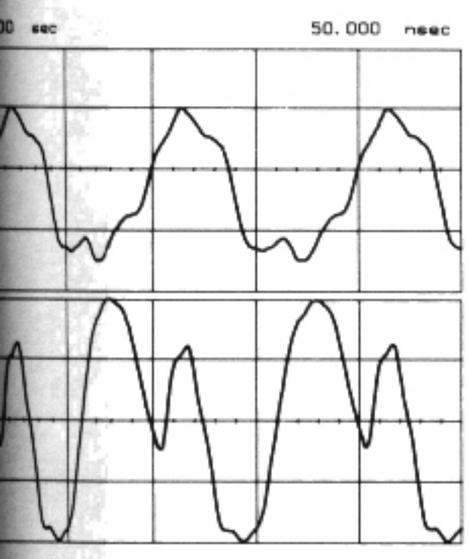
TEST POINT : junction R11/C11
SCOPE SETTING [DEFAULT]



TEST POINT : junction R12/C12

PROCEDURE :

1. Press PRESET.

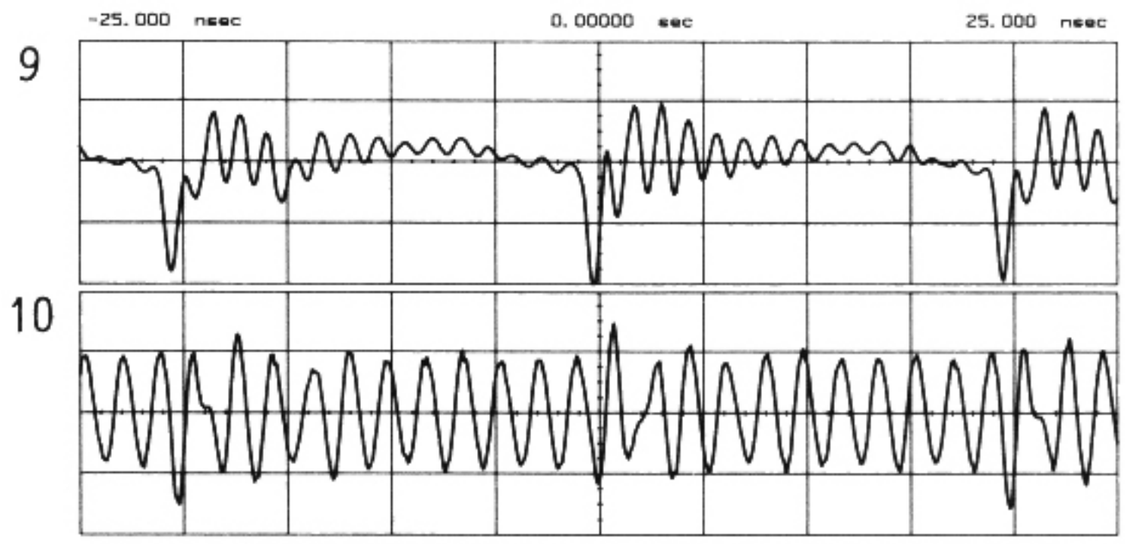


Offset - 190.0 mvolts
Offset - 13.64 volts
Delay - 0.00000 sec

9 BOARD : AA10

10 FUNCTION : SAMPLING GATE DRIVE

TEST POINT : junction R11/C11
SCOPE SETTING [DEFAULT]



Ch. 1 - 2.000 volts/div
Ch. 2 - 1.000 volts/div
Timebase - 5.00 nsec/div

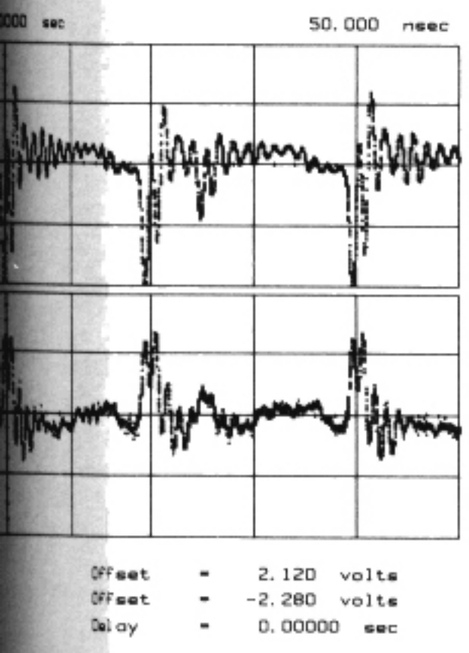
Offset - 2.120 volts
Offset - 0.000 volts
Delay - 0.00000 sec

FUNCTION : INPUT TO GATE.

TEST POINT : junction D1, D3 and R10

PROCEDURE :

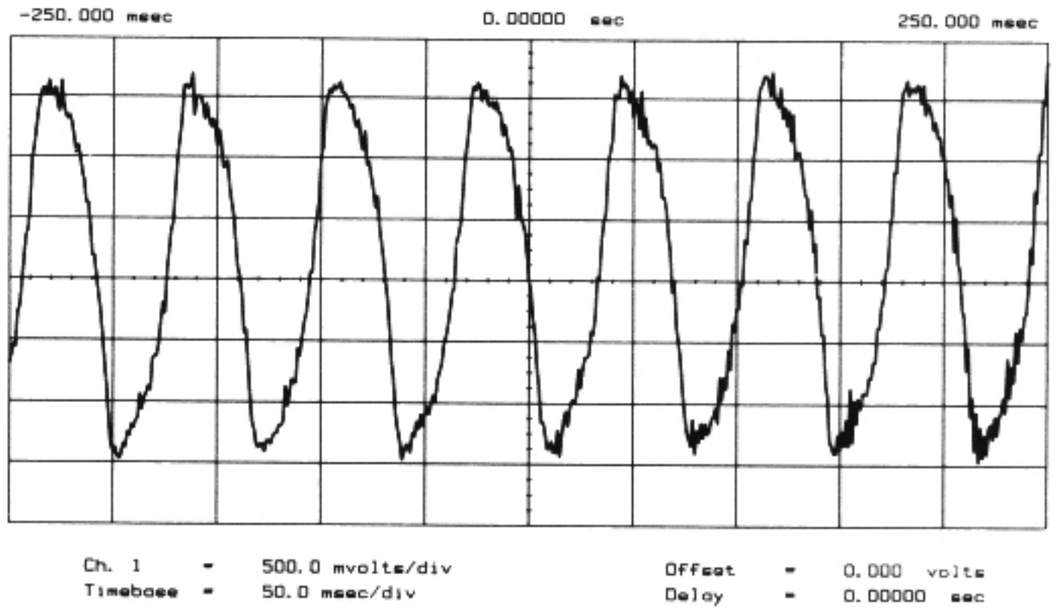
1. Press PRESET.



Offset - 2.120 volts
Offset - -2.280 volts
Delay - 0.00000 sec

11 BOARD : AA10 with SKAD grounded through PLNP
FUNCTION : SEARCH OSCILLATOR

TEST POINT : TP5
SCOPE SETTING [DEFAULT]



Ch. 1 - 500.0 mvolts/div
Timebase - 50.0 msec/div

Offset - 0.000 volts
Delay - 0.00000 sec

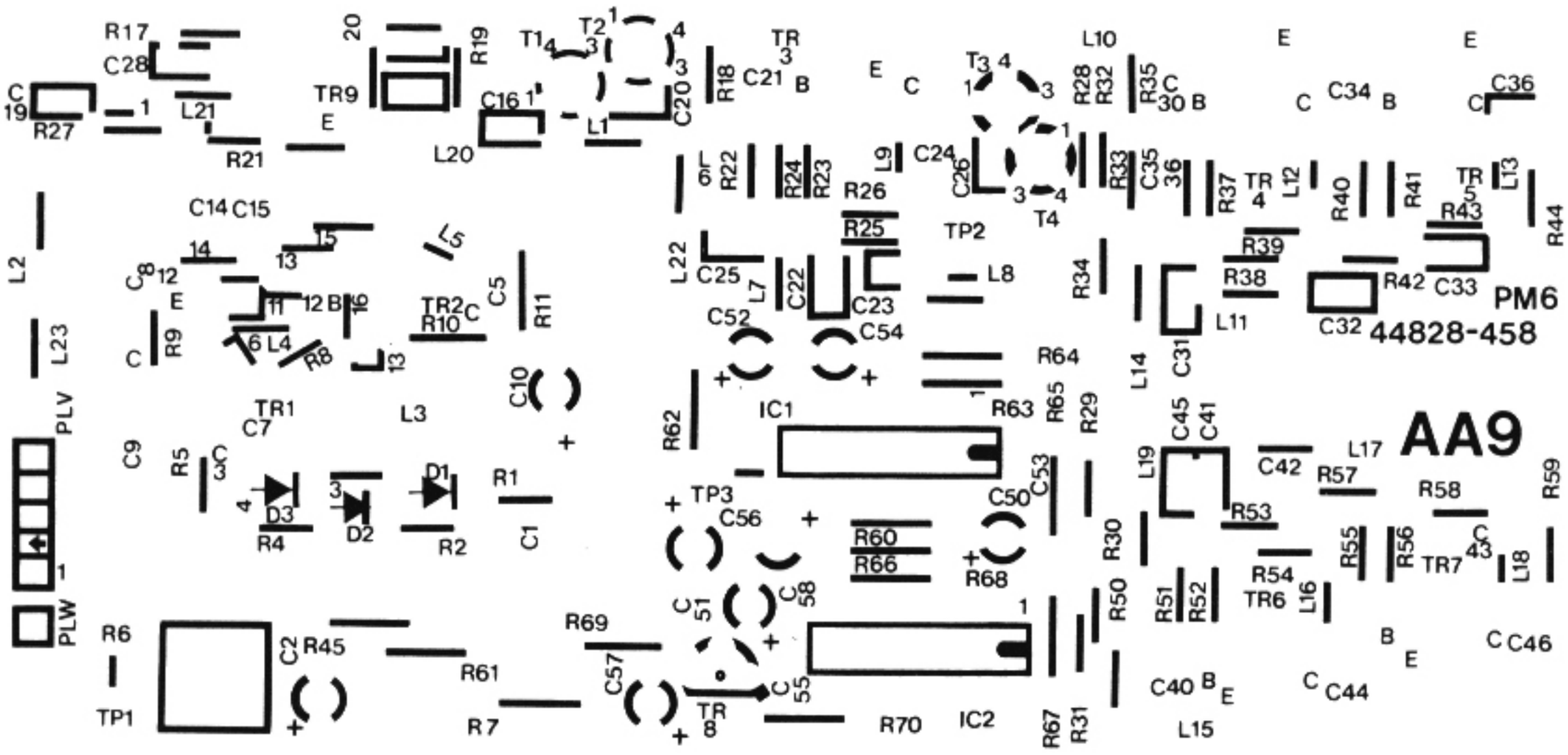
PROCEDURE :

1. Press PRESET.

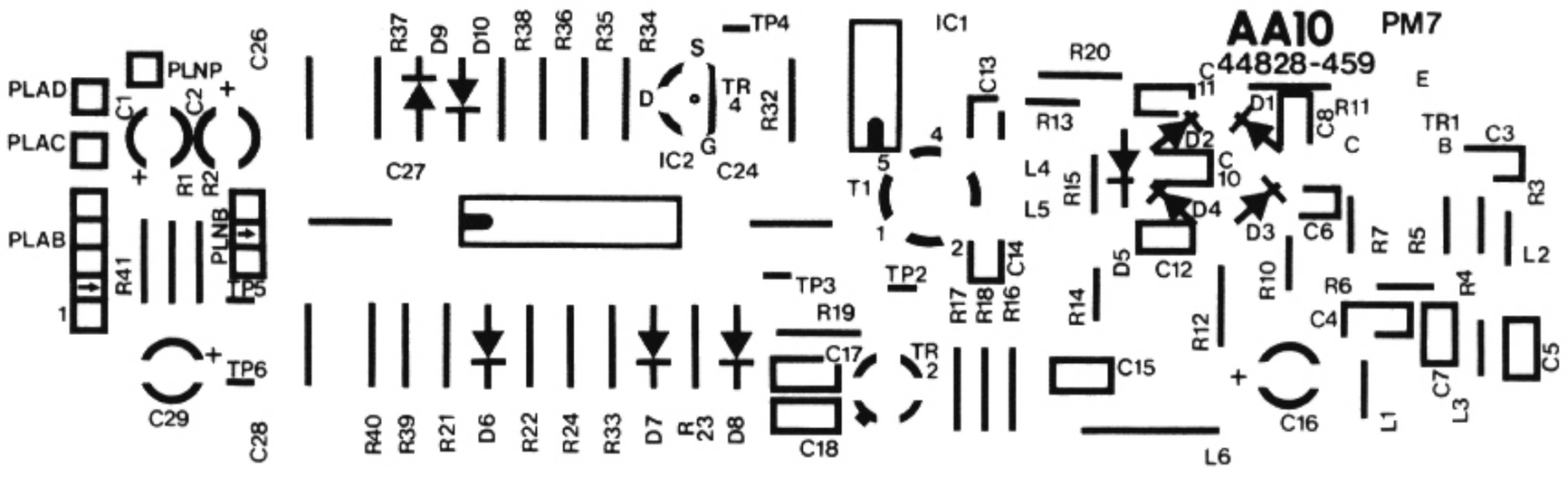
9 & AA10

Fig. 11a

May 86



Component layout for AA9



Component layout for AA10

Fig. 11

May 86

Drg. No. Z
Sh. 6 I

FROM AA0 ✱

PLV 5 — R60 10R — +15Vd — C50 10µ
4 — R61 10R — -5·5Vd — C51 10µ
3 — R69 10R — -15Vd — C57 10µ
2
1

REGULATOR

IC1 µA723 — +15Vd — R64 4k7 — R62 3k0 — R65 12k — C52 10µ — C53 100p — R63 10R — TP2 — +10V — C54 10µ

550MHz CLAPP VCO

+10V — L2 — R9 220R — C8 1n0 — C14 1n0 — R14 390R — C15 56p — R15 68R — L5 30n — R13 3k3 — C9 1n0 — TR1 BFR90 — R8 1k0 — C6 4p7 — C11 1p8 — R12 120R — C12 2p7 — TR2 BFR90 — C16 39p — C7 3p9 — C3 1n0 — L3 — PRESET FREQ. — R5 1k0 — C4 1n0 — R4 100k — D3 — R3 100k — D2 — R2 100k — D1 — D1-D3 BB405 — R1 100R — C1 1n0 — C STRAYS — L4 — R10 910R — R11 110R — C10 10µ — R16 6k2 — C13 1n0 — C5 1n0 — L1 — -10V

OUTPUT BUFFER

POW SPLI — T1 — 1 — 2 — 3

REGULATOR

IC2 µA723 — R66 3k0 — R67 2k2 — R68 4k7 — C56 10µ — TP3 — R70 2k0 — TR8 BC307A — C55 100p — C57 10µ — C58 10µ — -15Vd — -10V

SET FREQ — R7 4k7 — TP1 — R6 10k — C2 10µ — R45 4k7

PLW — V TUNE

AA9
44828 -458W

AA10
44828 - 459D

LEAD/LAG FILTER

PLAD — TP6 — R39 15k — C28 100n — R40 47R — PLNP

SEARCH OSC.

TP5 — 11 — IC2 (d) TL074CP — R36 10k — R35 3k0 — TP4 — C27 220n — R37 62k — C26 220n — R38 62k — D10 — D9 — 1N4448 — PLNB

SWITCHED GAIN AMP

IC2 (c) TL074CP — +15Vd — -15V — R34 11k — R32 6K2 — TR4 TIS74

CORRECT LOCK DETECTOR

+15V — R21 13k — IC2 (a) TL074CP — D6 1N4148 — R22 3k9 — IC2 (b) TL074CP — D7 1N4148 — R23 13k — -15V — R24 10k — R33 10k — C24 220n — D8 1N4148 — TP3

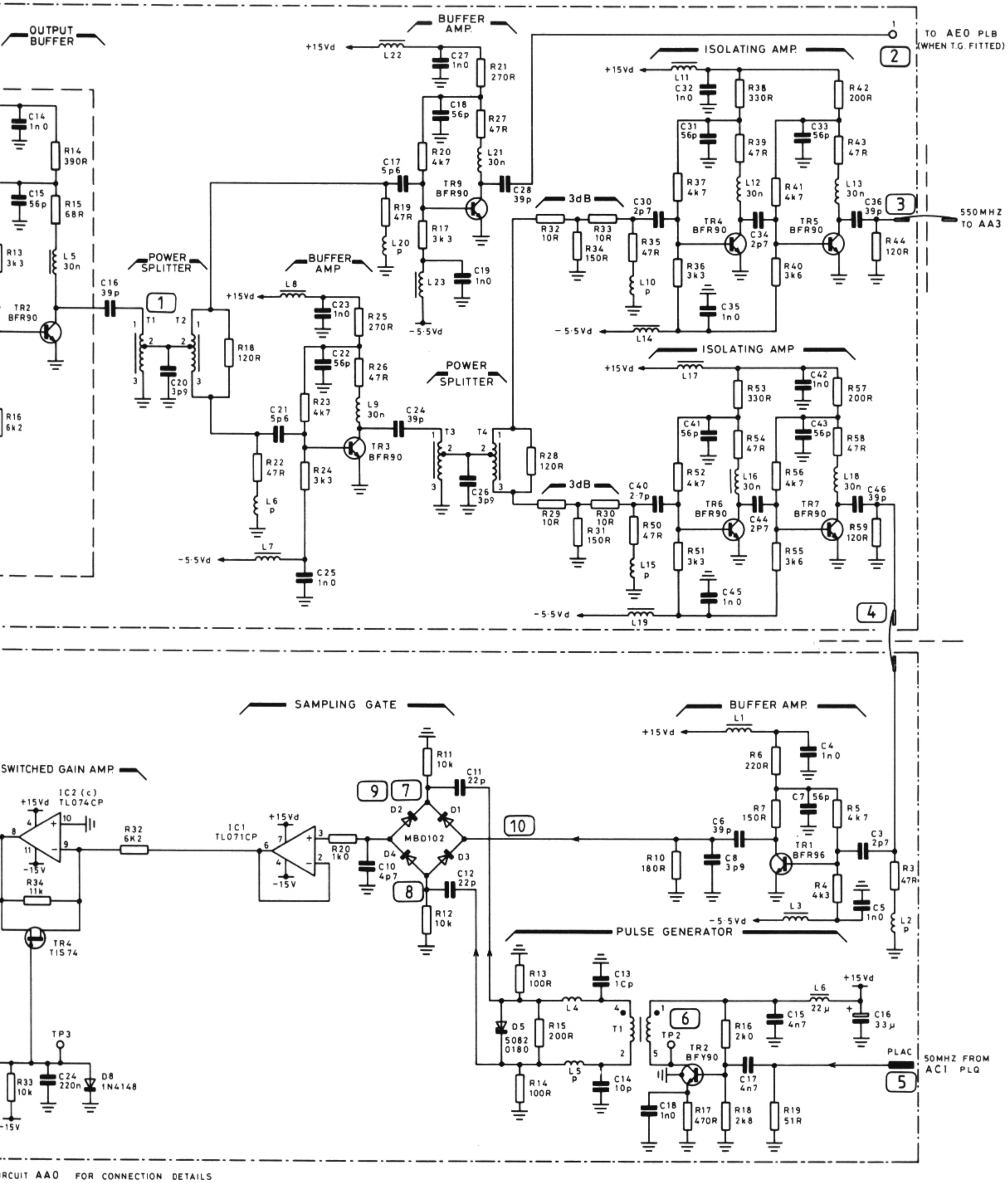
PLAB 5 — R1 10R — +15Vd — C1 33µ
4 — R2 10R — -5·5Vd — C2 33µ
3 — R41 10R — -15Vd — C29 33µ
2
1

FROM AA0 ✱

✱ SEE CIRCUIT AA0 FOR CONNECTION

Drg.No. Z44990-450
Sh.6 Iss.2

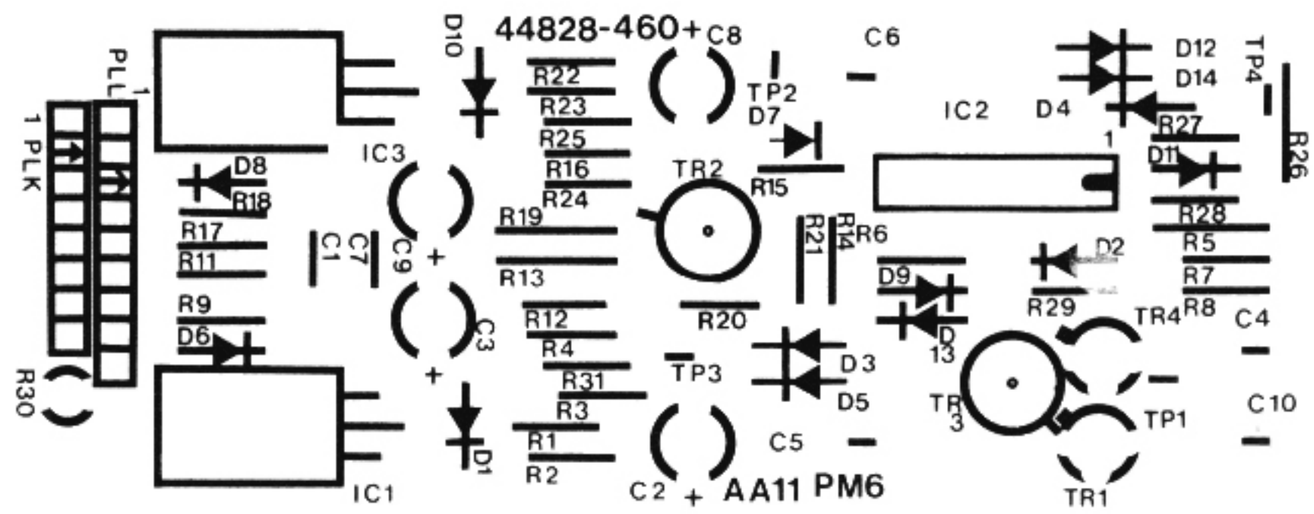
AA9 : Second LO V
AA10 : Sampling s



RCUIT AA0 FOR CONNECTION DETAILS

9 : Second LO VCO
10 : Sampling gate

Fig. 11
Chap. 7
Page 29/30



Component layout for AA11

Fig. 12

May 86

AA11

44828-4605

+10V REGULATOR

D1
1N4148

IC1
LM317

VIN VOUT
ADJ

C1
100n

R1
240R

C3
33µ

C2
10µ

R2
1k6

FAN CONTROL
TEMP. SENSOR

PLK

8

7

R30
47k @ 20°C
-t°

6

+15V

5

+5V

FROM AA0 ✱

4

-5·5V

3

-15V

2

1

-10V REGULATOR

C8
10µ

R22
1k6

C7
100n

IC3
LM317

ADJ
VIN VOUT

R23
240R

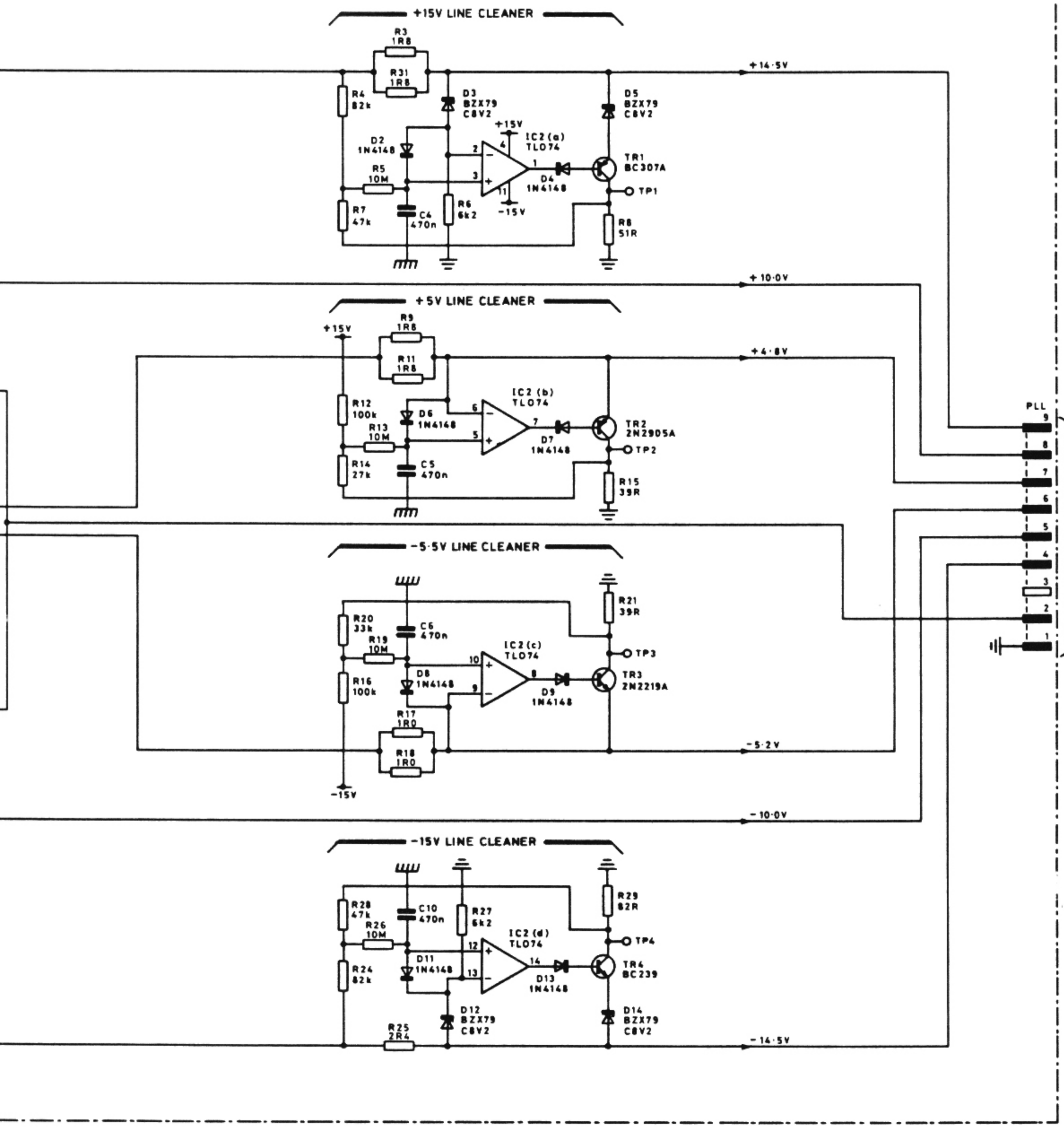
C9
33µ

D10
1N4148

✱ SEE CIRCUIT AA0 FOR CONNECTION DETAILS

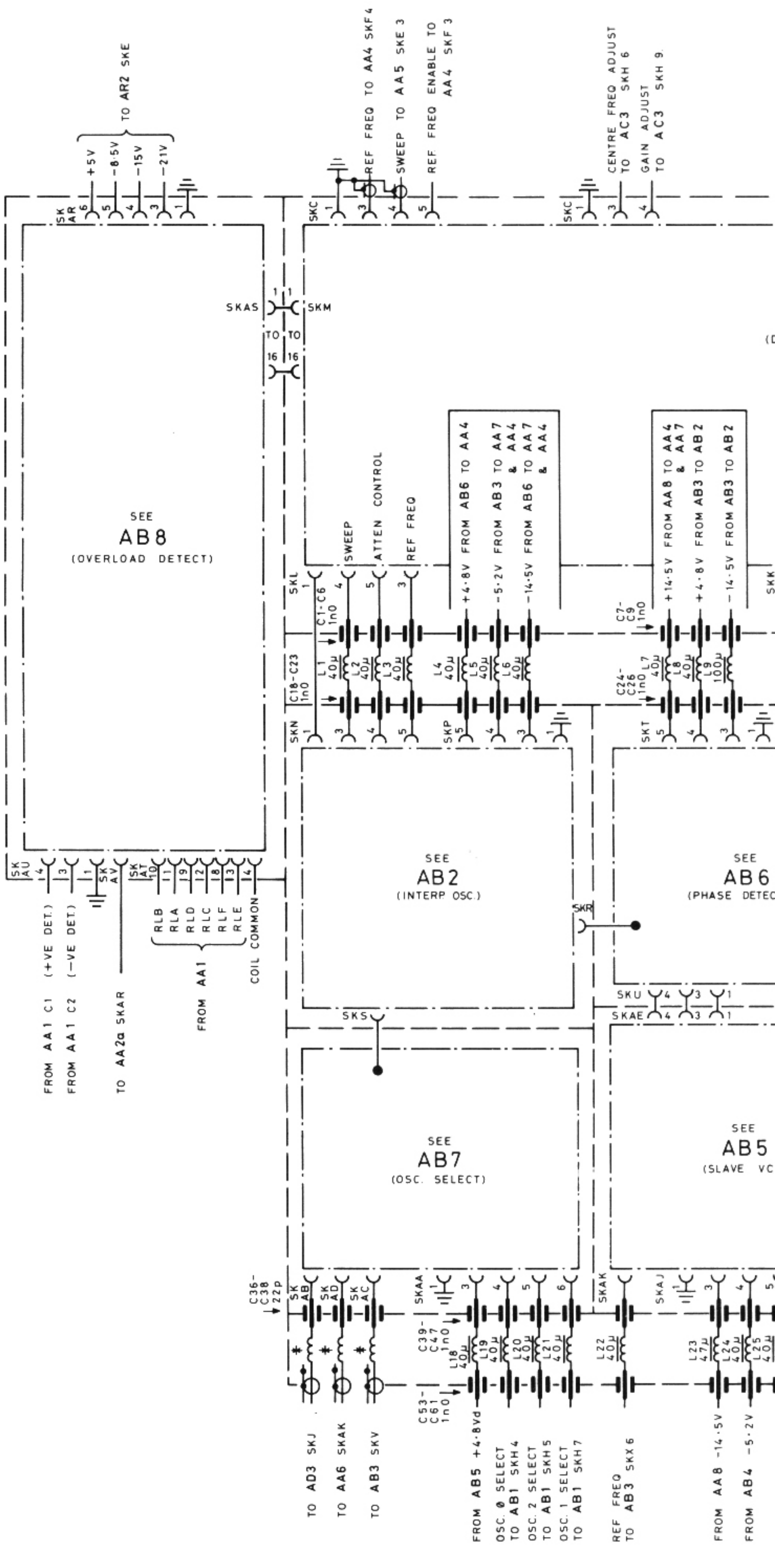
Drg.No.Z44828-460S
Sh.1 Iss.1

AA11:Line cleaner

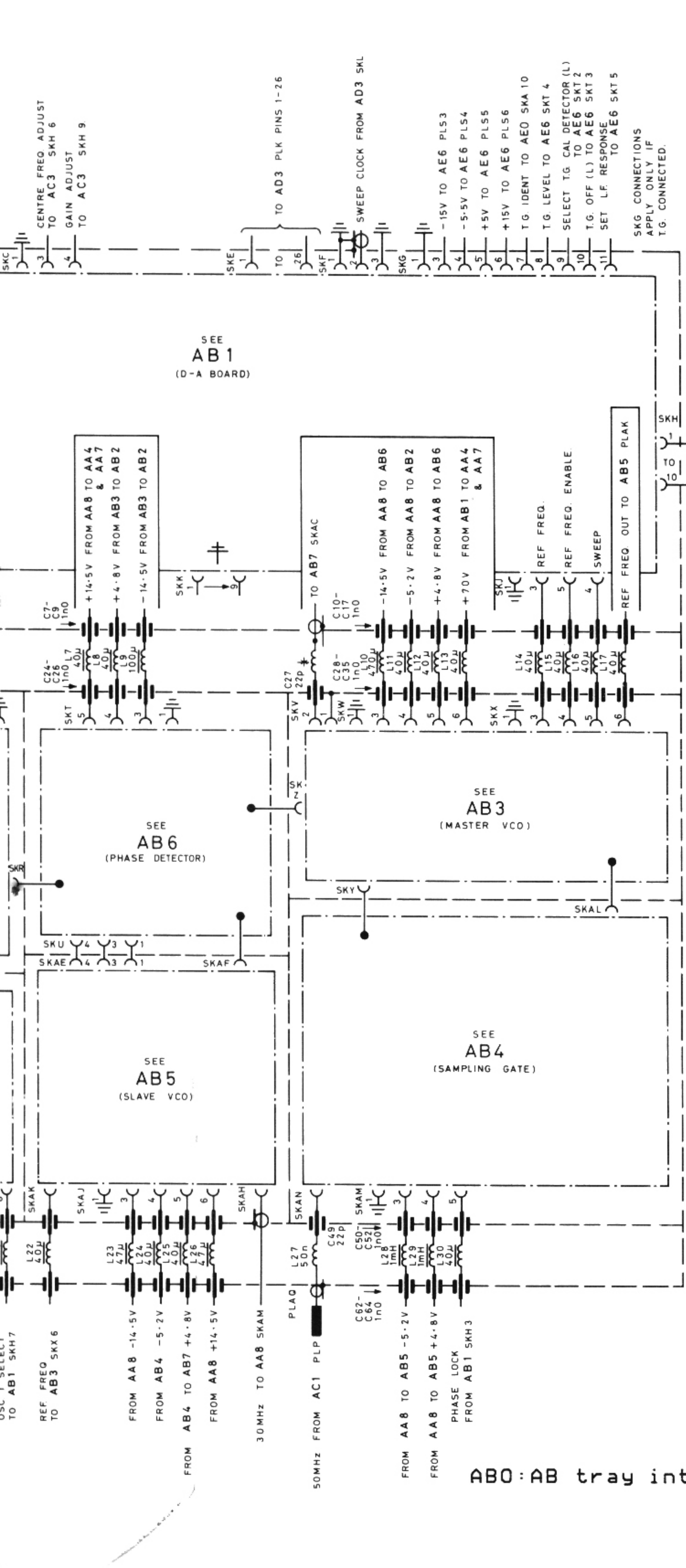


FOR CONNECTION DETAILS

:Line cleaner



Drg. No. Z44990-450
Sh. 2 Iss. 2

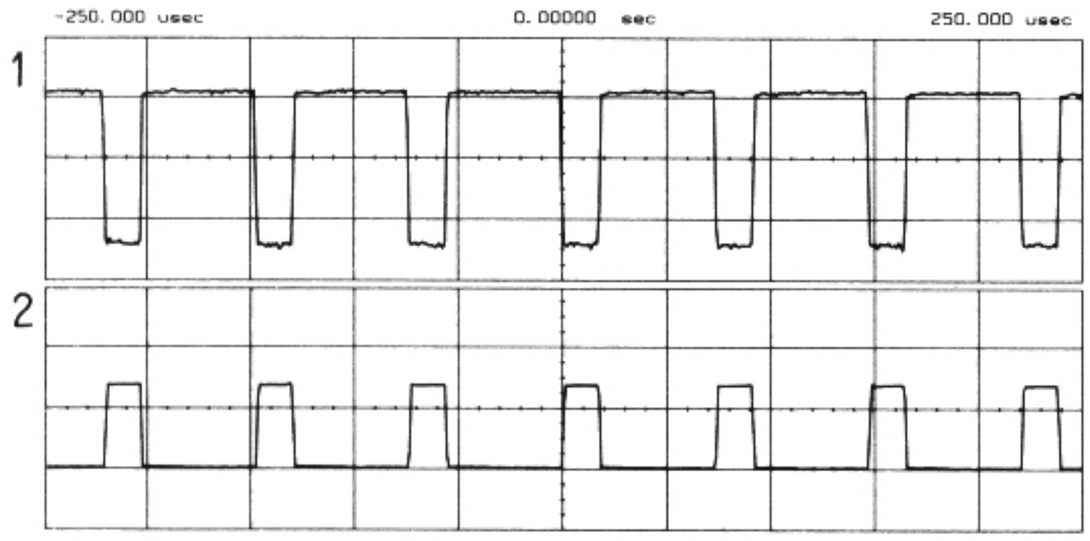


AB0: AB tray interconnection

1
2

BOARD : AB1

TEST POINT : PLF2 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC12 pin 14 for Ch. 2

PROCEDURE :

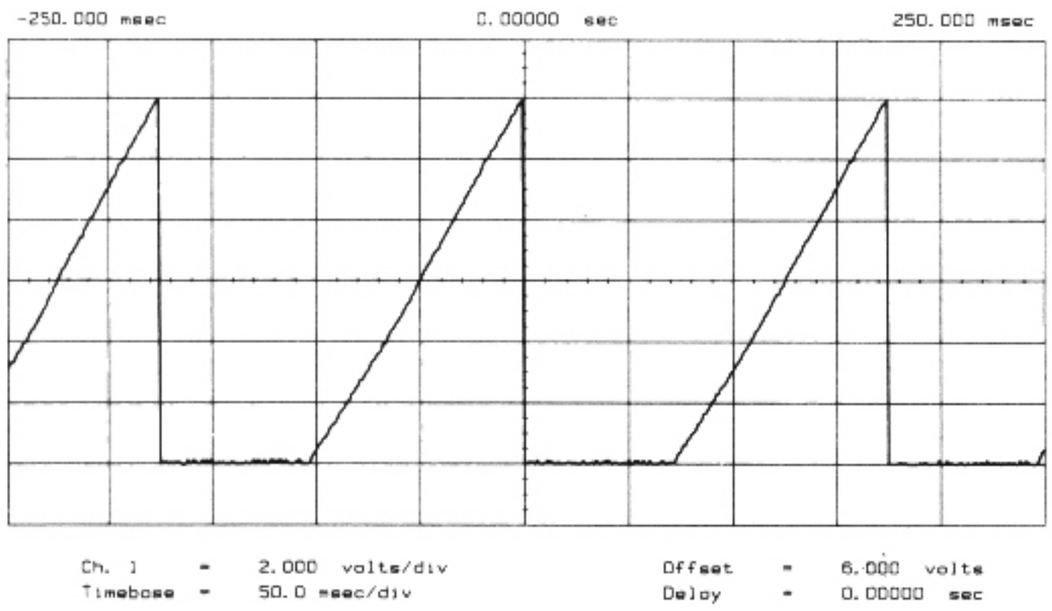
1. Press PRESET the select the following 2382 setting:

Span	5 kHz/DIV

3

BOARD : AB1

TEST POINT : TP4
SCOPE SETTING [DEFAULT]



PROCEDURE :

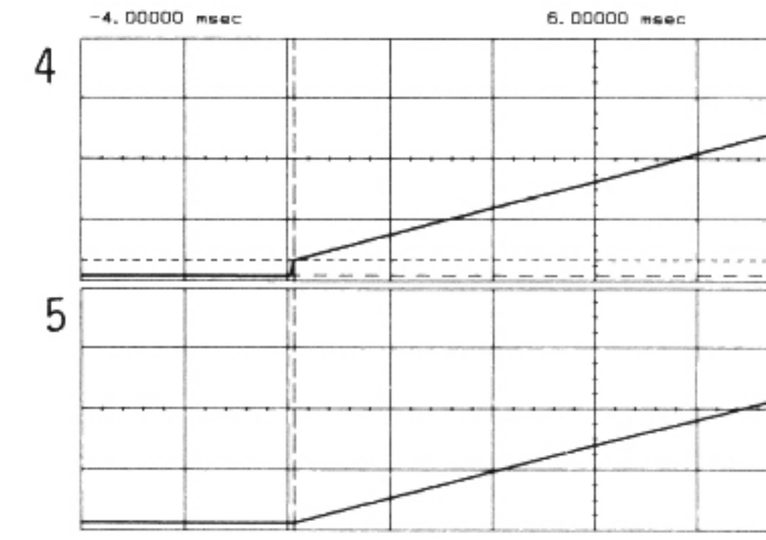
1. Press PRESET then select the following 2382 setting:

Span	20 MHz/DIV

4
5 *

BOARD : AB1

TEST POINT : TP4 (Fig. 14) for Ch. 1
SCOPE SETTING



TEST POINT : TP6 (Fig. 15) for Ch. 2

PROCEDURE :

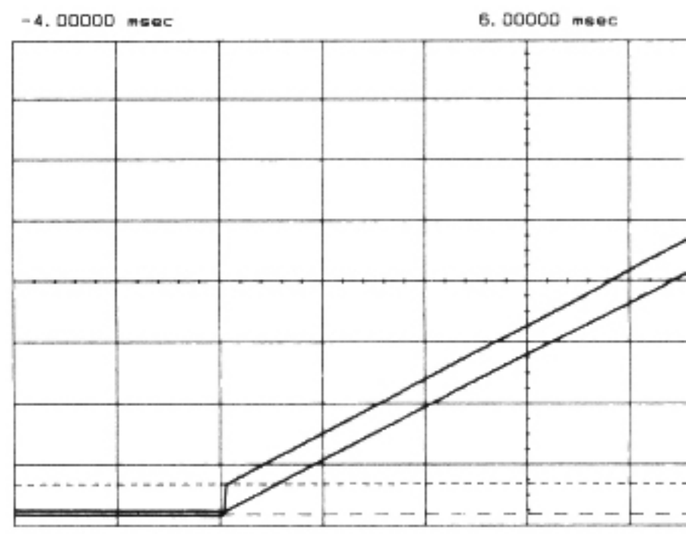
1. Press PRESET then select the following

Span	200 kHz/

6
7 *

BOARD : AB1

TEST POINT : TP4 (Fig. 14) for Ch. 1
SCOPE SETTING [DEFAULT]

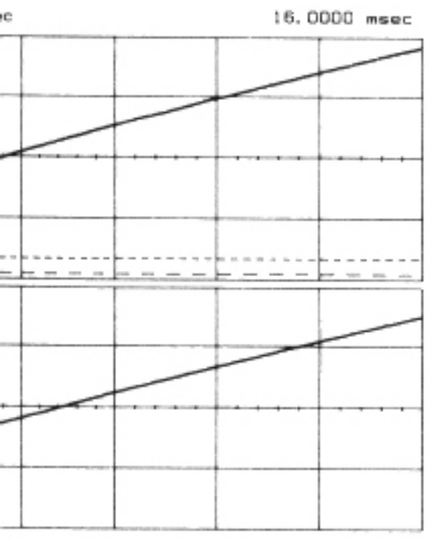


TEST POINT : TP6 (Fig. 15) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following

Span	200 kHz/



owing 2382 setting:

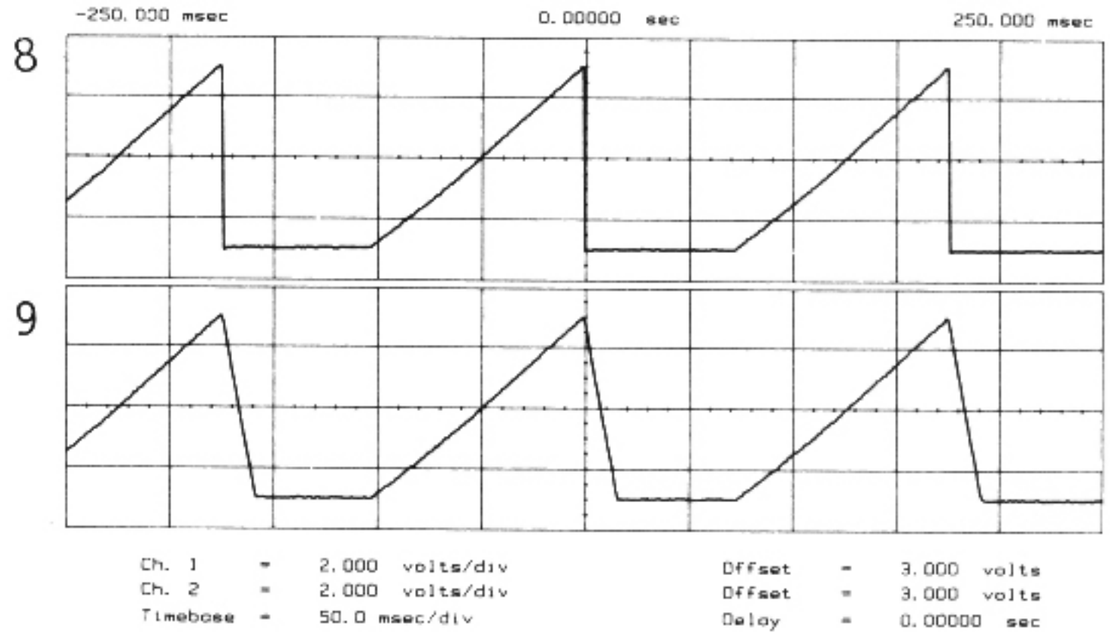
kHz/DIV

cct. drg. Fig. 15 refers

8 BOARD : AB1

9 *

TEST POINT : TP5 (Fig. 14) for Ch. 1
SCOPE SETTING [DEFAULT]



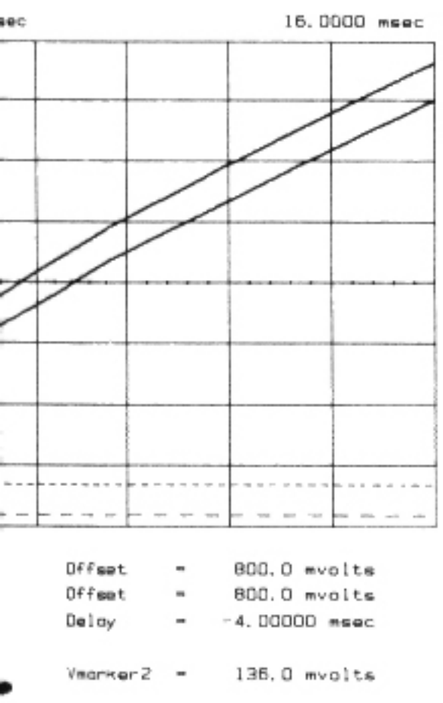
TEST POINT : TP7 (Fig. 15) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 setting.

Span	20 MHz/DIV

cct. drg. Fig. 15 refers



6 Ch. 1
7 Ch. 2

owing 2382 setting:

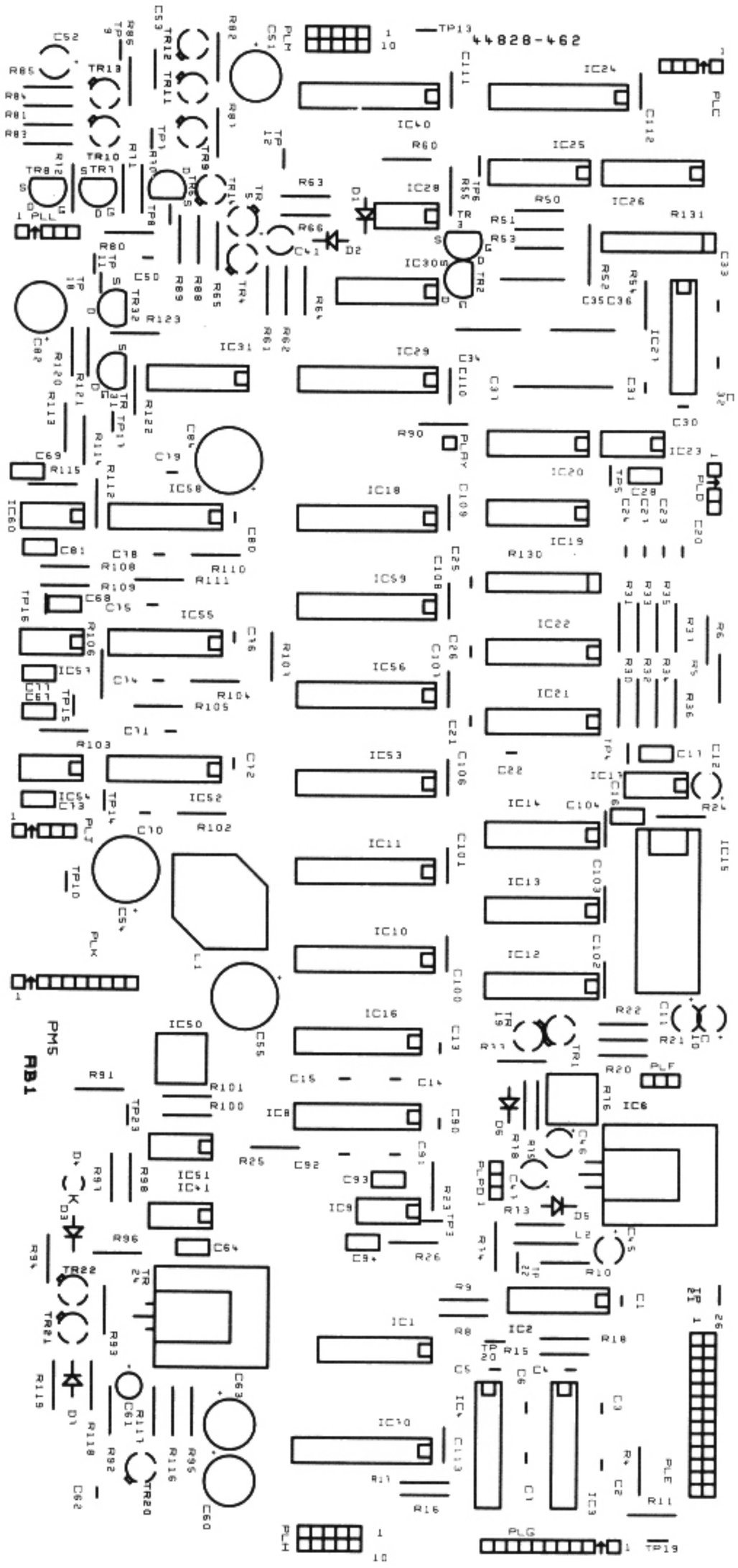
kHz/DIV

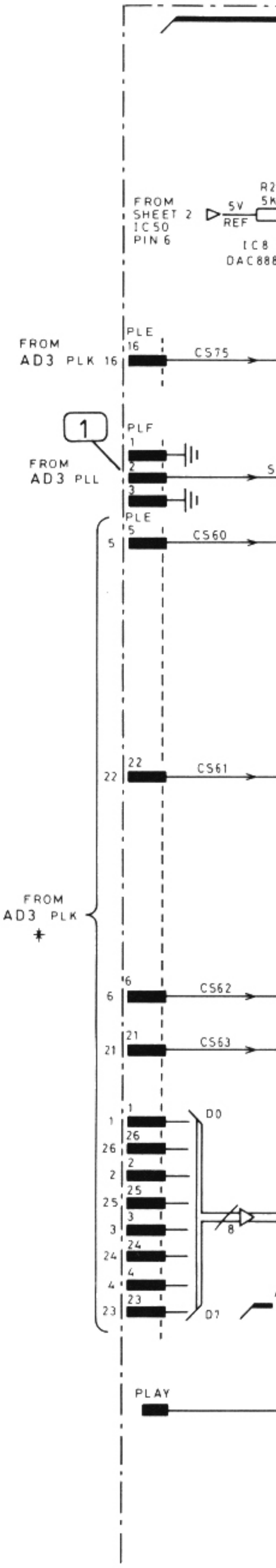
cct. drg. Fig. 15 refers

rms for AB1

Fig. 14a

May 86





Drg. No. Z44
Sh. 1 Iss

Component layout for AB1

Fig. 14

May 86

SET SWEEP D TO A GAIN

SWEEP D TO A

STEP D-TO-A

FROM SHEET 2 IC50 PIN 6

5V REF

R25 5K1

IC8 DAC888

8 BIT D-A

VREF(+)

VREF(-)

CE

D0

D7

C90 100n

C91 100n

C92 10n

C93 47p

R26 8K2

C94 100p

IC9 NE5534

+15V

-15V

+5V

-5.5V

C12 1µ0

C11 1µ0

C10 1µ0

IC15 DAC80

12 BIT D-A

OFFSET COMMON

REF IN LSB

SCALING NETWORK

I OUT

REF OUT MSB

R24 1K2

C13 100n

C14 100n

R23 51K

8 BIT D

FROM AD3 PLK 16

PLE 16

CS75

1

PLF 1

2

3

FROM AD3 PLL

SWEEP CLOCK

R22 5K1

R21 16K

R20 20R

TR1 BC239

TP 3

2

IC12 LS191

IC13 LS191

IC14 LS191

CLK

LOAD

RIPPLE CLK

DN/UP

EN A B C D

IC10 LS273

IC11 LS273

LATCH

DOWN / UP

LOAD

PLE 5

5

CS60

22

CS61

FROM AD3 PLK

6

CS62

21

CS63

1

26

2

25

3

24

4

23

D0

D7

8

QUIET DATA BUS

AUTO-TEST RESET

R90 4K7

PLAY

A

R11 100K

T.G. IDENT

INPUT ATTEN. OVERLOAD

PLG 7

PLE 14

PLM 5

PLE 13

FROM AE0 SKA 10

TO AD3 PLK 14

FROM AB8 PLAS 5

TO AD3 PLK 13

SEE CIRCUIT AB0 F

Drg.No. Z44828-462D

Sh.1 Iss.1

STEP D-TO-A | SUMMER | SWEEP ATTENUATOR | BUFFER

PART OF AB1
44828-462D

R24 1K2

C17 47p

IC17 5534

+15V

C16 100p

IC21(a) SD5002

÷1

IC23 5534

+15V

C28 100p

8 AD3

TP5

+5V

C13 100n

-5.5V

C14 100n

C15 10n

R23 51K

8 BIT D-A

VREF(+)

VREF(-)

CE

IC16 DAC888

D0

D7

TP4

-15V

3

4

6

AD3

R30 10K

R31 4K99

R32 2K52

R33 499R

R34 750R

R35 252R

R36 499R

R37 499R

IC21(b) ÷2

IC21(c) ÷4

IC21(d) ÷8

IC22(a) SD5002 ÷10

IC22(b) ÷16

IC22(c) ÷20

IC22(d) ÷40

QUIET DATA BUS

TWO

TO SHEET

+20V

IC19(a) LM348

R1 30(a) 220K

C20 10n

5.5V

IC19(b)

R1 30(b)

C21 10n

IC19(c)

R1 30(c)

C22 10n

IC19(d)

R1 30(d)

C23 10n

IC20(a) LM348

R1 30(e)

C24 10n

IC20(b)

R1 30(f)

C25 10n

IC20(c)

R1 30(g)

C26 10n

IC20(d)

R1 30(h)

C27 10n

IC18 LS273

CLK

LATCH

R

A

Vb FROM SHEET 2

✳ SEE CIRCUIT AB0 FOR CONNECTION DETAILS

AB1

AB1 : D-A converter

(Refer to Fig. 14a for published waveforms)

Fig. 15

May 86

PART OF
AB1
44828-462D

FROM AD3 PLK 7
PLE 7
CS64

FROM AD3 PLK 20
PLE 20
CS65

SWEEP INTEGRATOR

5
7
TP6

IC25 (a) µA339
IC25 (b)
IC25 (c) µA339
IC26 (a) LM348
IC26 (b)
IC26 (c)
IC26 (d)
+15V
-15V
+20V
-5·5V
Vb
R131 (a) 220K
R131 (b)
R131 (c)
R131 (d)
C30 10n
C31 10n
C32 10n
C33 10n

IC24 LS273
CLK
LATCH
R
D0
D7

R50 1M0
R51 1M0
R52 510K
R53 56K
R54 5K1
R55 470R
TR2 TIS74
TR3 TIS74
IC27(a)
IC27(b) SD5002
IC27(c)
IC27(d)
C34 2µ2
C35 2µ2
C36 1µ0
C37 5µ6

IC28 TL071
R60 4K7
D1 IN4148
R63 4K7

IC29 LS27

FROM SHEET ONE
QUIET DATA BUS
CS65

PRECISION VOLTAGE REFERENCE

IC51(a) LM358
IC51(b)
R100 27K
R101 12K
V REF
(+5V) SHEET 3
Vb
(+1·5V)

IC50 REF 02
VOLT REF
5V REF.

C70 100n
C71 100n
C72 10n
R102 2K0
IC52 DAC08HP
8 BIT D-A
V+
V- COMP
V REF(+)
V REF(-)
LSB
MSB
IO
VLC
IC53 LS273

REFERENCE LEVEL VOLTAGE GENERATOR

C67 47p
R103 5K0
C73 100p
IC54 5534
TP15
R106 320K
C74 100n
C75 100n
C76 10n
R104 2K0
R105 2K0
IC55 DAC08HP
IC56 LS273
R107 1K0
C84 470µ

C68 47p
R109 5K0
C77 100p
IC57 5534
R108 5K1
C78 100n
R110 1K0
R111 2K0

CS72
CS71
CS70
PLE 10
PLE 18
PLE 9
FROM AD3 PLK 10
FROM AD3 PLK 18
FROM AD3 PLK 9

Drg. No. Z44828-462D
Sh.2 Iss.5

AB1 : D-A converter

FROM AD3 PLK 20

PLE 20

CS65

RATE LIMITER

SWEEP SELECTOR

X1/X5 AMPLIFIER

IC28 TL071

R60 4K7

D1 IN4148

D2 IN4148

R61 33K

R62 3K0

R63 4K7

R64 1K8

TR4 BC239

R65 220R

C41 1µ0

TR5 BC239

R66 4K7

+15V

-15V

9

TP7

TR6 TIS74

R70 1M0

TP8

C50 100n

R80 1K0

TR9 BC449

TR10 BC449

R81 1K0

R83 10k

R84 2K0

R85 560k

TR13 BC449

C52 22µ

TR11 BC449

TR12 BC449

R82 75K

C51 22 µ

+70V FROM SHEET 3

TP9

H.F. OSC. SWEEP

R86 12K

C53 33p

R87 3K0

R88 5K1

TR14 BC449

R89 12K

PLC 4

FROM AA7 PLP 3 VIA AA5 PLE 3

IC30 (a) µA339

IC30 (b)

IC30 (c)

Vb

TR7 TIS74

TR8 TIS74

R71 1M0

R72 1M0

TP10

TP11

L.F. MASTER OSC. SWEEP

L.F. INTERPOLATION OSC. SWEEP

PLJ 1

PLJ 4

TO AB3 PLX 5

PLL 4

TO AB2 PLN 3

IC29 LS273

CLK LATCH R

D0

D7

8

SET T.G. L.F. RESPONSE

PLG 11

TO AE6 PLT 5

IC31 (a) µA339

IC31 (b)

TP13

REF FREQ. VOLTAGE ENABLE TO H.F. MASTER OSC.

PLC 5

TO AA4 PLF 3

TP14

REF FREQ. VOLTAGE ENABLE TO L.F. MASTER OSC.

PLJ 5

TO AB3 PLX 4

E LEVEL VOLTAGE GENERATOR

C68 47p

R109 5K0

C77 100p

IC57 5534

R108 5K1

TP16

R112 320K

C69 100p

R115 5K0

C81 100p

IC60 5534

R114 5K1

TP12

INTERP. OSC. SWEEP ATTEN CONTROL

PLL 5

TO AB2 PLN 4

TP17

R113 100R

REF FREQUENCY VOLTAGE

PLC 3

TO AA4 PLF 4

PLJ 3

TO AB3 PLX 3

SWITCHED FILTER

TP18

R122 1K0

REF FREQ

TR32 TIS74

C82 47µ

R123 1M0

R121 240R

TR31 TIS74

R120 1M0

PLL 3

2

1

TO AB2 PLN

C76 10n

C78 100n

C79 100n

C80 10n

IC55 DAC08 HP

IC58 DAC08HP

R110 1K0

R111 2K0

8 BIT D-A

V+ V- COMP

V REF (+) V REF (-) LSB MSB VLC

R107 1K0

C84 470 µ

IC56 LS273

IC59 LS273

IC31 (c)

IC31 (d)

REF FREQ. ENABLE FOR L.F. INTERP. OSC.

CS70

QUIET DATA BUS

TO SHEET THREE

PLE 9

FROM AD3 PLK 9

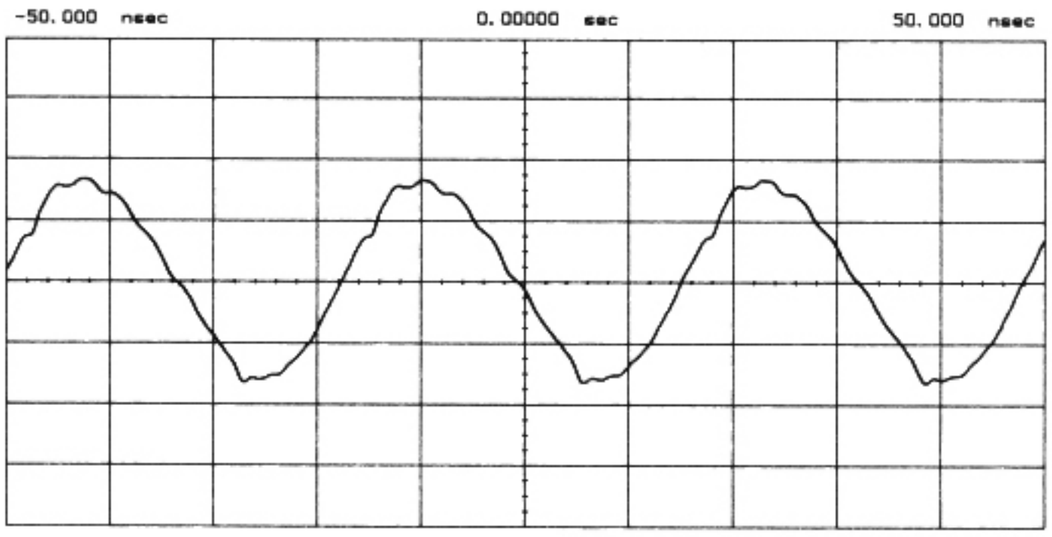
✳ SEE CIRCUIT AB0 FOR CONNECTION DETAILS

A converter

AB1

1 BOARD : AB3

TEST POINT : TP1
SCOPE SETTING [DEFAULT]



Ch. 1 = 200.0 mvolts/div
Timebase = 10.0 nsec/div
Offset = -2.300 volts
Delay = 0.00000 sec

PROCEDURE :

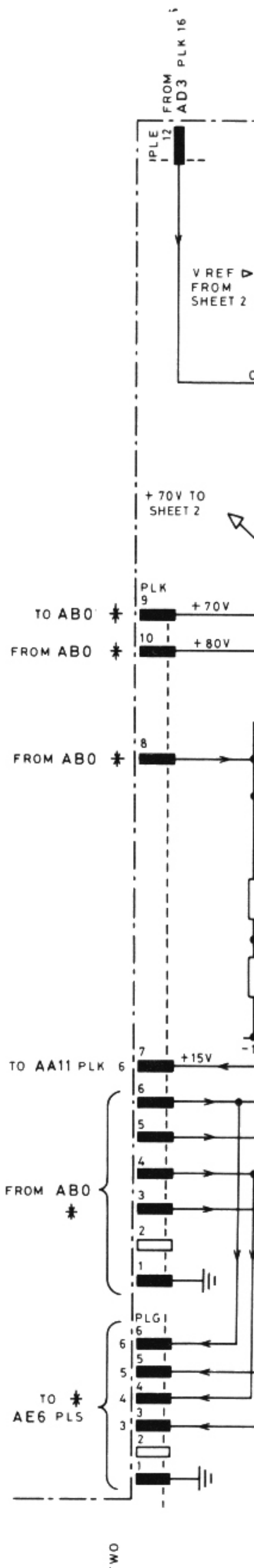
1. Press PRESET.

Waveform for AB3

(Refers to Fig. 17)

Fig. 16

May 86



FROM AD3 PLK 16

FROM AD3 PLK 11

T.G. OUTPUT LEVEL D-A

+5V

-5·5V

C5 100n

C6 100n

C7 10n

IC4 DAC888

IC2(d) LM348

R17 10K

V REF FROM SHEET 2

V REF(+)

8 BIT D-A

V REF(-)

CE

R18 20K

CS76

D0

D7

8

SET I.F. GAIN D-A

+5V

-5·5V

C4 100n

C3 100n

C2 10n

IC3 DAC888

IC2(c) LM348

TP20

R16 10K

V REF FROM SHEET 2

R15 20K

CS74

+70V TO SHEET 2

PLK 9

TO AB0

+70V

10

FROM AB0

+80V

R91 100R

C60 22µ

C62 100n

+15V REGULATOR

+70V CURRENT LIMIT

+70V REGULATOR

D5 IN4148

+20V

IC6 LM317

TP22

8

FROM AB0

L2

C45 10µ

D6 1N4148

R75 240R

C47 10µ

R73 24K

C46 10µ

R78 100R

SET +15V

R76 500R

R74 12K

1 PLPD

2

3

TR19 BC209C

R77 2K4

-15V

TR20 BC450

R95 7R5

TR24 TIP112

TP23

R116 10K

R93 10K

R117 33K

+5V

C64 100p

+15V

IC41 5534

TR22 BC449

R96 2K7

D7 1N4148

R118 20K

C61 2µ2

TR21 BC 449

D3 1N4148

R92 1K2

R119 20K

R94 3K0

D4 TIL209

-5·5V

-15V

WHEN D4 'ON' 70V LINE OUT OF REGULATION

TO AA11 PLK 6

7 +15V

6 +15V

5 L1 350µ +5V

4 -5·5V

3 -15V

2

1

FROM AB0

C54 220µ

C55 220µ

PLG

6

5

4

3

2

1

TO AE6 PLS

SUPPLY LINE TABLE			
IC	-5·5V	+5V	GROUND
IC10		20	10
IC11		20	10
IC12		16	8
IC13		16	8
IC14		16	8
IC18		20	10
IC21	2		
IC22	2		
IC24		20	10
IC27	2		
IC29		20	10
IC40		20	10
IC53		20	10
IC56		20	10
IC59		20	10
IC70		20	10

ALL IC'S TO BE DECOUPLED AT +5V PIN TO GROUND (EXCEPT 21, 22, 27) WITH 10n CAPACITOR

V REF (+5V) FROM SHEET 2

FROM SHEET TWO

8 QUIET DATA BUS

✱ SEE CIRCUIT AB0 FOR CONNECTION DETAILS

Drg.No. Z44828-462D
Sh.3 Iss.2

AB1 : D-A converter

PART OF
AB1
44828-462D

FROM AD3 PLK 17
PLE 17
CS73

R4 100R
TP19
0V TO 10V
TO LEVEL CONTROL
PLG 8
TO AE6 PLT4

IC2(c) LM348
TP20
R15 20K
R5 100R
0V TO 10V
GAIN ADJUST
PLD 4
TO AC3 PLH9
2
1
3
TO AC3 PLH6

+5V
IC1 AD7524
VREF FROM SHEET 2
VDD
VREF
CS
WR
IO
D0
D7
IC2(b) LM348
R8 10K
R9 300K
-15V
+15V
IC2(a) LM348
TP21
R6 100R
CENTRE FREQ.ADJUST
1·0V TO 11·0V
R10 20K
C1 100n

C63 22µ
+70V REGULATOR

OSCILLATOR CONTROL LATCH

T.G. OFF (L)
PLG 10
TO AE6 PLT3

TR24
IP112
TP23
C64 100p
IC41 5534
R96 2K7
R97 130K
R98 10K
D3 1N4148
D4 TIL209
R22
C449

PLH 1
TO AA4 PLF6 VIA AA5 PLD8

CS66
IC70 LS273
CLK
LATCH
R
H.F. MASTER SG DRIVE ON (H)
LOOP CLOSED / PHASE LOCKED (L)
L.F. MASTER OSC. PHASE LOCK ON (L)
SELECT H.F. MASTER (L)
SELECT L.F. MASTER (L)
SELECT INTERP OSC. (L)
TO AA4 PLF5
TO AB4 PLAM5
TO AB7 PLAA

PLG 9
SELECT T.G. CAL. DETECTOR (L)
TO AE6 PLT2

INPUT ATTEN. LATCH

CS67
IC40 LS273
SELECT 10dB PAD (H)
SELECT 20dB PAD (H)
SELECT 30dB PAD (H)
SELECT 3dB PAD (H)
SELECT SWITCH A (H)
SELECT SWITCH B (H)
SOLENOID CHANGE (L)
OVERLOAD CLEAR (L)
PLM
TO AB8 PLAS

V REF (+5V) FROM SHEET 2

'ON' 70V LINE REGULATION

PLE 8 19
FROM AD3 PLK 8
FROM AD3 PLK 19

AB1

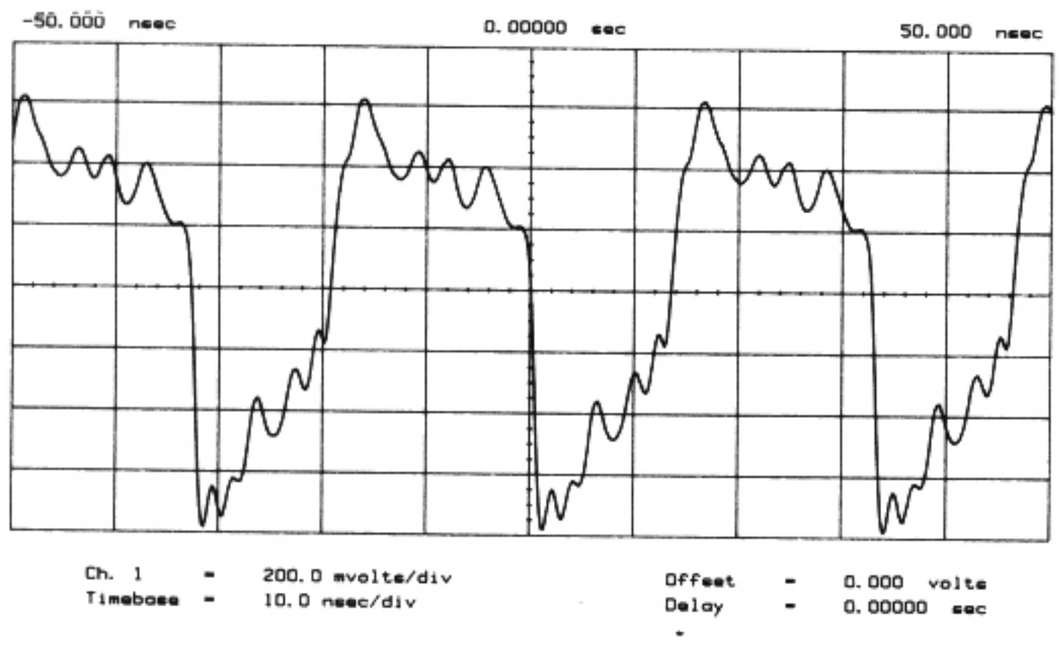
converter

Fig. 16
Chap. 7
Page 39

(See Fig. 16 for waveform 1)

2 BOARD : AB3

TEST POINT : TP2
SCOPE SETTING [DEFAULT]

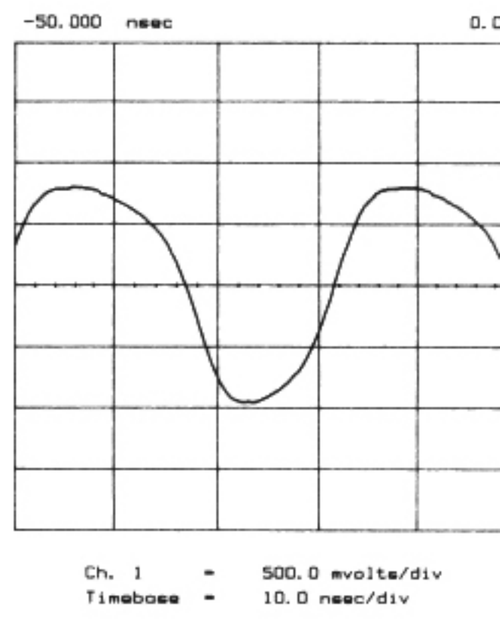


PROCEDURE :

1. Press PRESET.

4 BOARD : AB4

TEST POINT : TP1
SCOPE SETTING [DEFAULT]

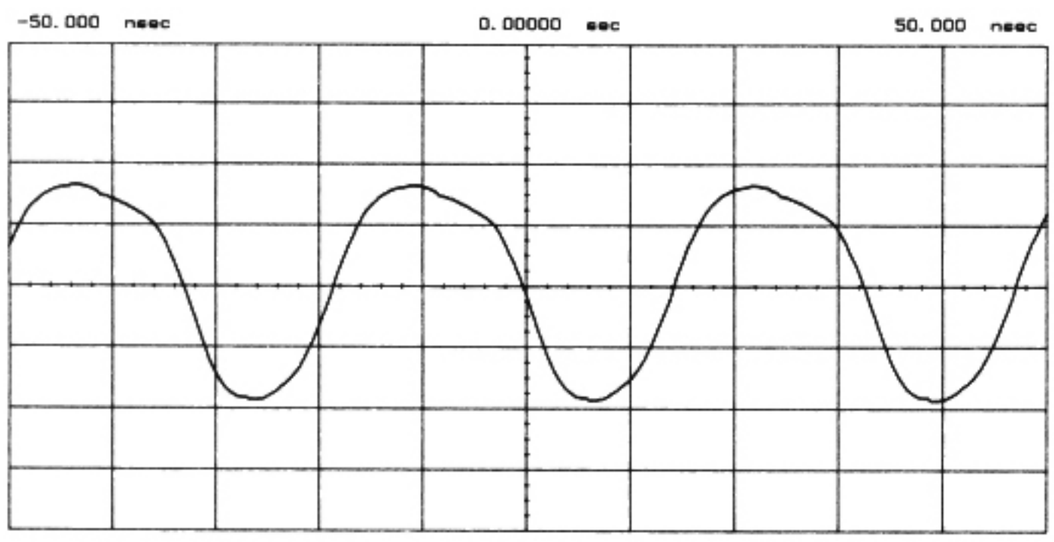


PROCEDURE :

1. Press PRESET.

3 BOARD : AB3

TEST POINT : TP3
SCOPE SETTING [DEFAULT]

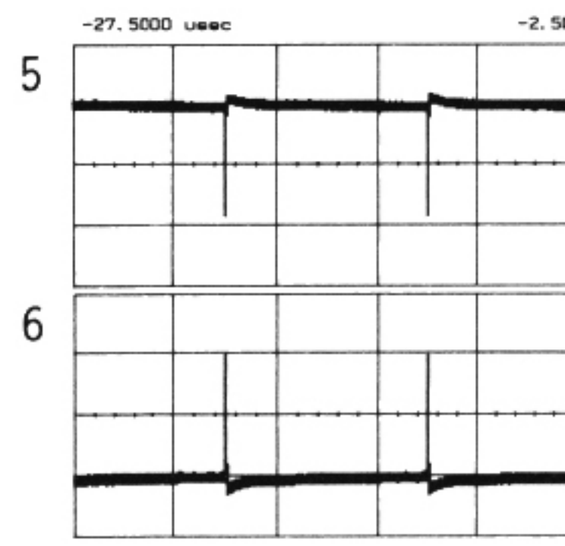


PROCEDURE :

1. Press PRESET.

5
6 BOARD : AB4

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP3 for Ch. 2

PROCEDURE :

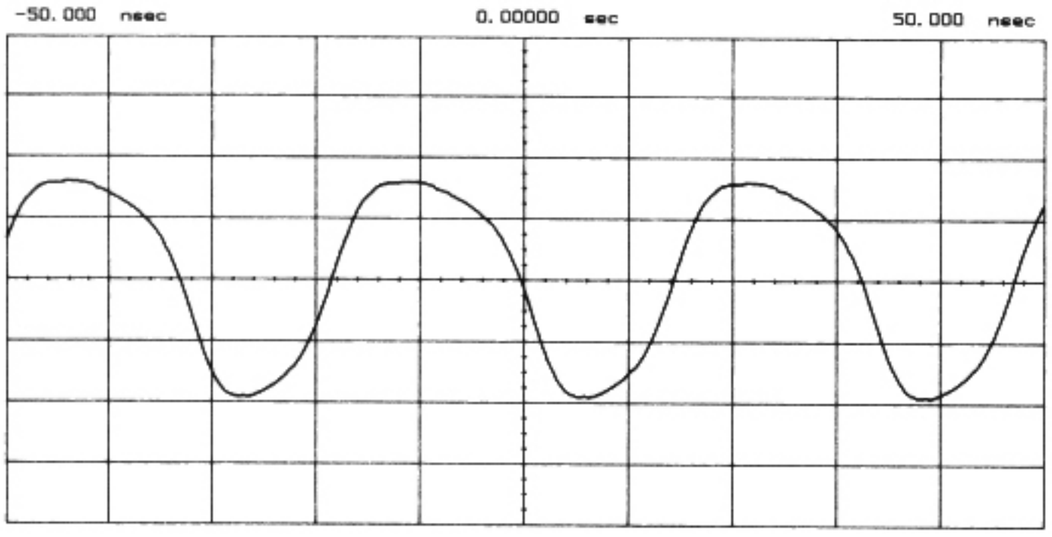
1. Press PRESET.

Note. Traces obtained at TP6 and TP

Fig. 17a
Chap. 7
Page 40

4 BOARD : AB4

TEST POINT : TP1
SCOPE SETTING [DEFAULT]

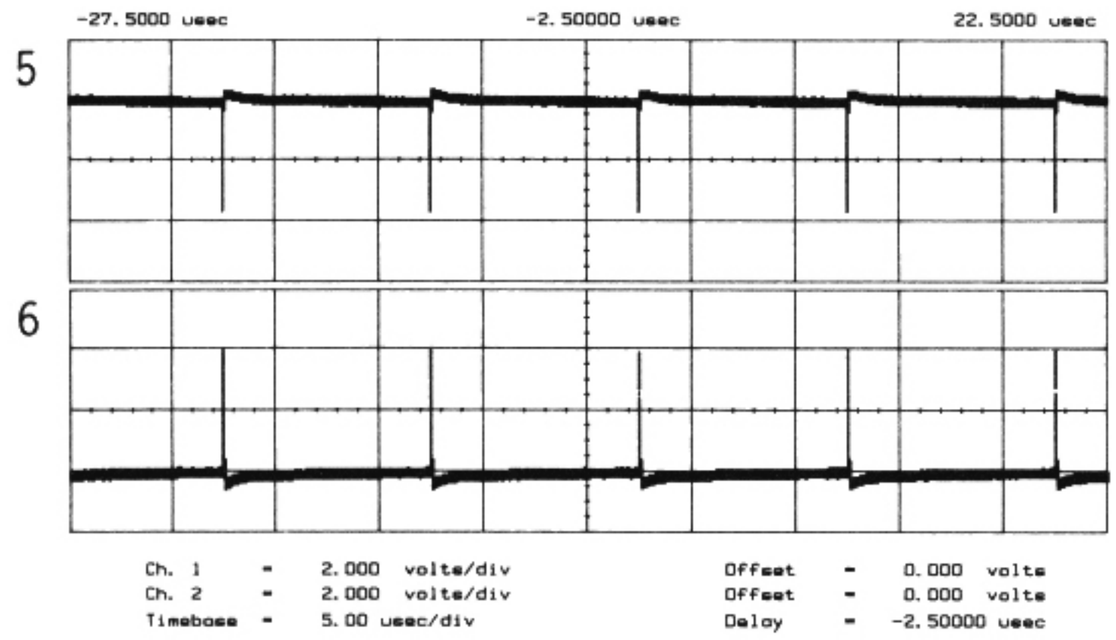


PROCEDURE :

1. Press PRESET.

5 BOARD : AB4
6

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP3 for Ch. 2

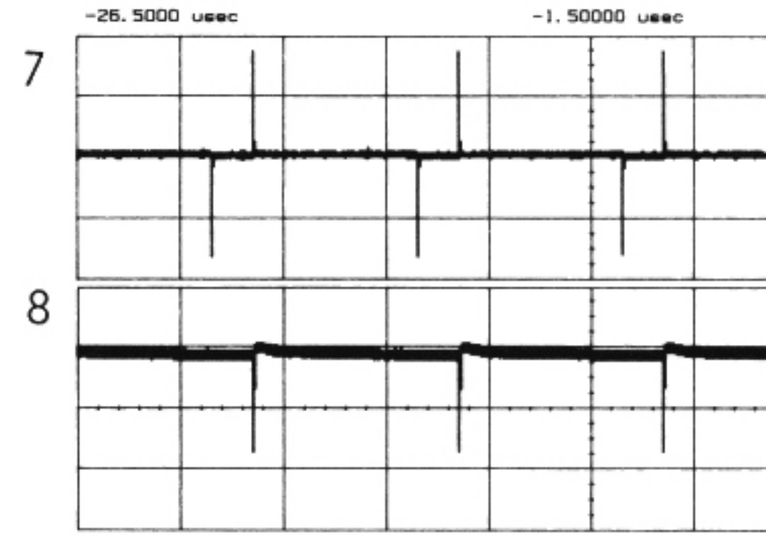
PROCEDURE :

1. Press PRESET.

Note. Traces obtained at TP6 and TP7 should be the same as TP2 and TP3.

7 BOARD : AB4
8

TEST POINT : TP4 for Ch. 1
SCOPE SETTING [DEFAULT]



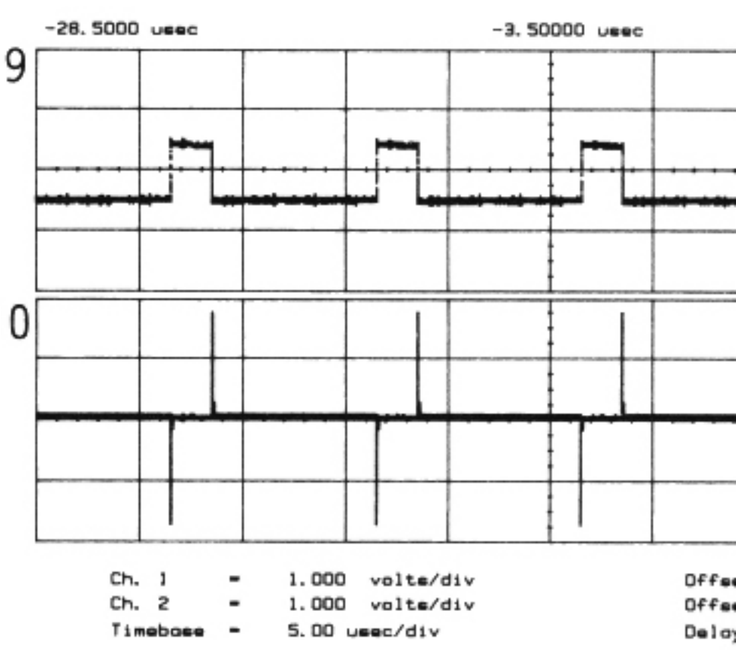
TEST POINT : TP2 for Ch. 2

PROCEDURE :

1. Press PRESET.

9 BOARD : AB4
10

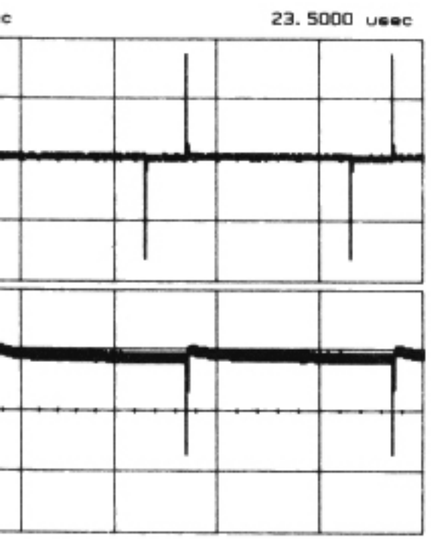
TEST POINT : TP11 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP4 for Ch. 2

PROCEDURE :

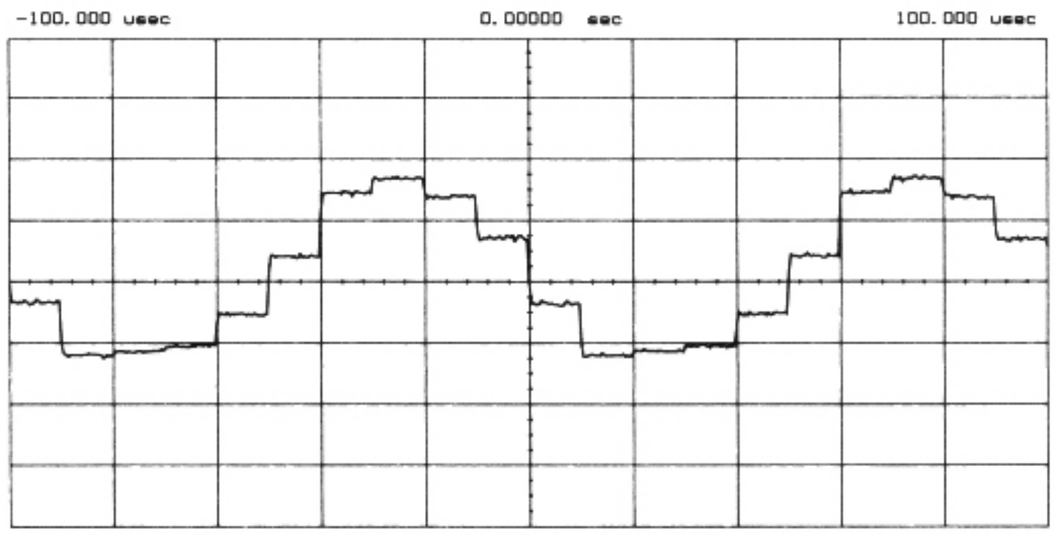
1. Press PRESET.



Offset - 0.000 volts
Offset - 0.000 volts
Delay - -1.50000 usec

11 BOARD : AB4

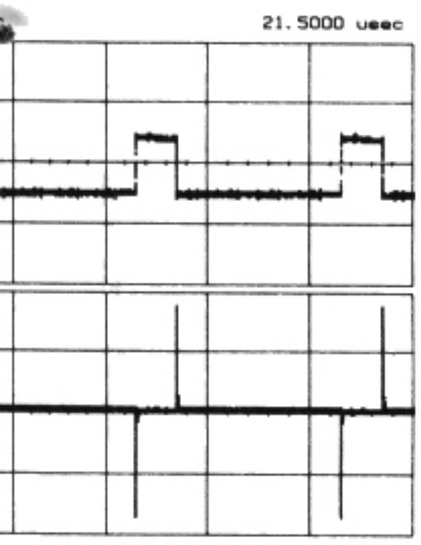
TEST POINT : TP5
SCOPE SETTING [DEFAULT]



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 0.00000 sec

PROCEDURE :

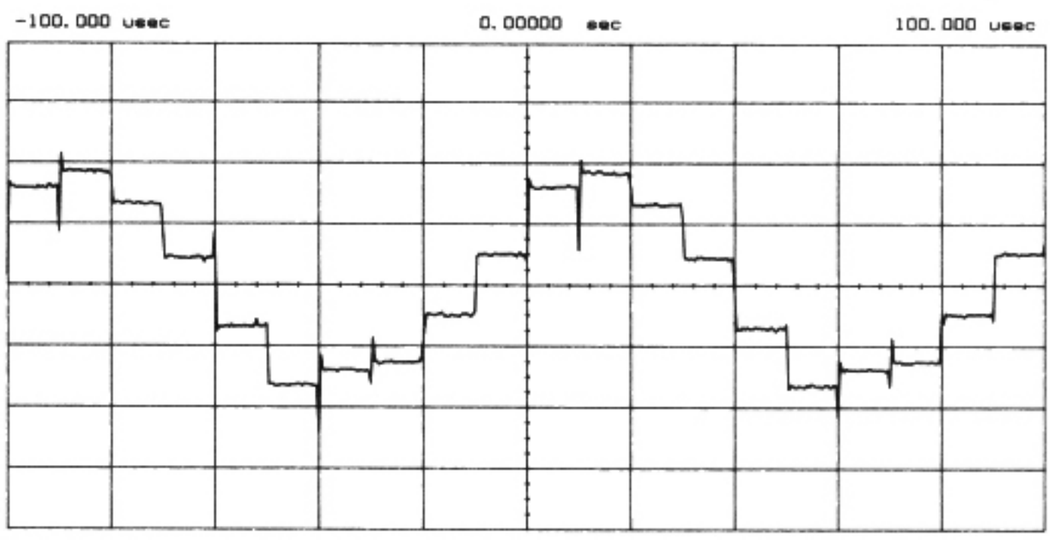
1. Press PRESET then disconnect PLY from board AB3.
2. Inject 30.01 MHz at 10 dBm into board AB4 through SLY.



Offset - -1.100 volts
Offset - 0.000 volts
Delay - -3.50000 usec

12 BOARD : AB4

TEST POINT : TP8
SCOPE SETTING [DEFAULT]



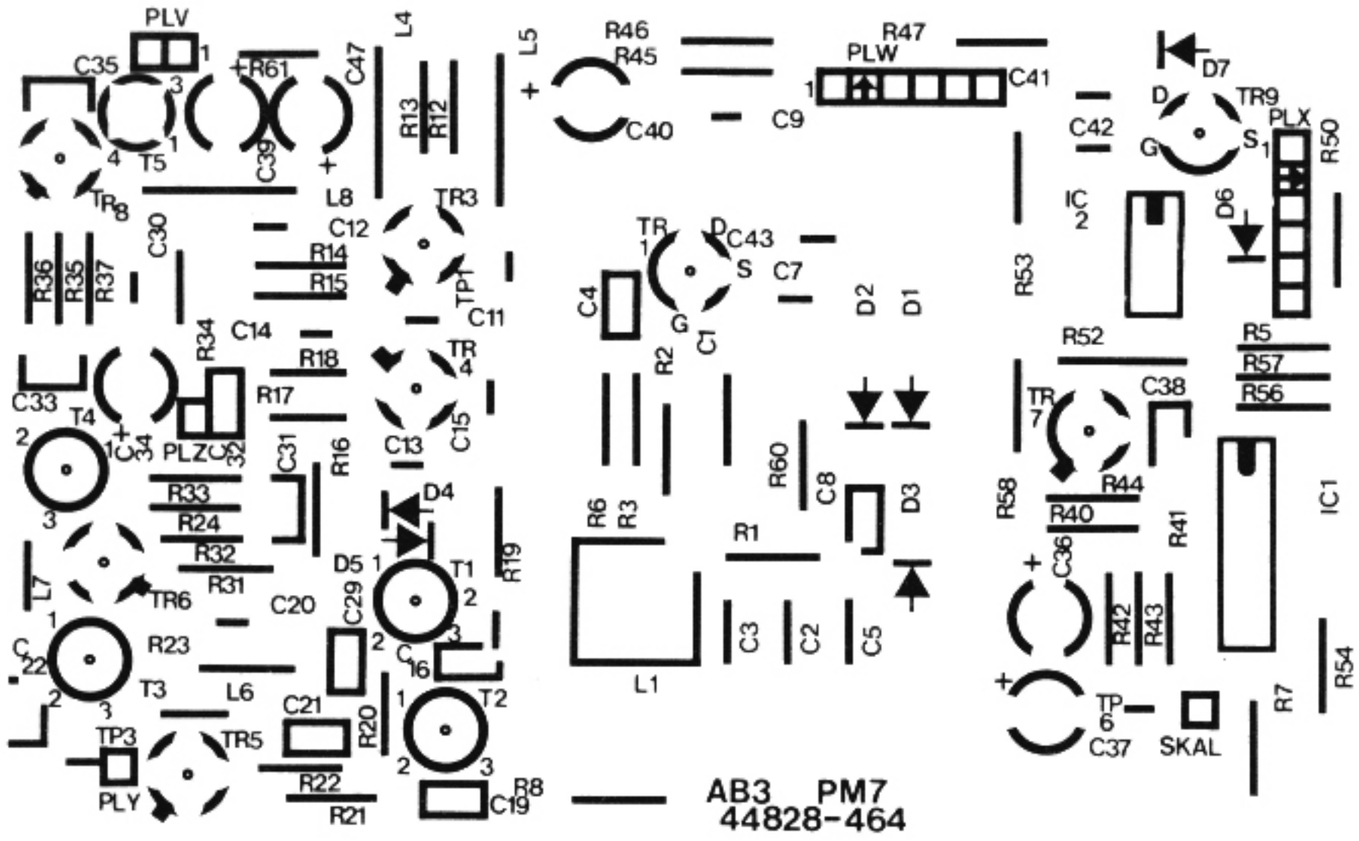
Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 0.00000 sec

PROCEDURE :

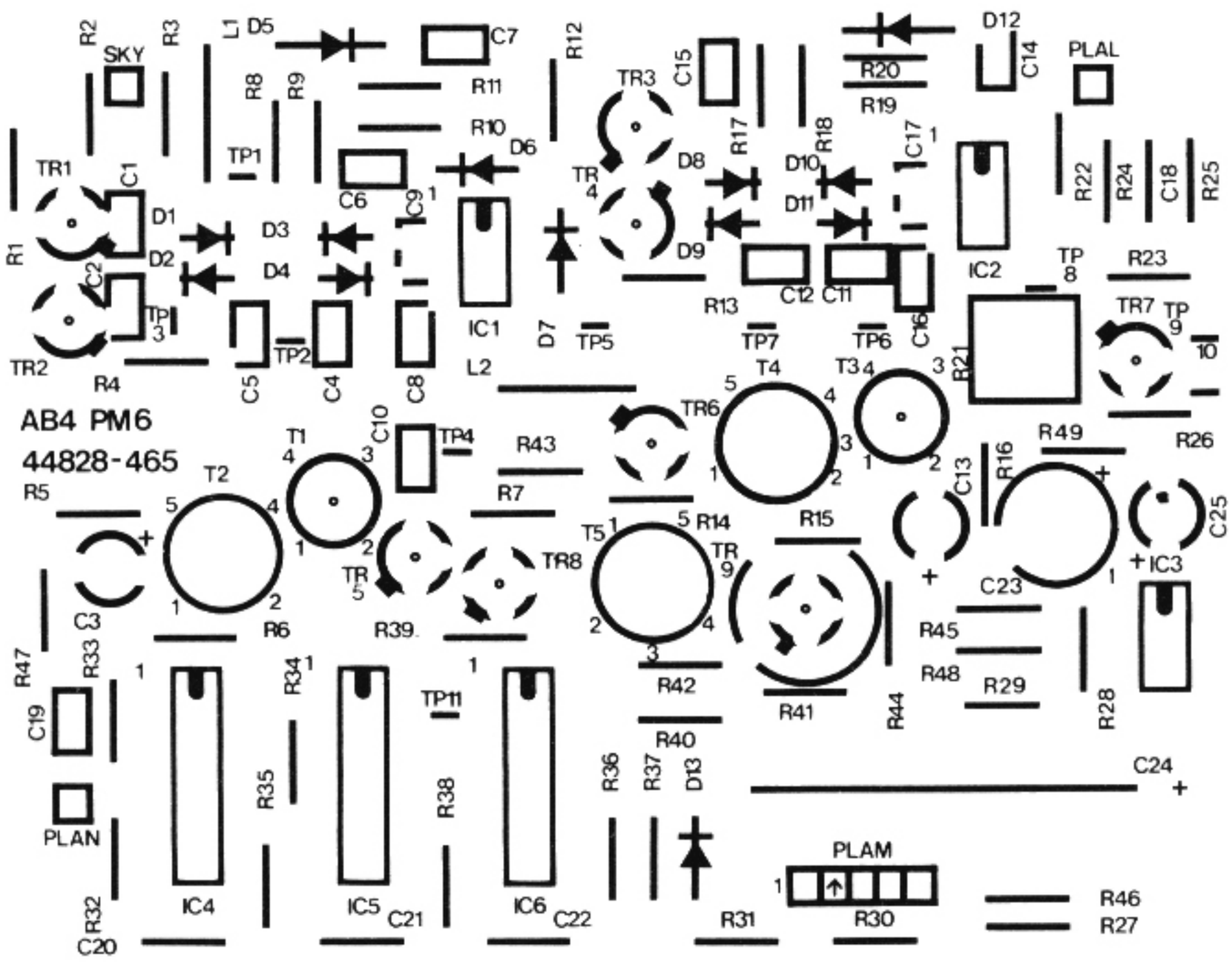
1. Press PRESET then disconnect PLY from board AB3.
2. Inject 30.01 MHz at 10 dBm into board AB4 through SLY.

Fig. 17a

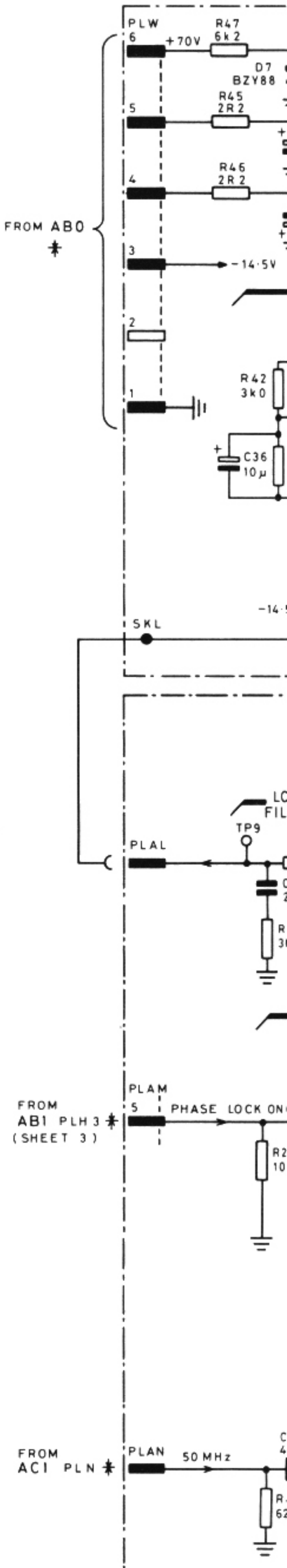
May 86



Component layout for AB3



Component layout for AB4



Drg. No. Z
Sh. 7 I

Fig. 17
May 86

FROM AB0 ✱

PLW
6 +70V R47 6k2 → +20Vd
D7 BZY88
C41 22n
5 R45 2R2 → +4·8V
C40 33µ
4 R46 2R2 → −5·2Vd
C39 33µ
3 → −14·5V
2
1

REGULATOR

IC1 µA723
12 V+ 11 VC
6 13 VREF COMP
4 5
9 V− 7
R42 3k0
C38 100p
R40 8k2
R41 3k6
C36 10µ
R43 3k0
TP6
−12V
C37 33µ
R44 2k0
TR7 BC308
−14·5V

PLX
4 FROM AB1 PLJ 5 — REF. FREQ. ENABLE
3 FROM AB1 PLJ 3 — REF. FREQ. IN
2
1
5 FROM AB1 PLJ 4 — SWEEP
6 TO AB5 PLAK — REF. FREQ. OUT

REF. FREQ. SWITCH
TR9 2N4857
R50 1M0
D6 1N4148

HIGH GAIN / LOW FREQ. RESPONSE AMP.
IC2(b)
R54 390R
R57 24k
R56 390R
R52 1M0
C42 100n
IC2(a) TL072
+20Vd
−12V

26-34MHz VOLTAGE CONTROLLED OSCILLATOR

R53 2k2
R60 10k
C43 100n
C5 150p
C8 330p
C1 33p
TR1 J310
R1 300k
R2 300k
C2 15p
C3 15p
C4 4n7
R6 1k6
R3 3k9
−12V
D1 BB809
D2
D3 BB809
L1
SET FREQ.
R5 240R
R58 200R
C7 10n
C9 22n
R8 33k
R7 10k

AB3
44828-464P

SKL
PLL CONTROL

SECOND SAMPLING GATE
+4·8Vd
R20 2k7
TP6
R18 5k1
C11 4n7
C15 4n7
D12 5V6
D10 D8
MBD102
D11 D9
C14 4n7
C16 220p
TP7
R17 5k1
C12 4n7
R19 2k7
−5·2V

AB4
44828-465X

BALANCED BUFFER
+4·8Vd
R12 10k
TR3 ZTX108
D6 1N414
D7 1N41
TR4 BC308
R13 10k
−5·2V

SECOND STRETCHER
12
TP8
LOOP FILTER
TP9
PLAL
R24 2k0
R22 680R
C18 220n
R25 360R
R23 1k0
ZERO OFFSET
R49 330R
R21 10k
+4·8Vd
C17 6p8
IC2 TL071
−5·2V

LOOP SWITCH
+4·8Vd +4·8Vd
R28 100k
IC3 LS741
TP10
R26 10k
TR7 ZTX108
PLAM
5
FROM AB1 PLH 3 ✱ (SHEET 3)
PHASE LOCK ON(L)
R27 10k
R29 20k
R30 10k
R31 10k
D13 1N4148
−5·2V

PULSE DRIVER
TR6 MPSL08
R14 200R
T3
T4
R15 200R
R16 1k0
C13 2µ2
−5·2V

÷ 500
÷5 ÷2
IC4 MC10138
÷5
IC5 MC10138
÷2 ÷5
IC6 MC10138
TP11
9
R39 20R
R33 390R
C19 4n7
R32 1k2
C20 10n
R35 1k8
R34 1k8
C21 10n
R36 1k8
C22 10n
R37 1k8
R38 1k8
−5·2V

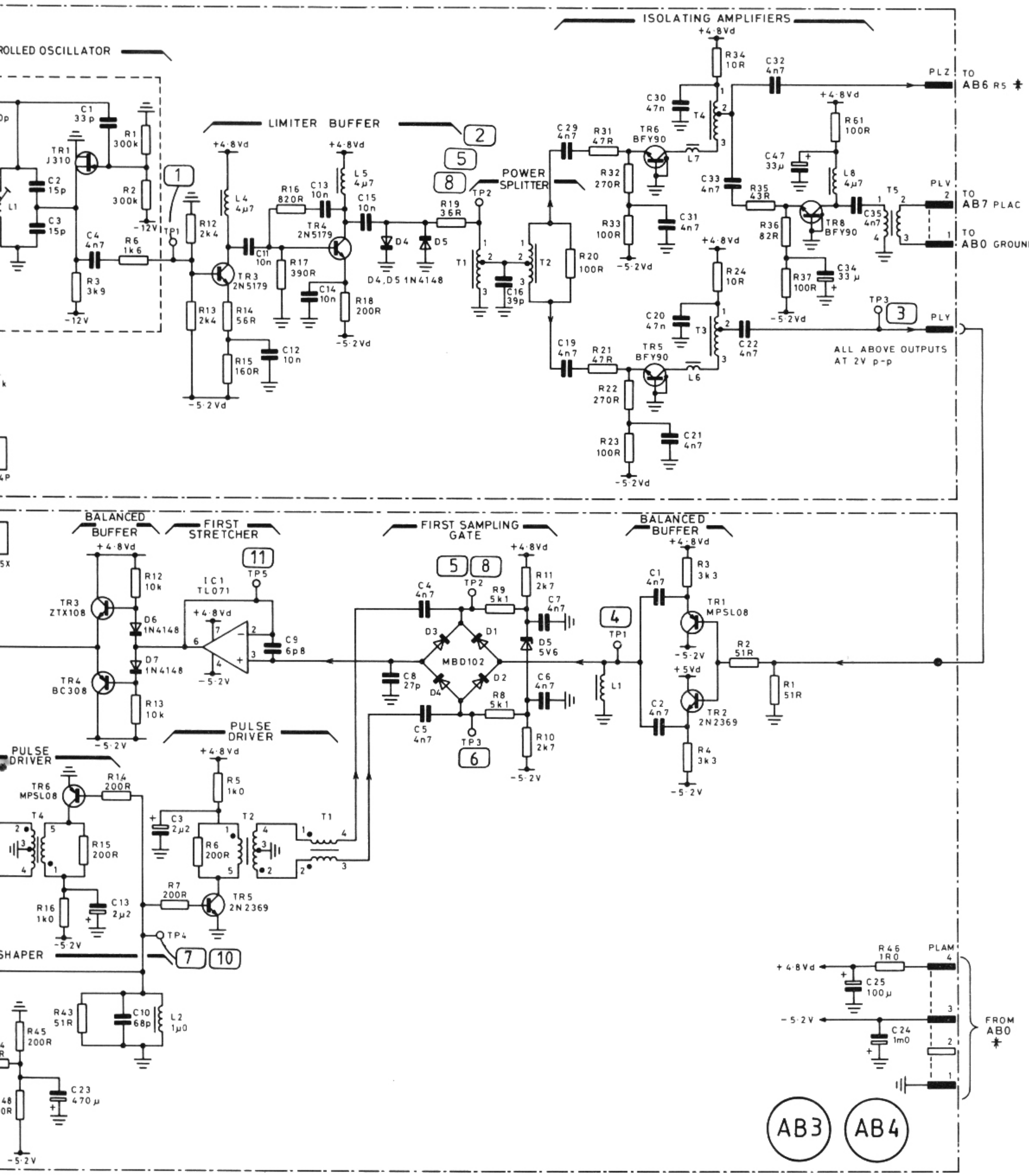
PULSE SHAPER
T5
R43 51R
C10 68p
R45 200R
R44 20R
TR8 BFY90
TR9 BFY90
+4·8V
R40 10R
R42 10R
R41 100R
R48 820R
C23 470µ
−5·2V
−5·2V

FROM AC1 PLN ✱
PLAN 50 MHz
R47 62R

✱ SEE CIRCUIT AB0 FOR CONNECTION

Drg. No. Z44990-450
Sh. 7 Iss. 3 & 1

AB3: Master VCO
AB4: Sampling ga



UIT AB0 FOR CONNECTION DETAILS

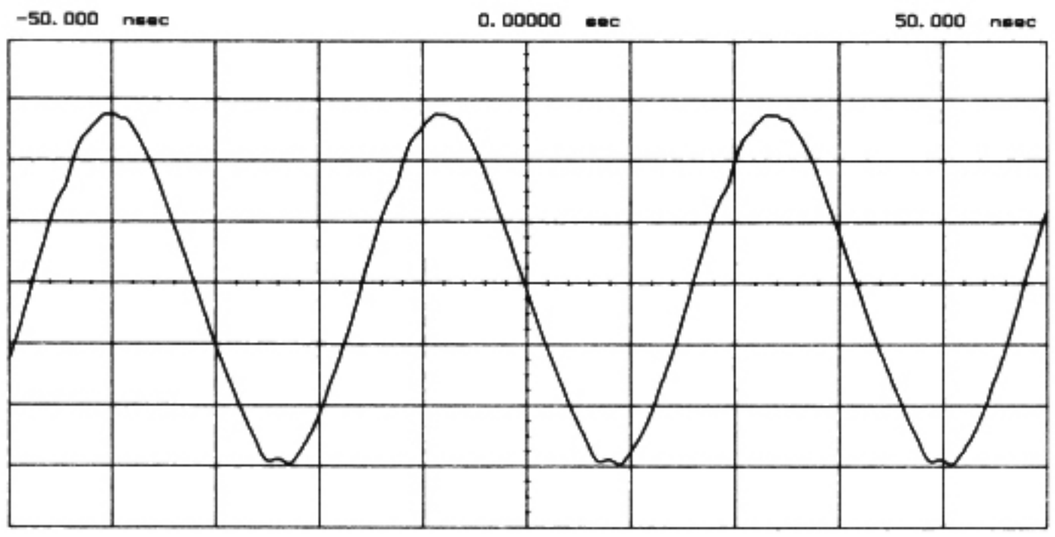
3:Master VCO

4:Sampling gate

Fig. 17
Chap. 7
Page 41

1 BOARD : AB5

TEST POINT : TP1
SCOPE SETTING [DEFAULT]

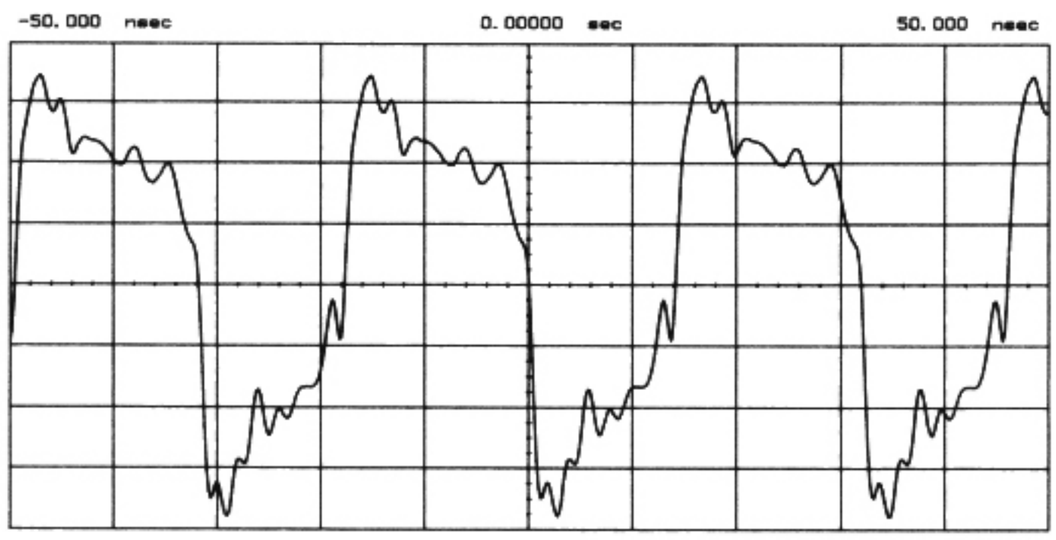


PROCEDURE :

1. Press PRESET.

2 BOARD : AB5

TEST POINT : TP2
SCOPE SETTING [DEFAULT]

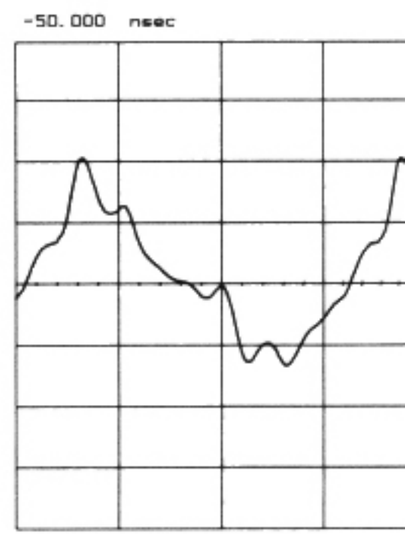


PROCEDURE :

1. Press PRESET.

3 BOARD : AB5

TEST POINT : TP3
SCOPE SETTING [DEFAULT]

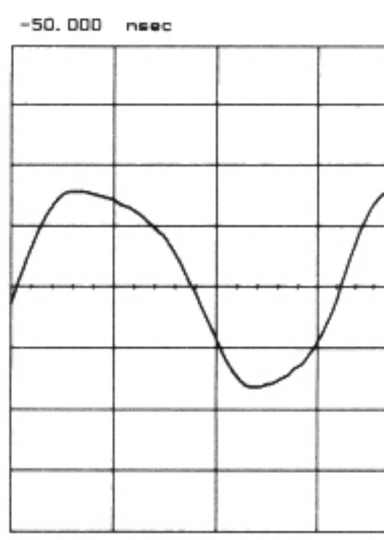


PROCEDURE :

1. Press PRESET.

4 BOARD : AB5

TEST POINT : TP4
SCOPE SETTING [DEFAULT]



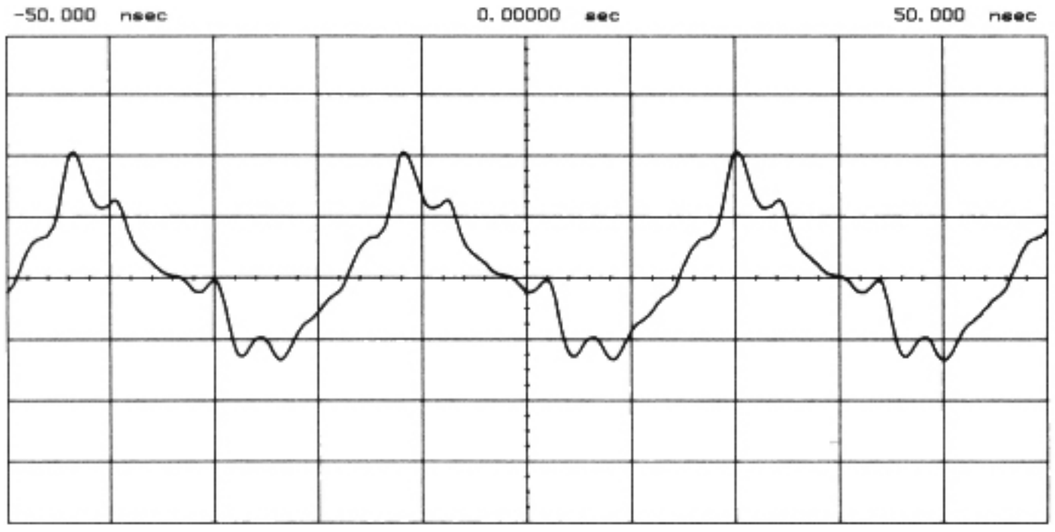
PROCEDURE :

1. Press PRESET.

Fig. 18a
Chap. 7
Page 42

3 BOARD : AB5

TEST POINT : TP3
SCOPE SETTING [DEFAULT]



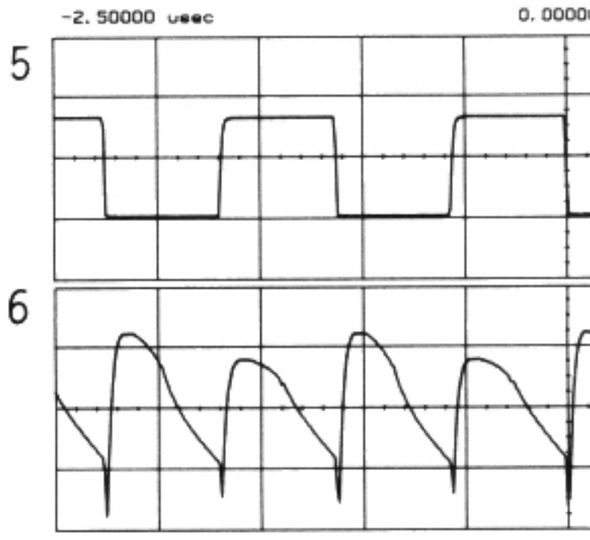
Ch. 1 - 500.0 mvolts/div
Timebase - 10.0 nsec/div
Offset - 0.000 volts
Delay - 0.00000 sec

PROCEDURE :

1. Press PRESET.

5 6 BOARD : AB6

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 - 2.000 volts/div
Ch. 2 - 200.0 mvolts/div
Timebase - 500 nsec/div

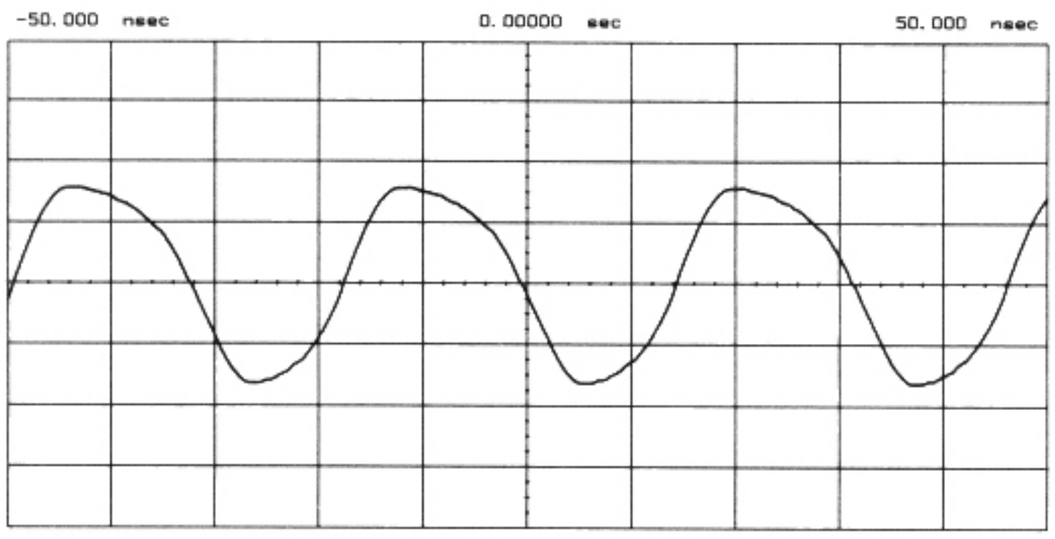
TEST POINT : IC4 pin 16 for Ch. 2

PROCEDURE :

1. Press PRESET.

4 BOARD : AB5

TEST POINT : TP4
SCOPE SETTING [DEFAULT]



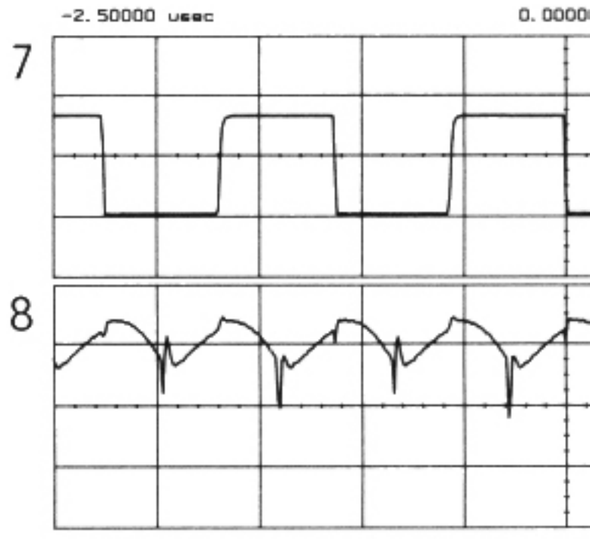
Ch. 1 - 500.0 mvolts/div
Timebase - 10.0 nsec/div
Offset - 0.000 volts
Delay - 0.00000 sec

PROCEDURE :

1. Press PRESET.

7 8 BOARD : AB6

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



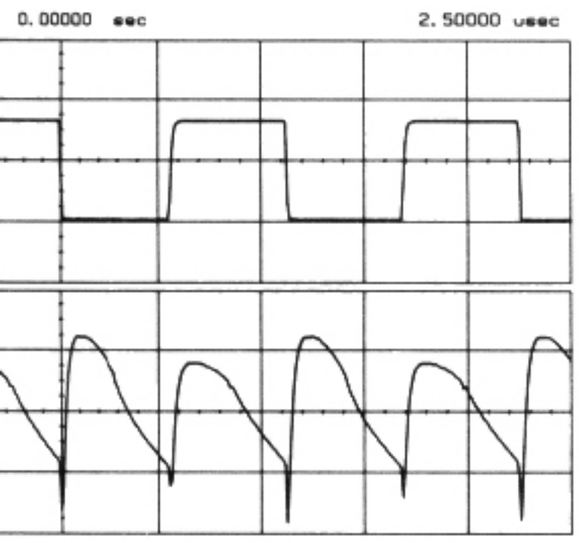
Ch. 1 - 2.000 volts/div
Ch. 2 - 200.0 mvolts/div
Timebase - 500 nsec/div

TEST POINT : TP5 for Ch. 2

PROCEDURE :

1. Press PRESET.

Waveforms for AB5 & AB6



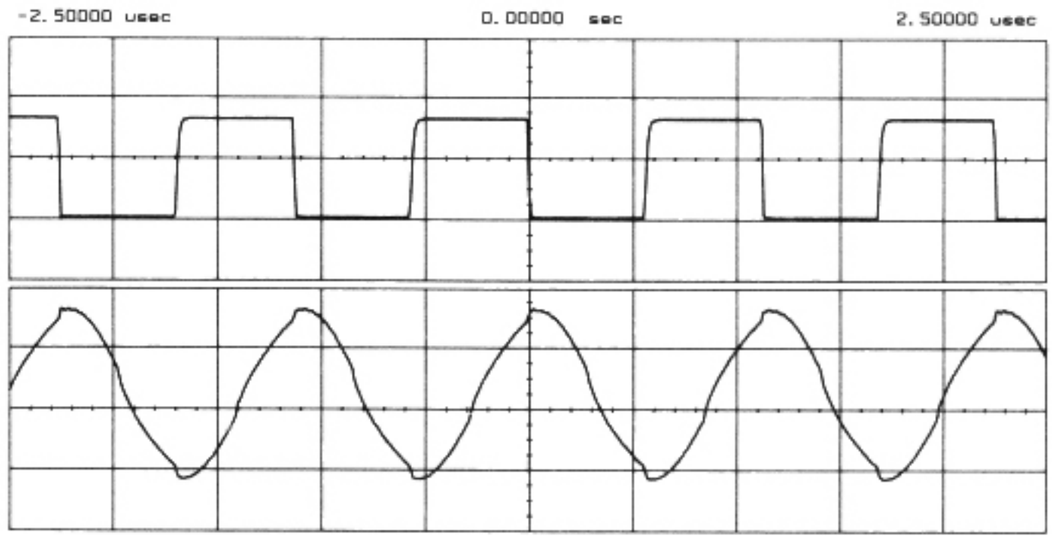
Offset - 2.000 volts
Offset - 0.000 volts
Delay - 0.00000 sec

9 BOARD : AB6

10

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]

9



10

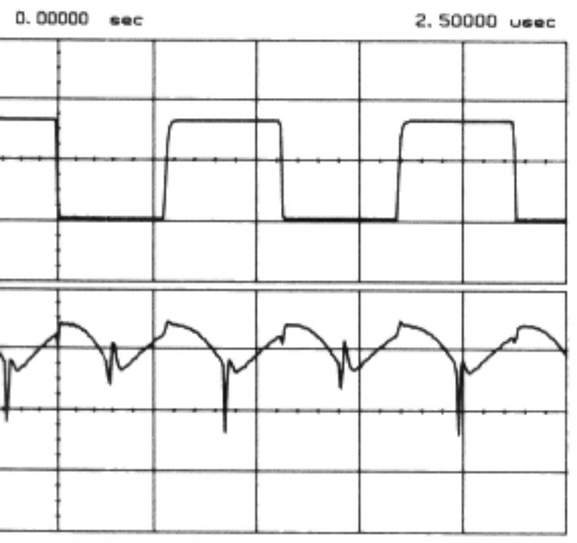
Ch. 1 - 2.000 volts/div
Ch. 2 - 200.0 mvolts/div
Timebase - 500 nsec/div

Offset - 2.000 volts
Offset - 0.000 volts
Delay - 0.00000 sec

TEST POINT : TP3 for Ch. 2

PROCEDURE :

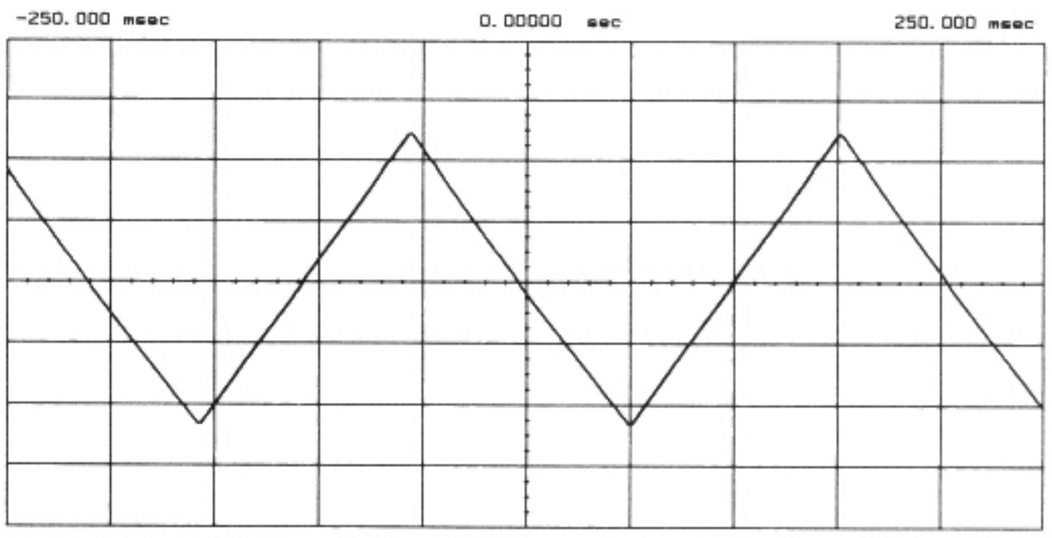
1. Press PRESET.



Offset - 2.000 volts
Offset - 0.000 volts
Delay - 0.00000 sec

11 BOARD : AB6

TEST POINT : IC5 pin 1
SCOPE SETTING [DEFAULT]



Ch. 1 - 5.000 volts/div
Timebase - 50.0 msec/div

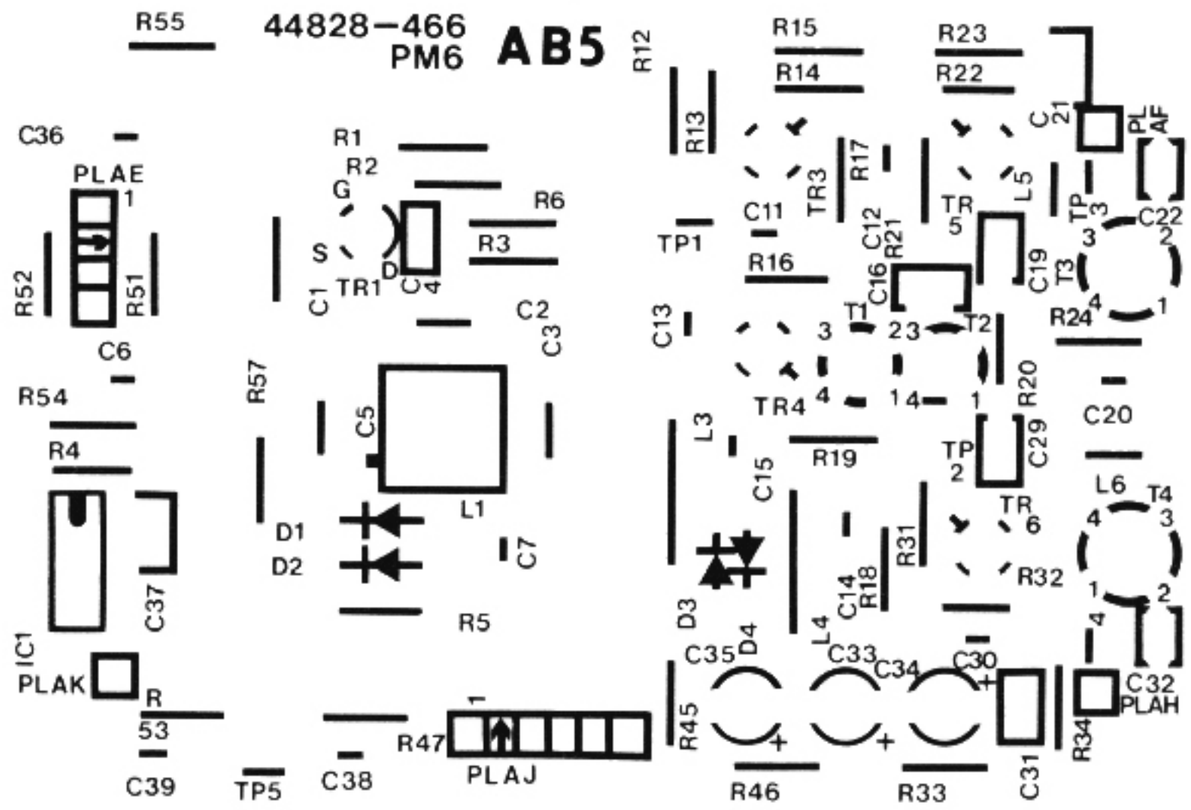
Offset - 0.000 volts
Delay - 0.00000 sec

PROCEDURE :

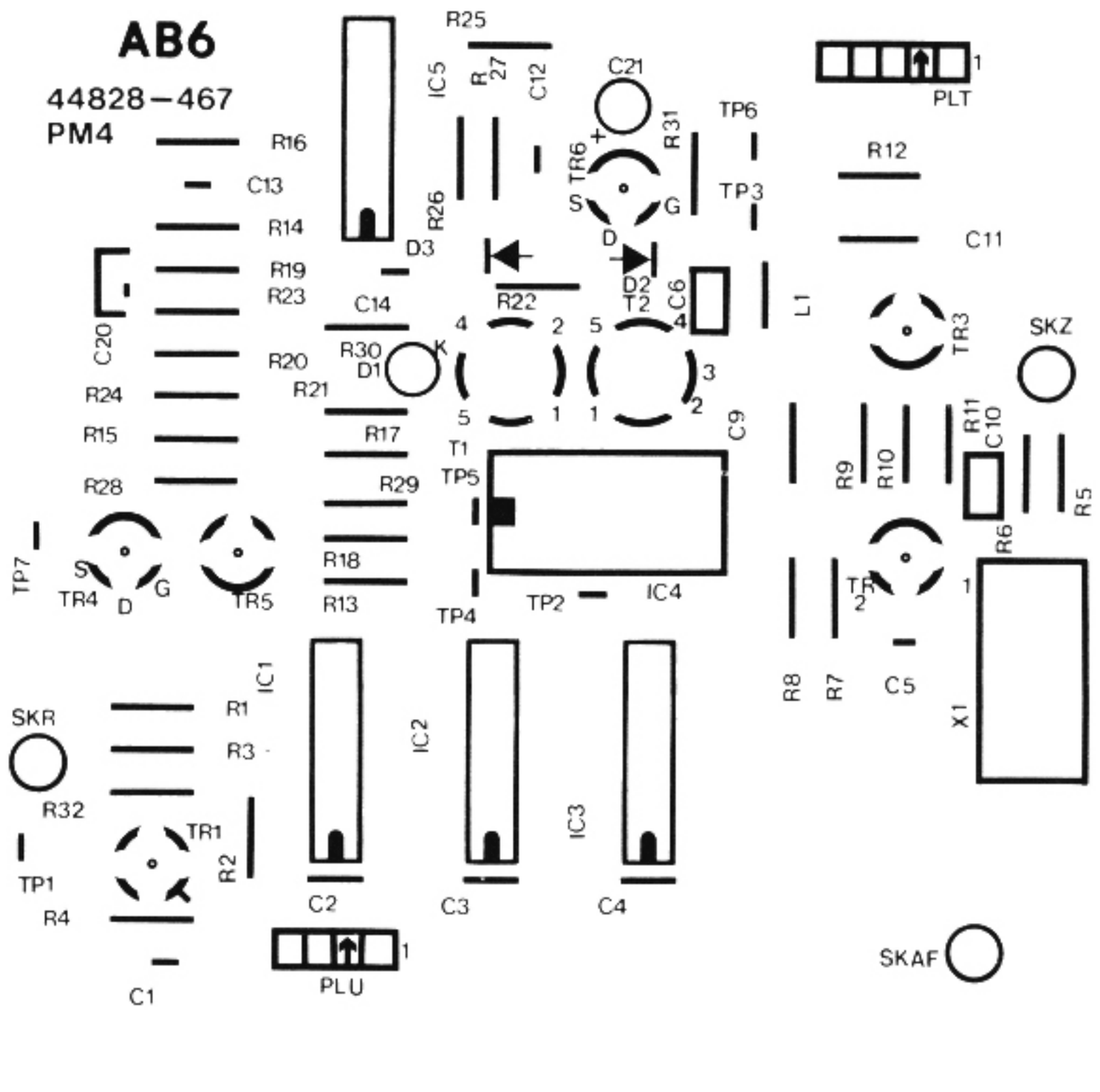
1. Press PRESET.

Fig. 18a

May 86



Component layout for AB5



Component layout for AB6

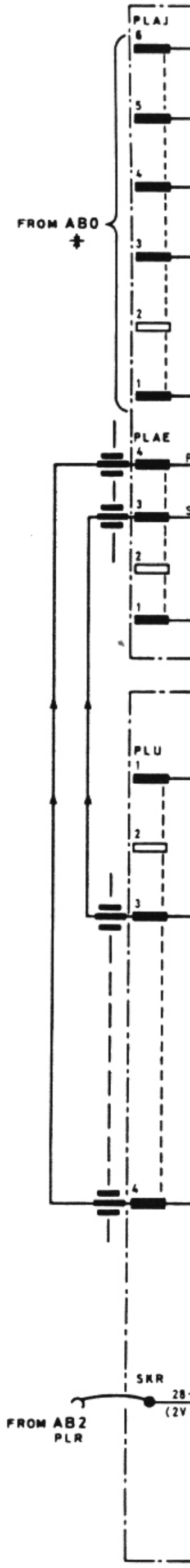


Fig. 18

May 86

FROM AB0

PLAJ

+14·5V
C38 22n
R45 2R2
+4·8Vd
C34 33µ
R46 2R2
-5·2Vd
C33 33µ
R47 2R2
-14·5Vd
C35 33µ
C39 22n

FROM AB3 PLX 7

PLAK

REF. FREQ. IN

R4 1k0
C6 470n

28-35MHz VOLTAGE CONTROLLED OSCILLATOR

R57 10k
C5 100p
COARSE FREQ.
L1
C2 33p
C3 33p
TR1 J310
C1 33p
R1 300k
R2 300k
-14·5Vd
D1 BB809
D2 BB809
C4 4n7
R6 1k6
TP1
R3 3k9
-14·5V

CONTROL SIGNAL SUMMER

PLAE

PLL CONTROL
SEARCH SIGNAL
R55 5k1
R52 5k1
R51 4k7
C36 1µ0
IC2 TDA1034N
+14·5V
C37 33p
TP5
R54 1k0
-14·5Vd
R53 1k0
R5 470R
C7 10n

SEARCH OSCILLATOR

PLU

R24 100k
IC5(d) TL074
R23 2k0
R25 1M0
TP6
IC5(c) TL074
R26 100k
R27 2k2
C21 2µ2
-14·5V
R31 3k3
TR6 2N4857
R22 10k
D2 1N4148

COMP.

+14·5V
C12 33µ
IC5(a) TL074
R17 820k
0·3µS DELAY
TP5
R18 1k5
R29 1k5
C20 220p
R20 3k0
-14·5V
C14 33µ
D3 1N4148

TR5 BC308
R30 100k
R29 15k
R28 30k
-14·5V
D1 TIL209
OUT OF LOCK
R21 1k2

LOOP FILTER

R15 150k
TR4 2N4857
C13 10n
R14 1k3
IC5(b) TL074
TP7
R16 1k6
R13 10k

LOOP PHASE DISCRIMINATOR

IC4(c) SD5000
T1
IC4(d)

QUAD PHASE ÷2

+4·8V
IC3(a) LS74
TP2

÷16
÷2
÷8

IC1 LS93

IN PHASE ÷2

IC3(b) LS74

IC2 LS00

SKR
28-32MHz
(2V p-p)
FROM AB2 PLR

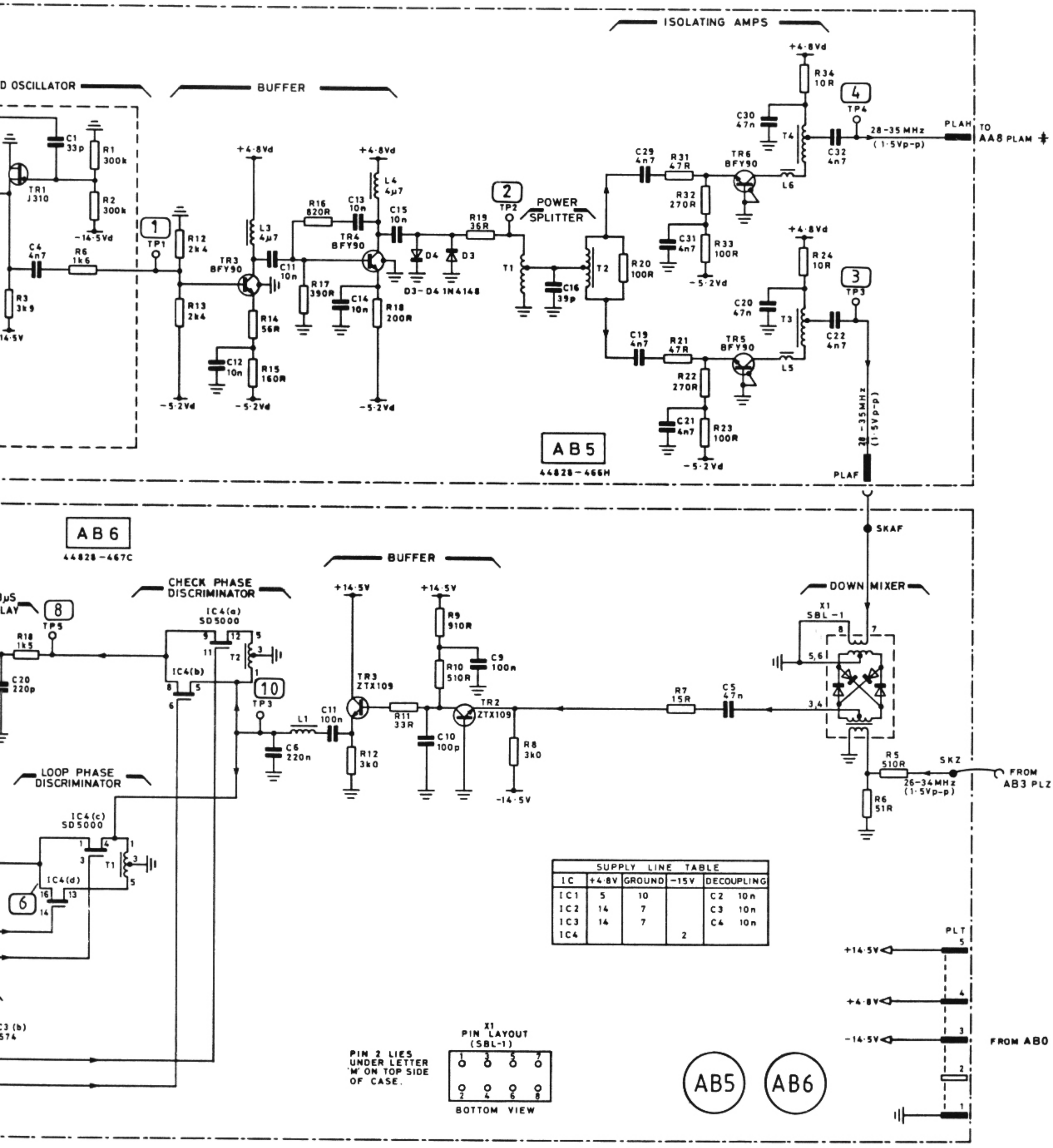
R1 51R
R2 4k7
R3 1k0
R32 10R
TR1 BFY90
R4 330R
C1 22n

AB6
44828-467C

‡ SEE CIRCUIT AB0 FOR CONNE

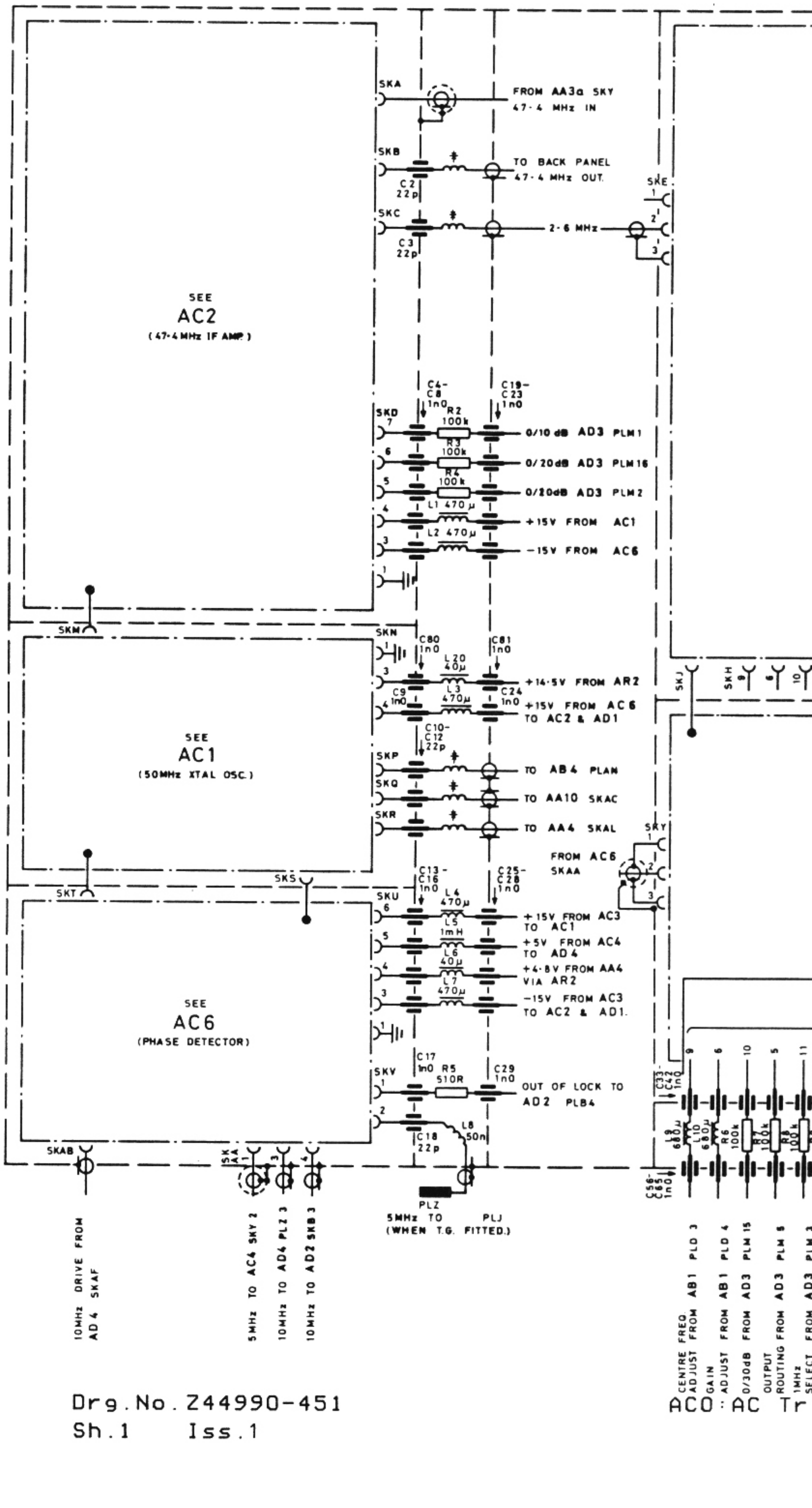
Drg.No. Z44990-450
Sh.8 Iss.1 & 4

AB5: Slave VCO
AB6: Phase detec

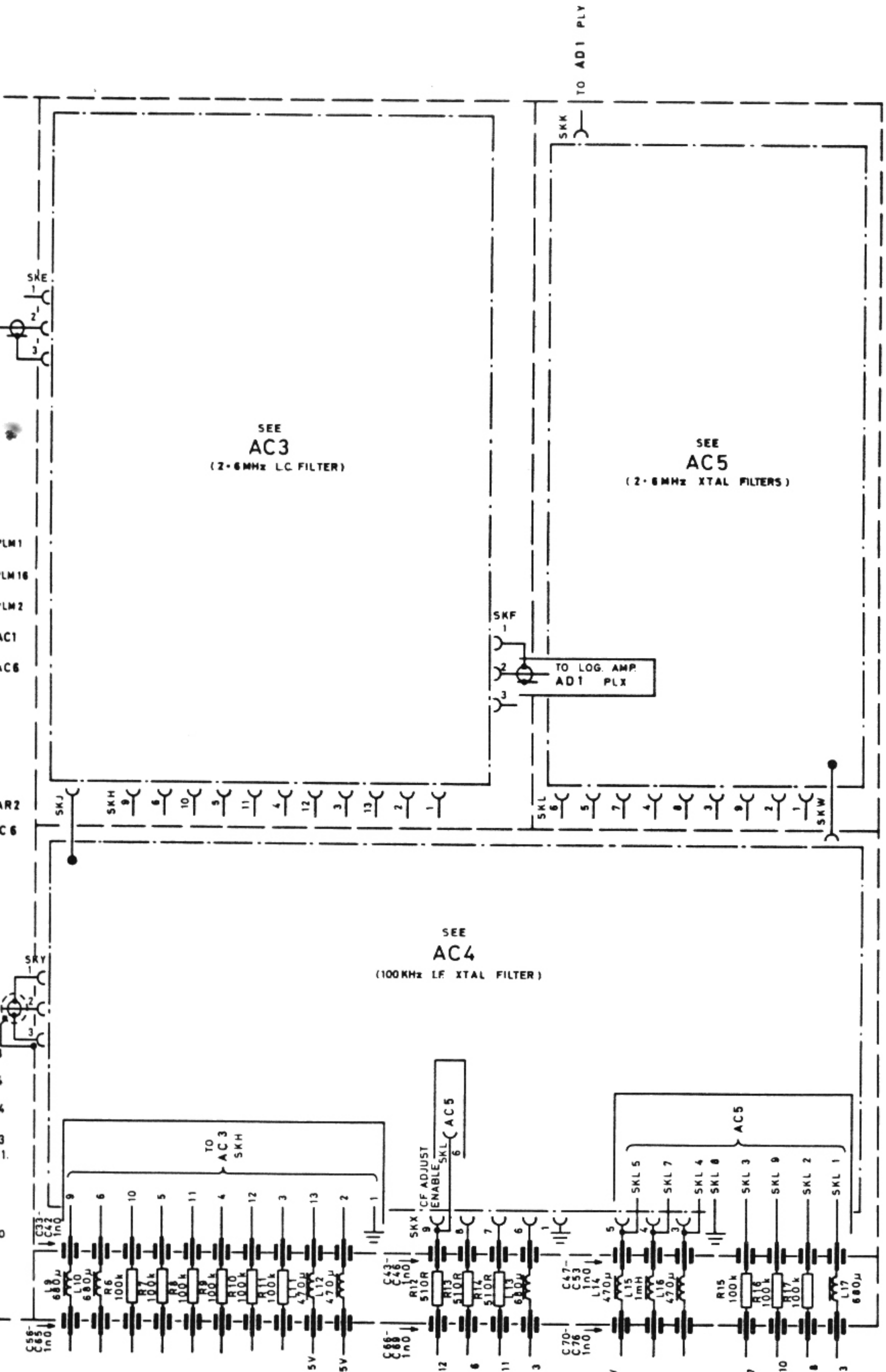


SUPPLY LINE TABLE				
IC	+4·8V	GROUND	-15V	DECOUPLING
IC1	5	10		C2 10n
IC2	14	7		C3 10n
IC3	14	7		C4 10n
IC4			2	

5: Slave VCO
5: Phase detector



Drg. No. Z44990-451
Sh. 1 Iss. 1



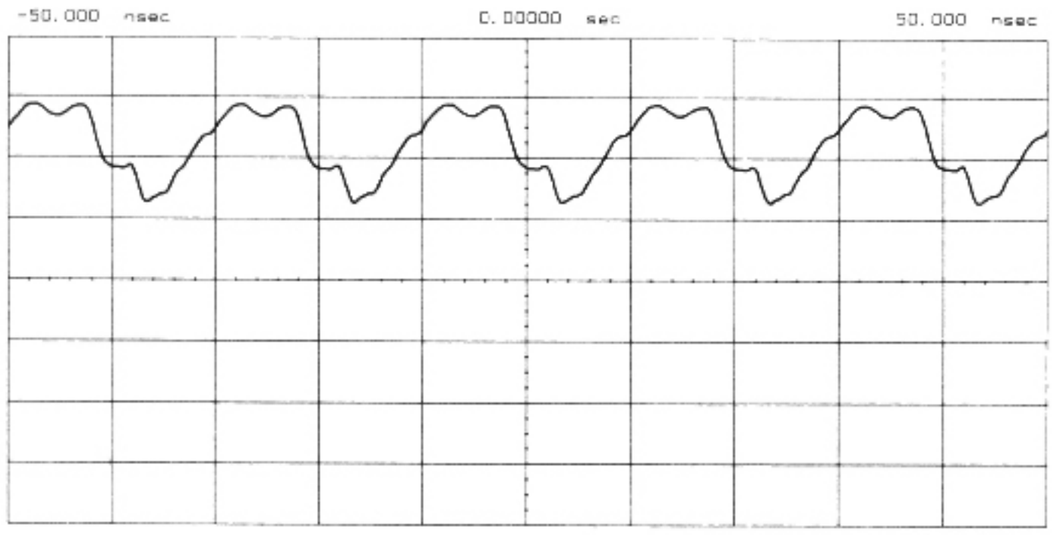
AC0 : AC Tray interconnection

AC0

Fig. 19
Chap. 7
Page 45

1 BOARD : AC1

TEST POINT : TP2
SCOPE SETTING [DEFAULT]



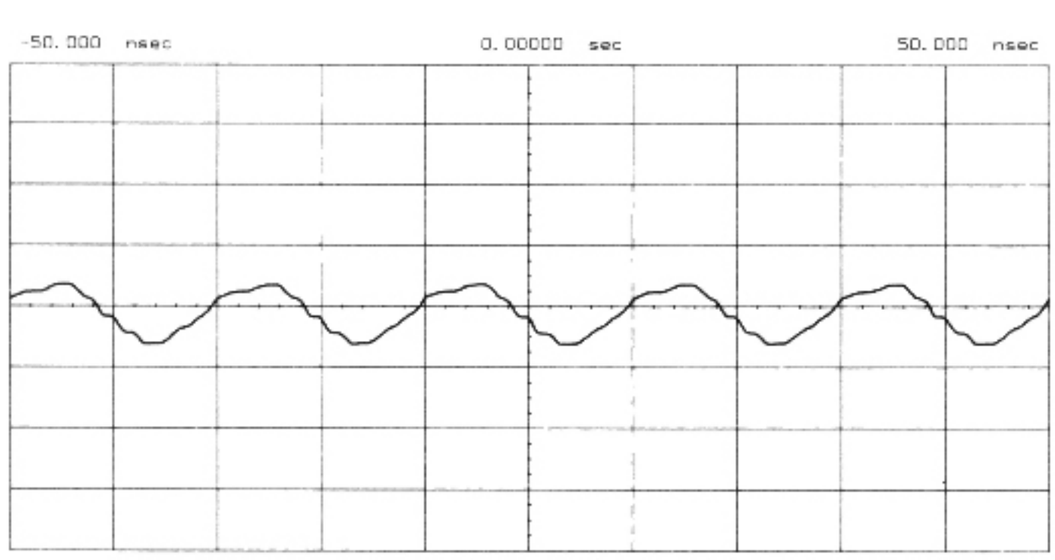
Ch. 1 = 1.000 volts/div
Timebase = 10.0 nsec/div
Offset = 5.000 volts
Delay = 0.00000 sec

PROCEDURE :

1. Press PRESET.

2 BOARD : AC1

TEST POINT : TP3
SCOPE SETTING [DEFAULT]



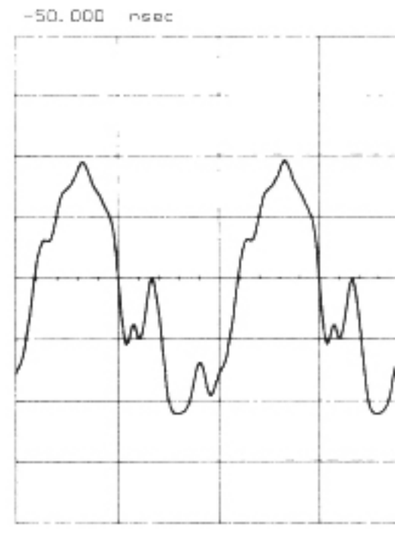
Ch. 1 = 1.000 volts/div
Timebase = 10.0 nsec/div
Offset = 10.00 volts
Delay = 0.00000 sec

PROCEDURE :

1. Press PRESET.

3 BOARD : AC1

TEST POINT : TP4
SCOPE SETTING [DEFAULT]



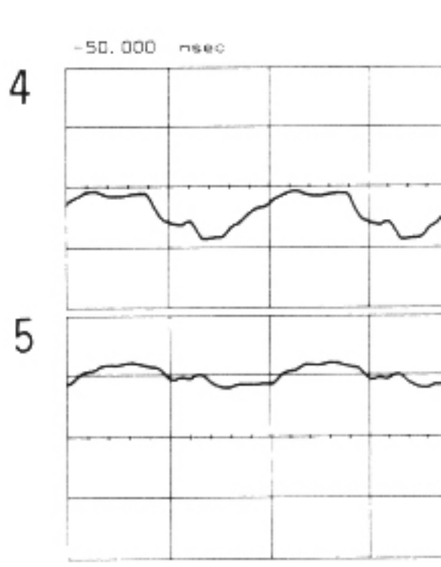
Ch. 1 = 200.0 mvolts
Timebase = 10.0 nsec/d

PROCEDURE :

1. Press PRESET.

4 BOARD : AC1
5

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volt
Ch. 2 = 2.000 volt
Timebase = 10.0 nsec/d

TEST POINT : TP4 for Ch. 2

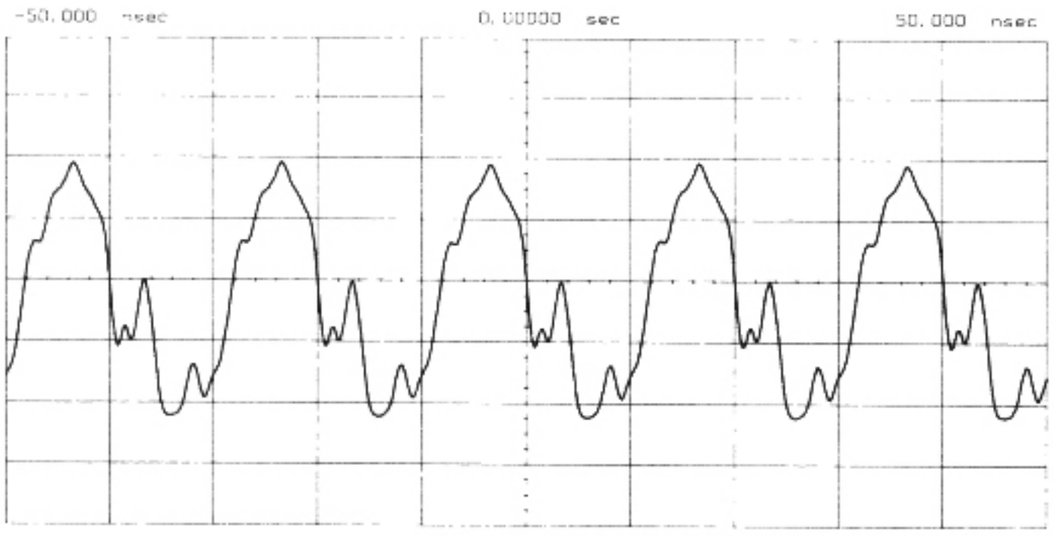
PROCEDURE :

1. Press PRESET.

Fig. 20a
Chap. 7
Page 46

3 BOARD : AC1

TEST POINT : TP4
SCOPE SETTING [DEFAULT]



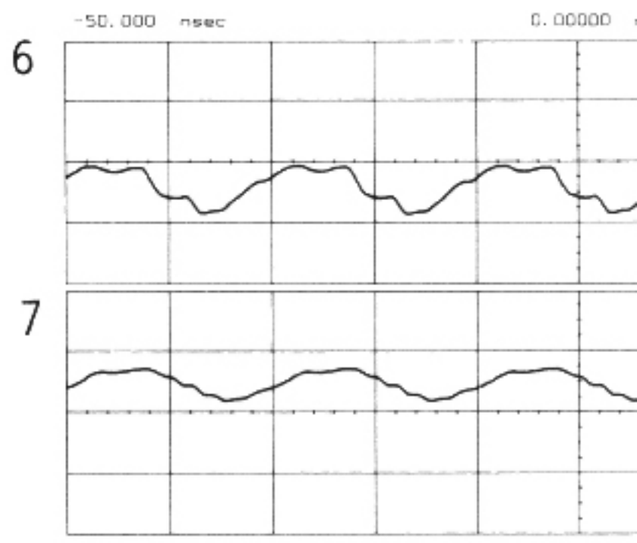
Ch. 1 = 200.0 mvolts/div
Timebase = 10.0 nsec/div
Offset = 2.000 volts
Delay = 0.00000 sec

PROCEDURE :

1. Press PRESET.

6 7 BOARD : AC1

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volts/div
Ch. 2 = 2.000 volts/div
Timebase = 10.0 nsec/div

TEST POINT : TP3 for Ch. 2

PROCEDURE :

1. Press PRESET.

4 5 BOARD : AC1

TEST POINT : TP2 for Ch. 1
SCOPE SETTING [DEFAULT]

Ch. 1 = 2.000 volts/div
Ch. 2 = 2.000 volts/div
Timebase = 10.0 nsec/div
Offset = 9.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

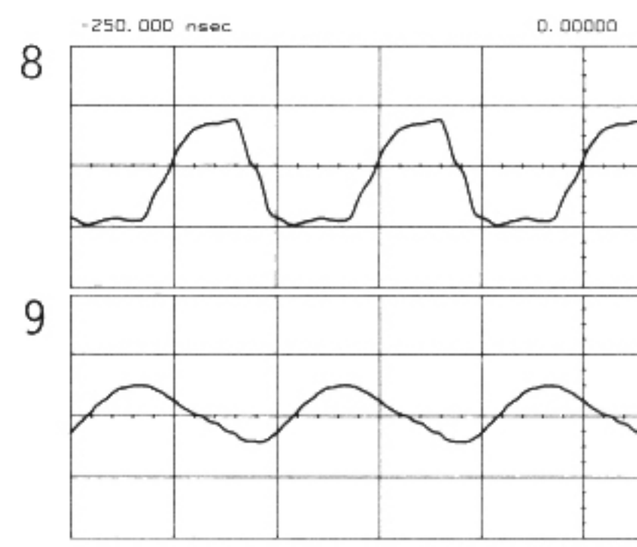
TEST POINT : TP4 for Ch. 2

PROCEDURE :

1. Press PRESET.

8 9 BOARD : AC6

TEST POINT : PLAA4 for Ch. 1
SCOPE SETTING [DEFAULT]



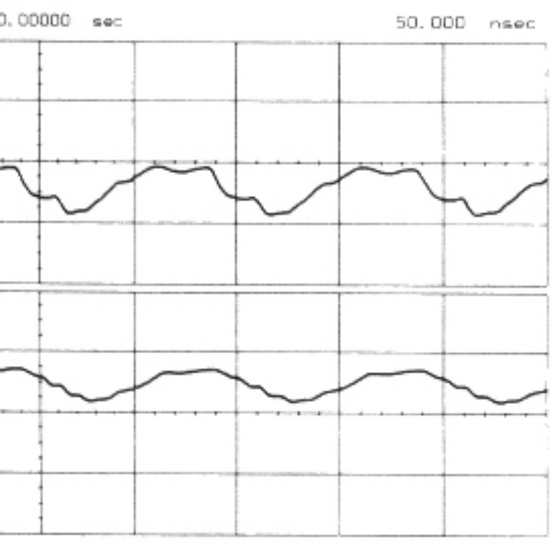
Ch. 1 = 2.000 volts/div
Ch. 2 = 1.000 volts/div
Timebase = 50.0 nsec/div

TEST POINT : PLAA3 for Ch. 2

PROCEDURE :

1. Press PRESET.

Waveforms for AC1 & AC6

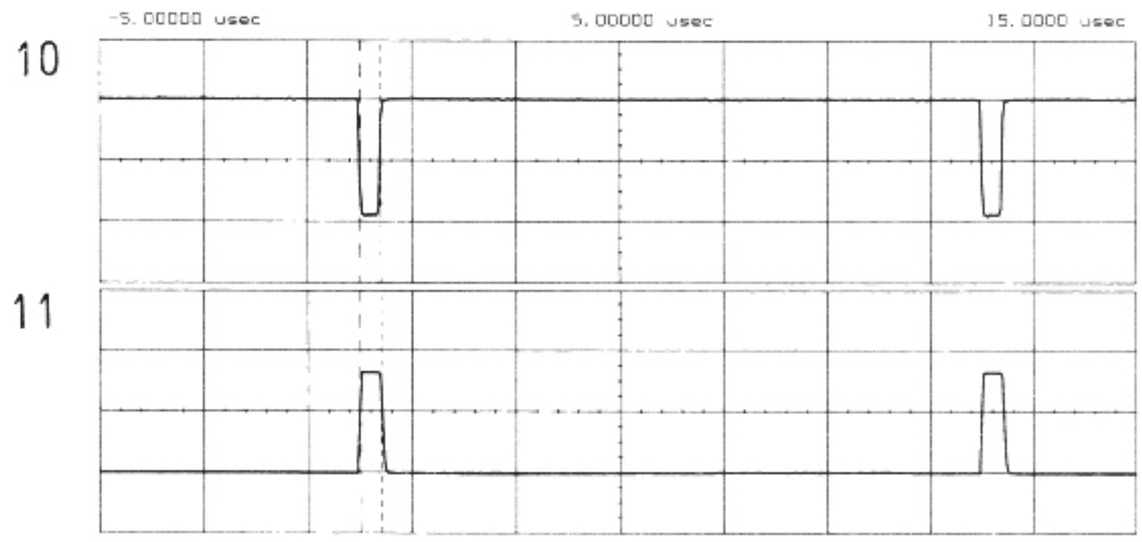


Offset = 9.000 volts
Offset = 9.000 volts
Delay = 0.00000 sec

10
11

BOARD : AC6

TEST POINT : TP6 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volts/div
Ch. 2 = 10.00 volts/div
Timebase = 2.00 usec/div
Delta T = 400.000 nsec
Start = 0.00000 sec

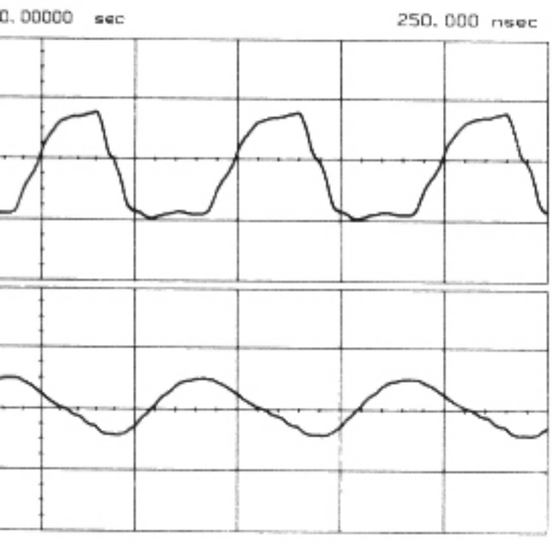
Offset = 2.000 volts
Offset = -2.000 volts
Delay = 5.00000 usec

Stop = 400.000 nsec

TEST POINT : TP2 for Ch. 2

PROCEDURE :

1. Press PRESET.

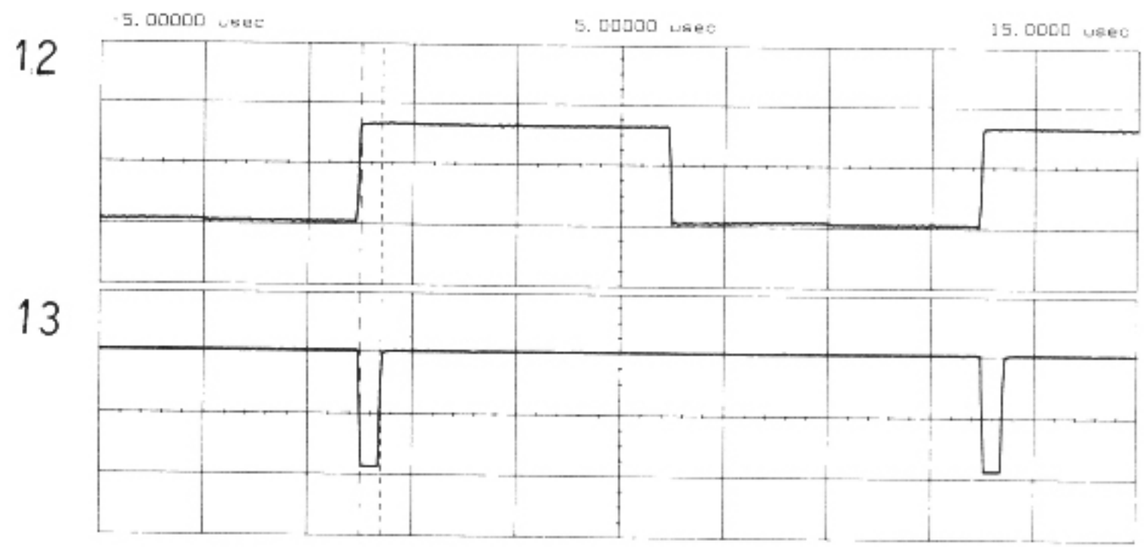


Offset = 2.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

12
13

BOARD : AC6

TEST POINT : TP7 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volts/div
Ch. 2 = 2.000 volts/div
Timebase = 2.00 usec/div
Delta T = 400.000 nsec
Start = 0.00000 sec

Offset = 2.000 volts
Offset = 2.000 volts
Delay = 5.00000 usec

Stop = 400.000 nsec

TEST POINT : TP6 for Ch. 2

PROCEDURE :

1. Press PRESET.

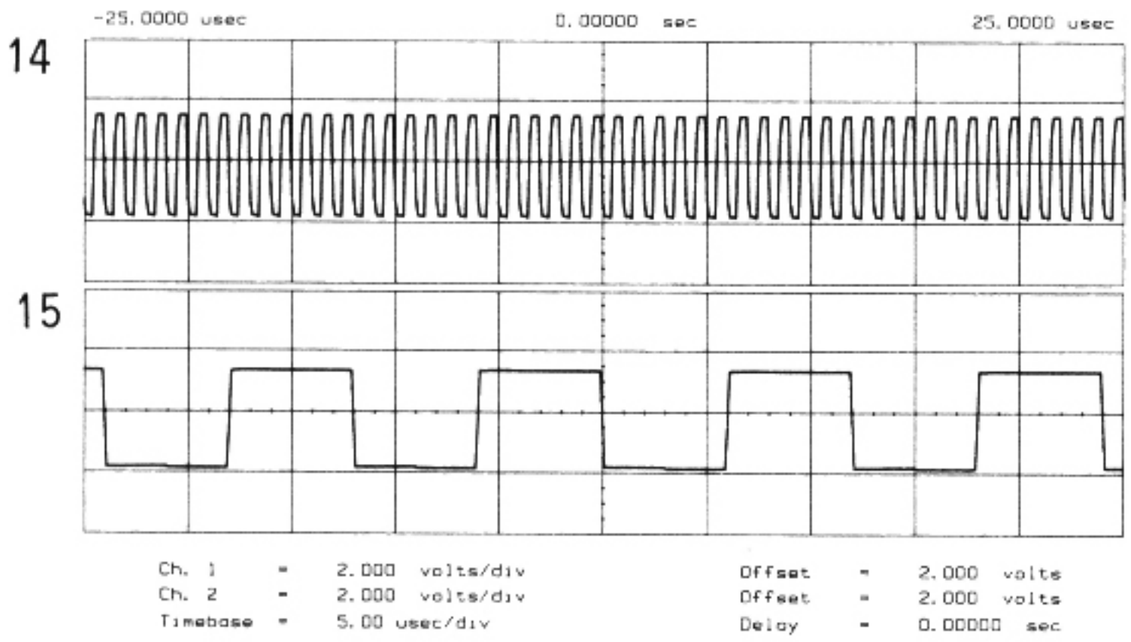
Fig. 20a

May 86

14 BOARD : AC6

15

TEST POINT : TP8 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP7 for Ch. 2

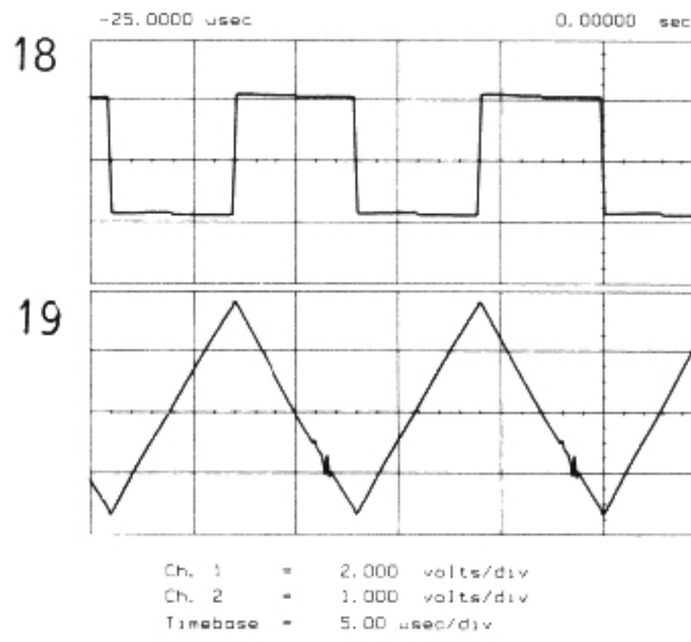
PROCEDURE :

1. Press PRESET.

18 BOARD : AC6

19

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP1 for Ch. 2

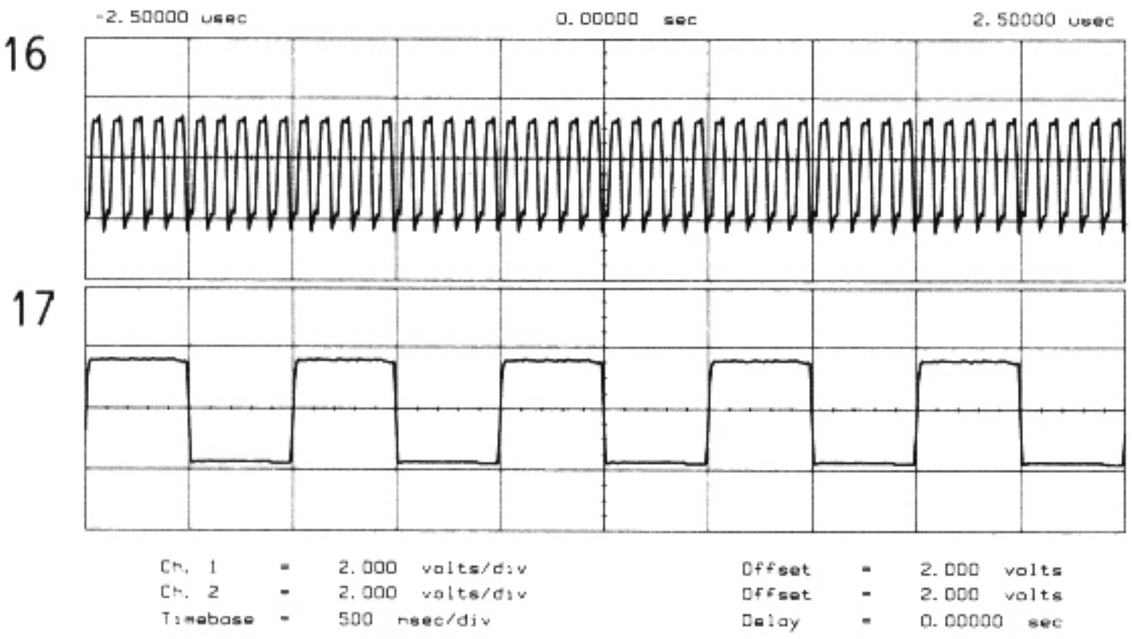
PROCEDURE :

1. Press PRESET.

16 BOARD : AC6

17

TEST POINT : TP9 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP8 for Ch. 2

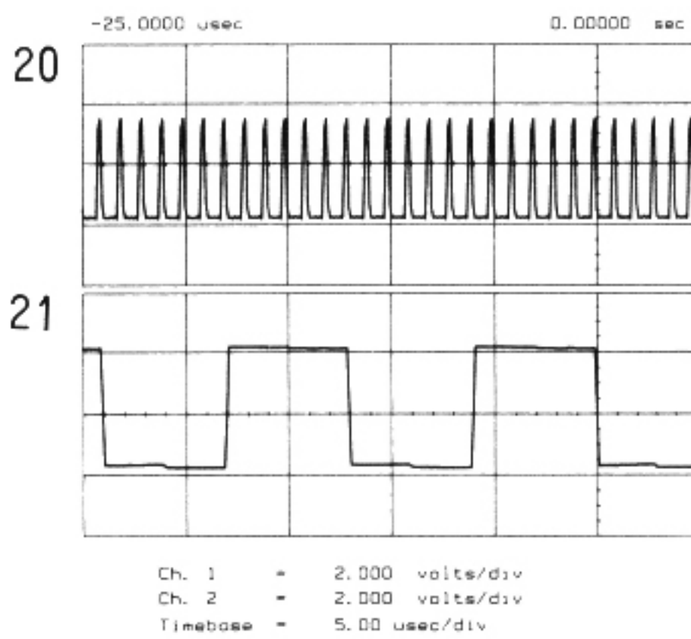
PROCEDURE :

1. Press PRESET.

20 BOARD : AC6

21

TEST POINT : TP10 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP5 for Ch. 2

PROCEDURE :

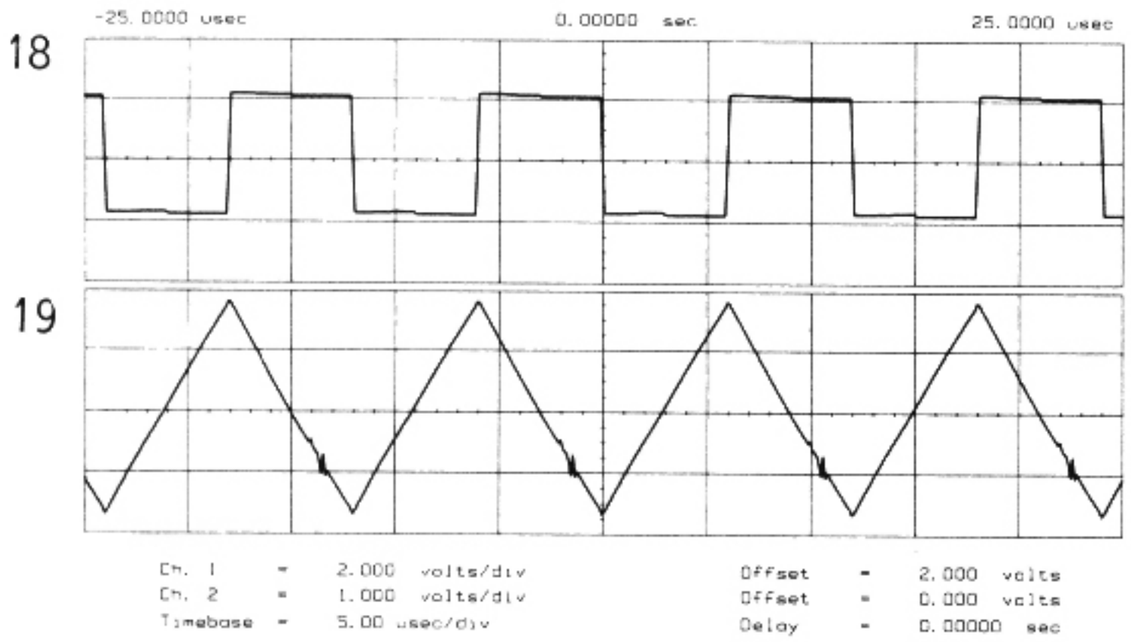
1. Press PRESET.

Fig. 20b
Chap. 7
Page 48/47

18
19

BOARD : AC6

TEST POINT : TP5 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP1 for Ch. 2

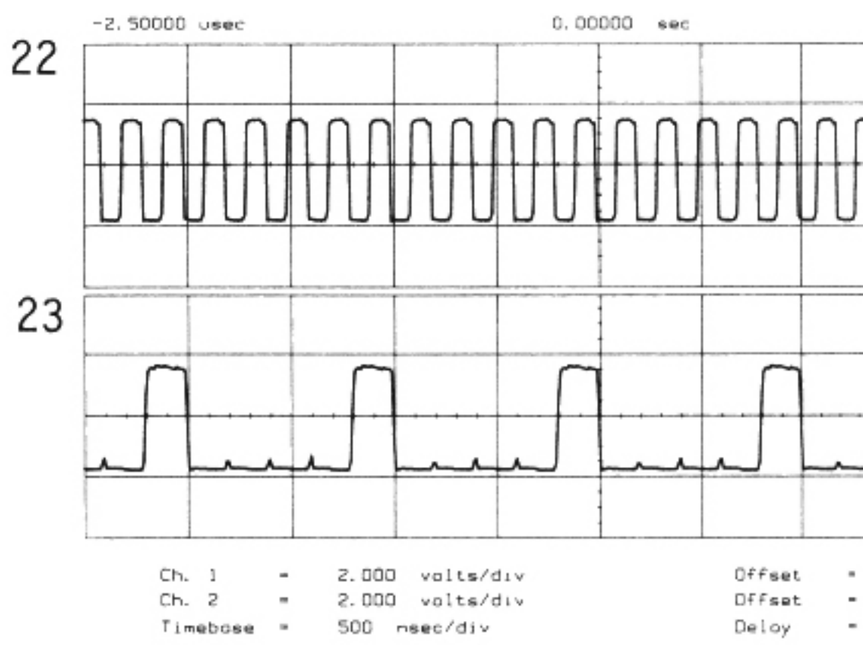
PROCEDURE :

1. Press PRESET.

22
23

BOARD : AC6

TEST POINT : TP11 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP10 for Ch. 2

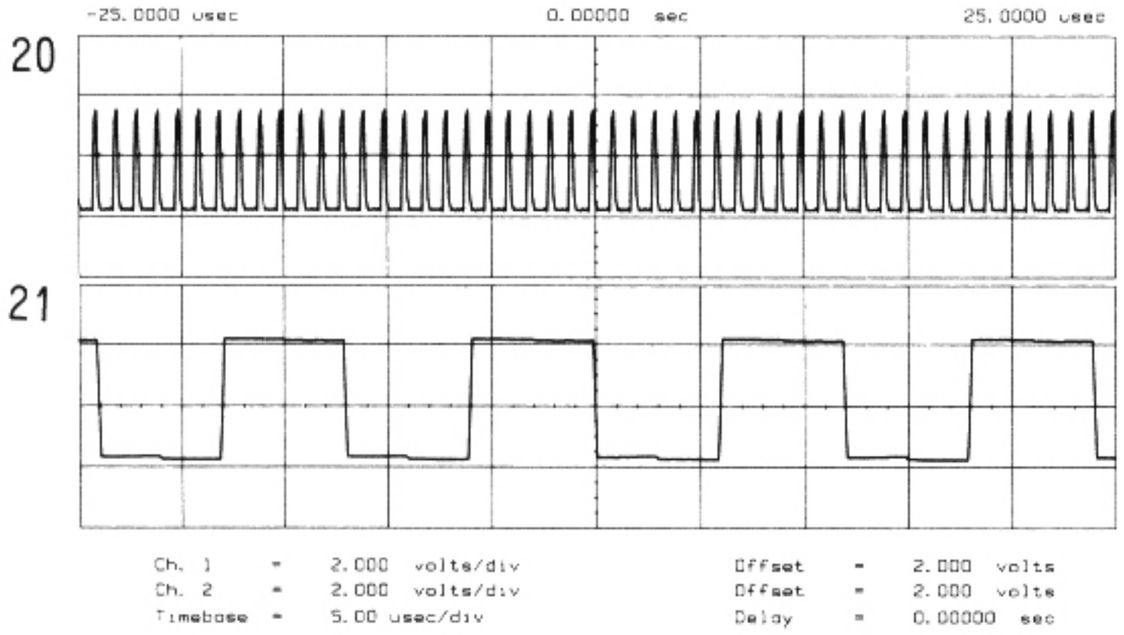
PROCEDURE :

1. Press PRESET.

20
21

BOARD : AC6

TEST POINT : TP10 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP5 for Ch. 2

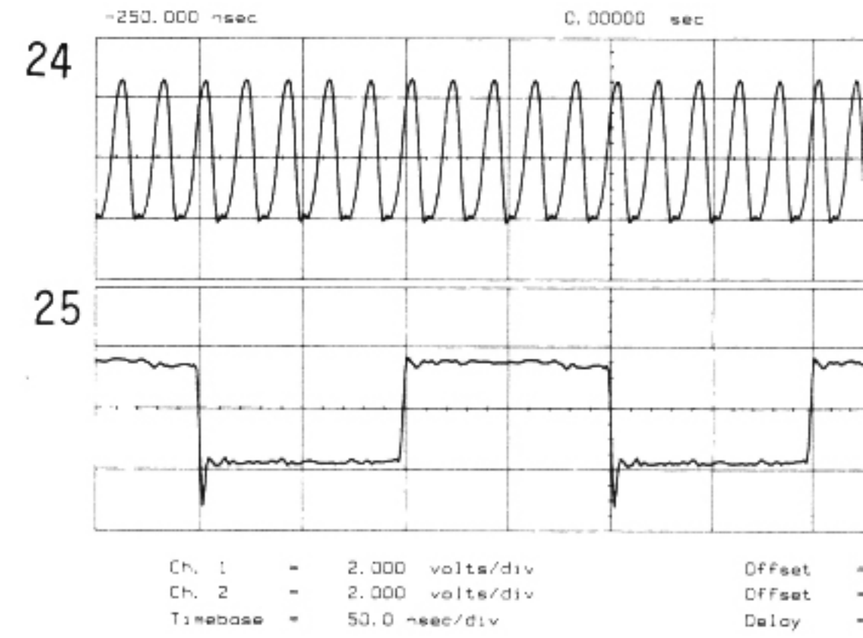
PROCEDURE :

1. Press PRESET.

24
25

BOARD : AC6

TEST POINT : TP12 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP11 for Ch. 2

PROCEDURE :

1. Press PRESET.

Waveforms for AC1 & AC6

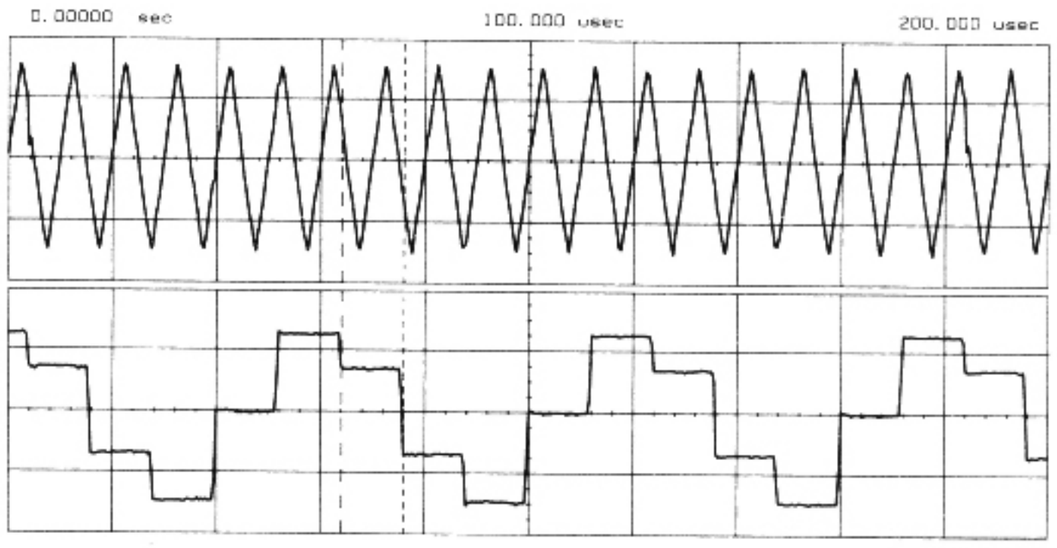
2.50000 usec

fset = 2.000 volts
fset = 2.000 volts
lay = 0.00000 sec

26
27

BOARD : AC6

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	1.000 volts/div	Offset	=	0.000 volts
Ch. 2	=	1.000 volts/div	Offset	=	0.000 volts
Timebase	=	20.0 usec/div	Delay	=	0.00000 sec
Delta T	=	12.0000 usec			
Start	=	64.0000 usec	Stop	=	76.0000 usec

TEST POINT : TP3 for Ch. 2

PROCEDURE :

1. Press PRESET then disconnect SKS from AC1.
2. Inject 60 MHz at 0 dBm through a 50 Ω coaxial load into AC6 SKS.

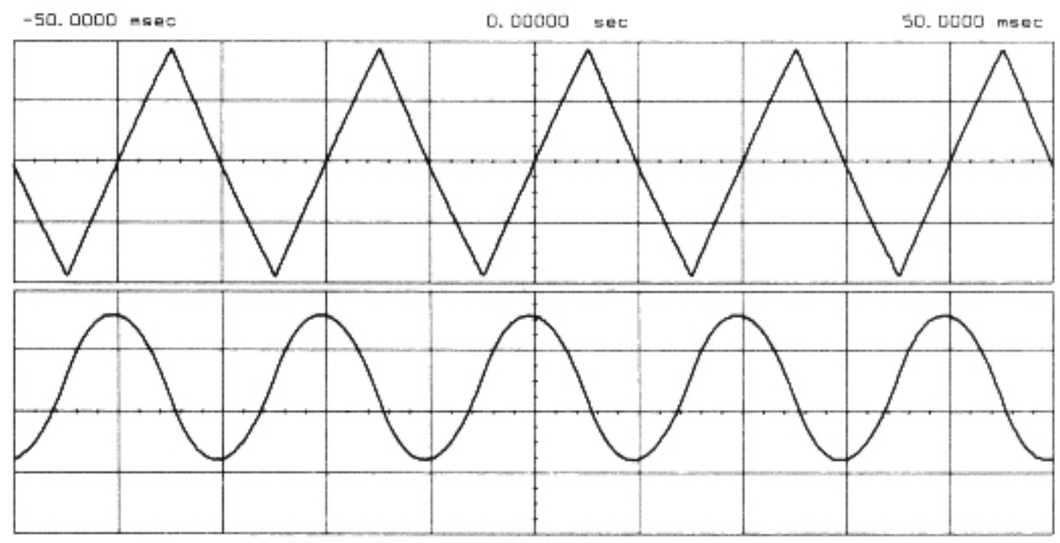
250.000 nsec

ffset = 2.000 volts
ffset = 2.000 volts
elay = 0.00000 sec

28
29

BOARD : AC6

TEST POINT : TP3 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1	=	1.000 volts/div	Offset	=	0.000 volts
Ch. 2	=	1.000 volts/div	Offset	=	0.000 volts
Timebase	=	10.0 msec/div	Delay	=	0.00000 sec

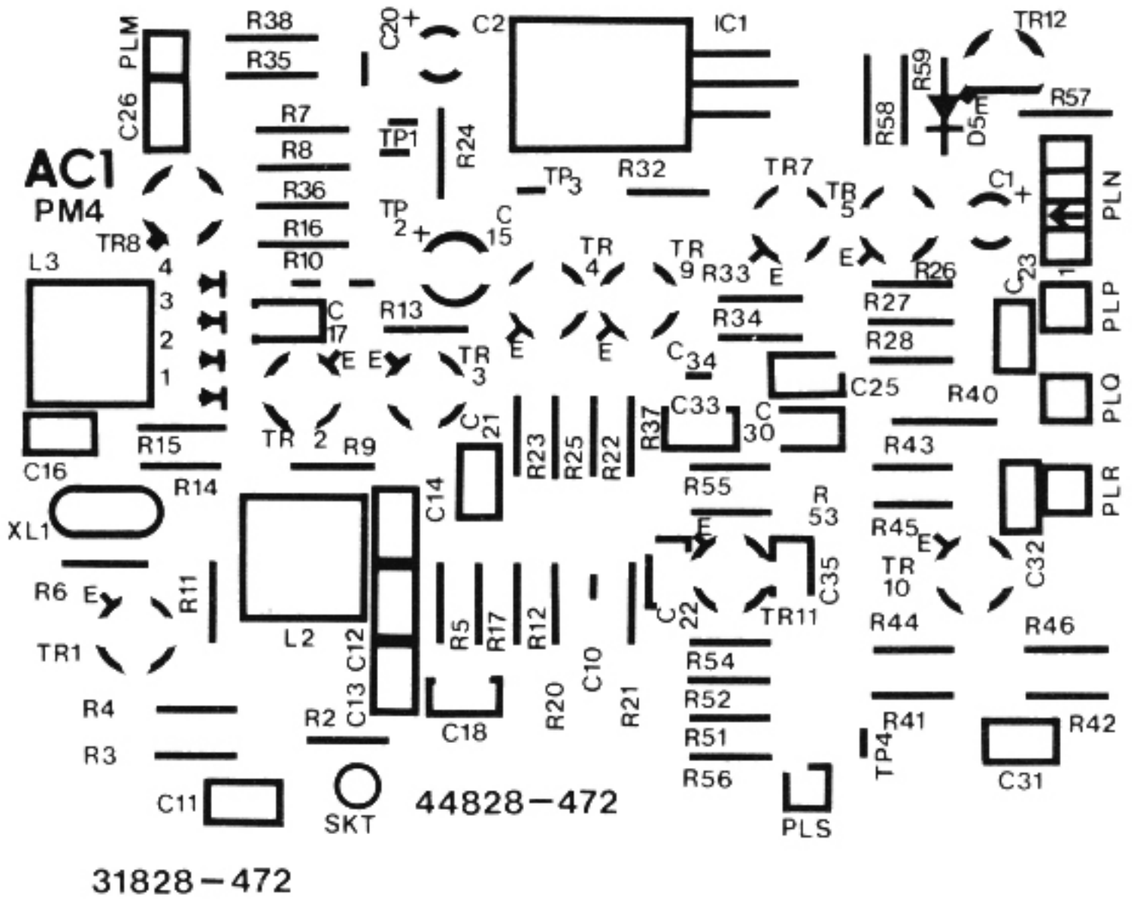
TEST POINT : TP4 for Ch. 2

PROCEDURE :

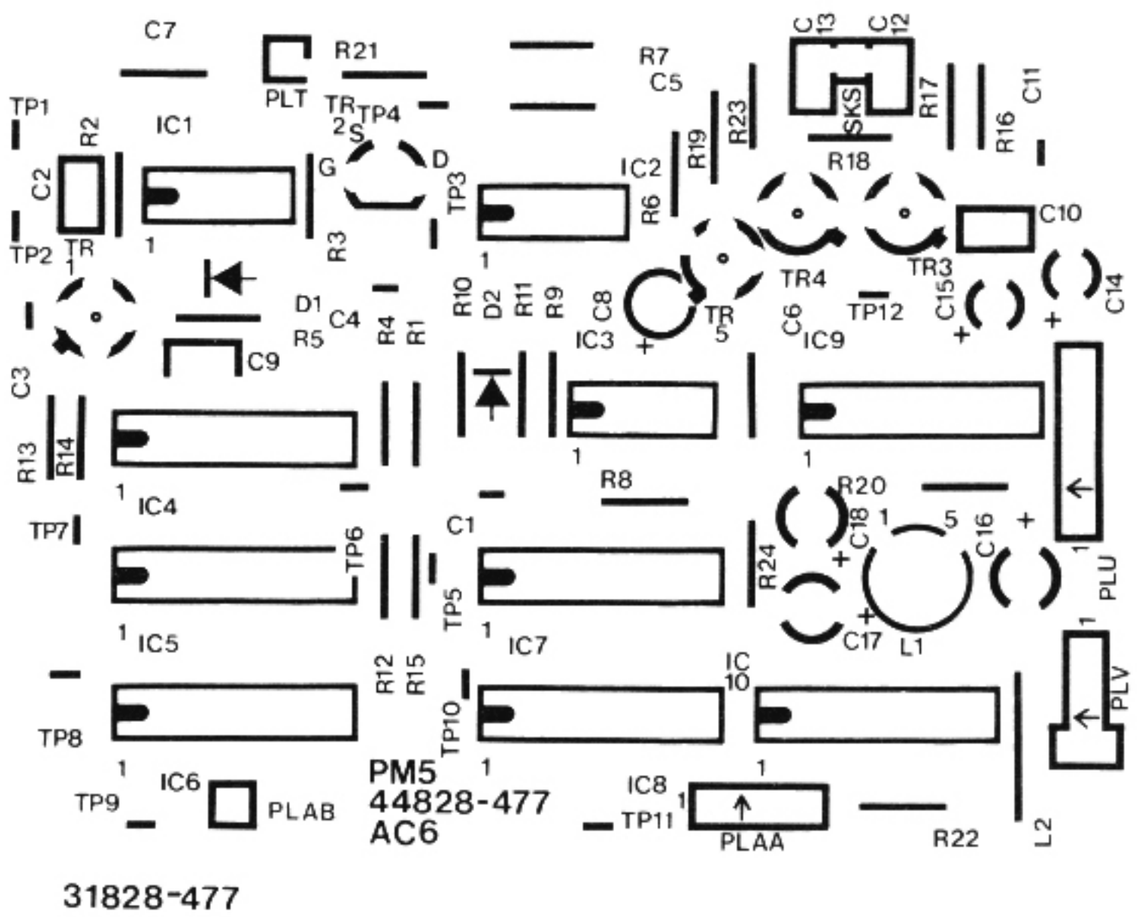
1. Press PRESET then disconnect SKS from AC1.
2. Inject 50.03 MHz at 0 dBm through a 50 Ω coaxial load into AC6 SKS.

Fig. 20b

May 86



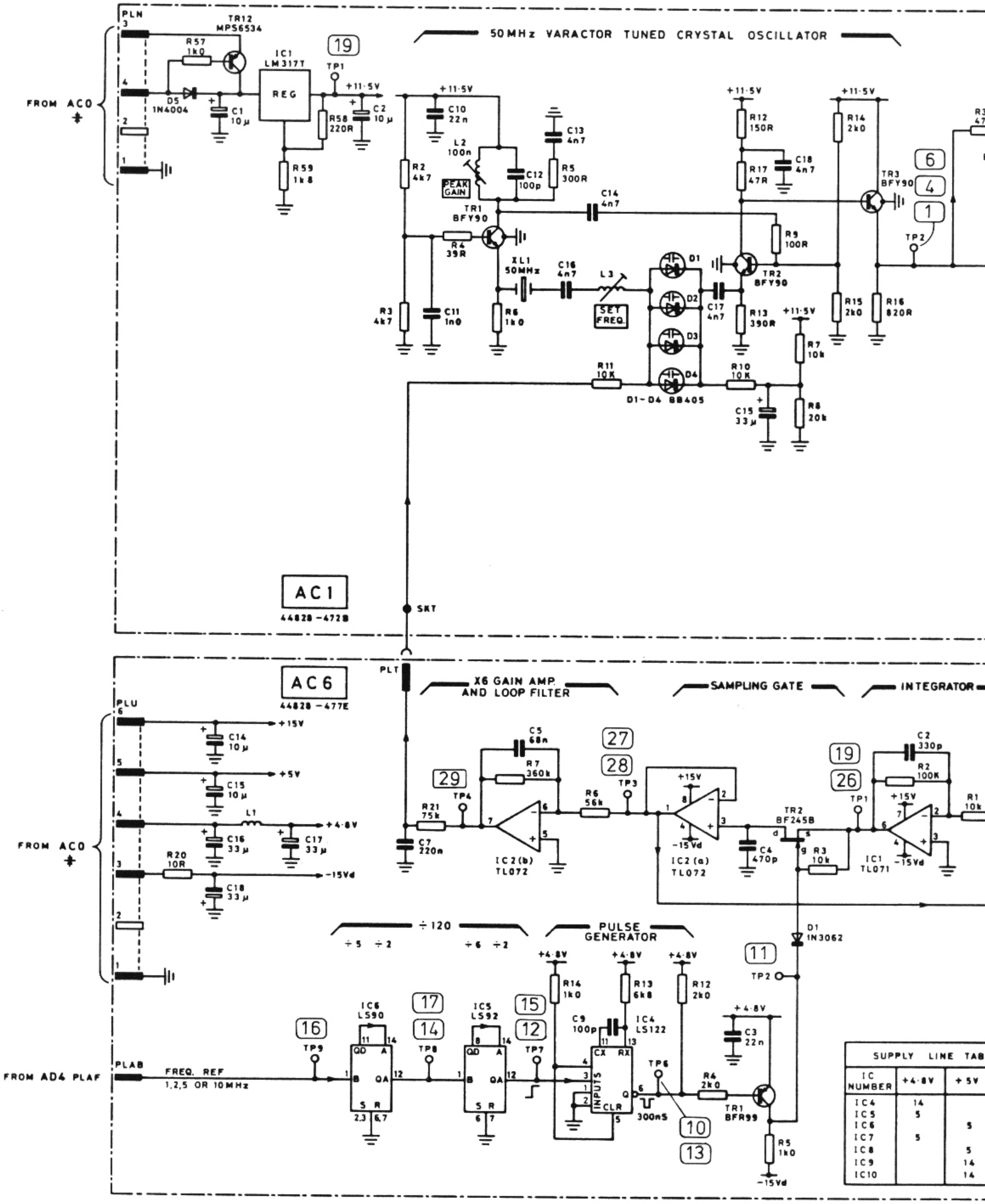
Component layout for AC1



Component layout for AC6

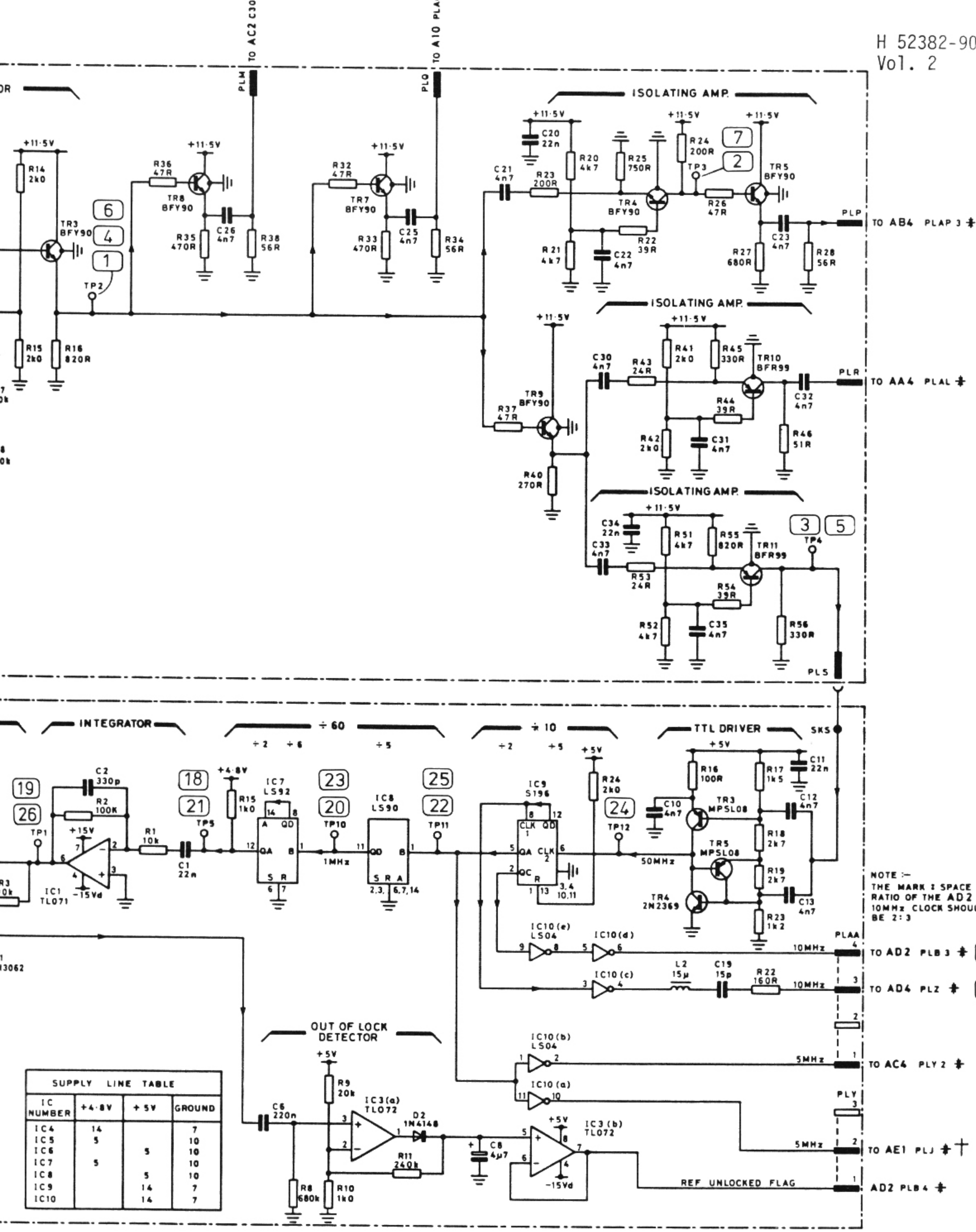
Fig. 20

May 86



Drg.No. Z44990-451
Sh.3 Iss.2&1

AC1 : 50MHz cryst.
AC6 : Phase detec



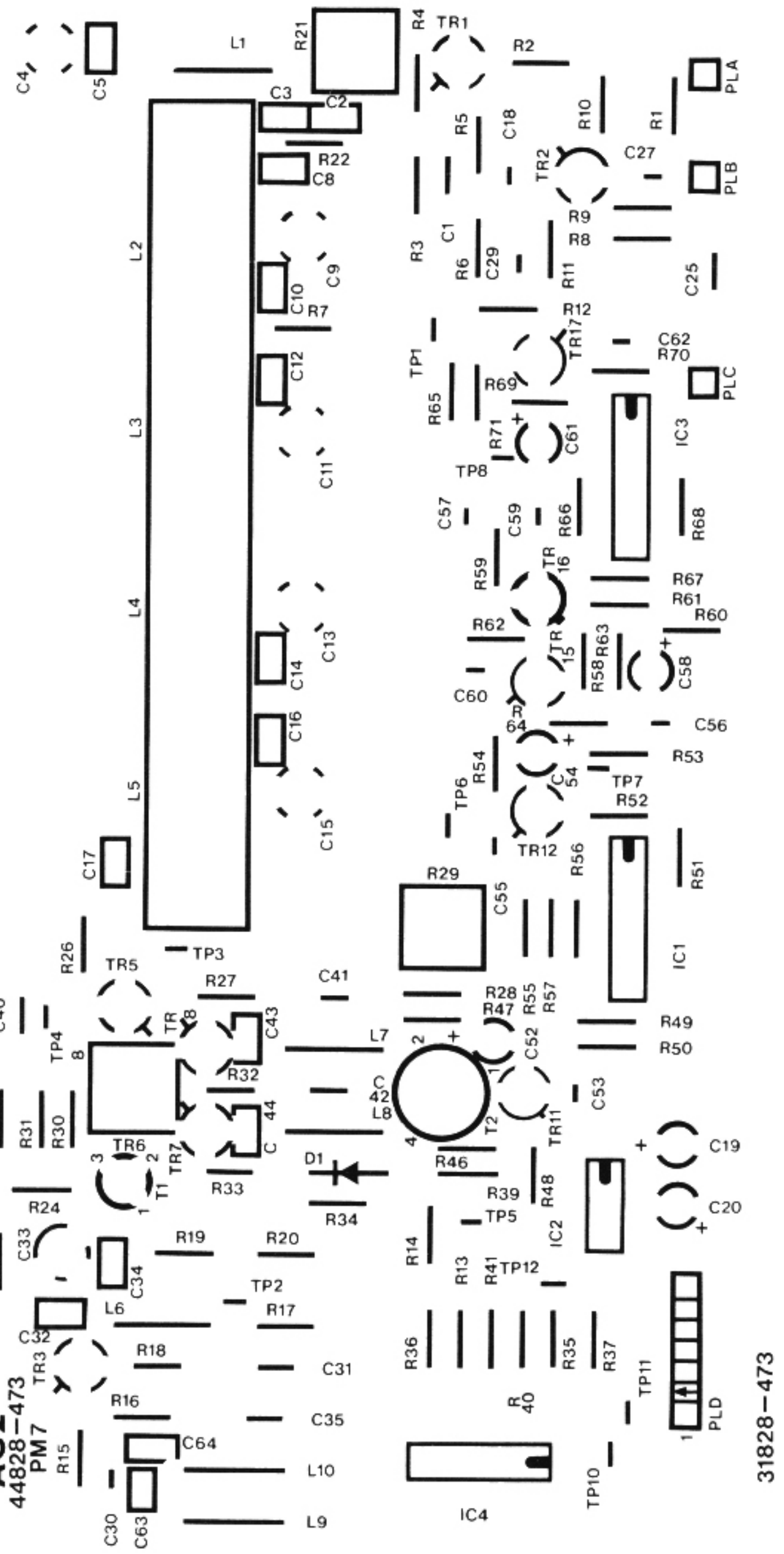
SUPPLY LINE TABLE			
IC NUMBER	+4·8V	+5V	GROUND
IC4	14		7
IC5	5		10
IC6		5	10
IC7	5		10
IC8		5	10
IC9		14	7
IC10		14	7

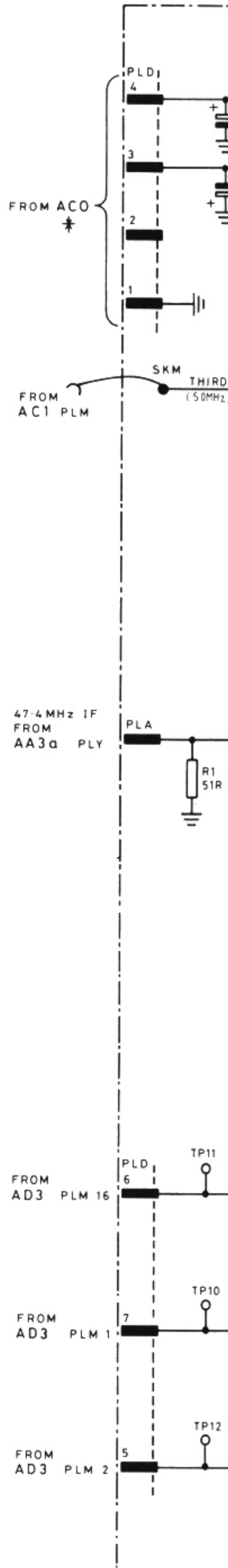
SEE CIRCUIT AC0 FOR CONNECTION DETAILS

+ IF TRACKING GENERATOR FITTED

AC1 AC6

1 : 50MHz crystal oscillator
6 : Phase detector





Component layout for AC2

Fig. 21

May 86

AC 2

44828-473K

FROM ACO ✱

PLD

4 — +15V — C19 3µ3 — R40 100k

3 — −15V — C20 3µ3 — 1·6Vb — R41 12k

2

1

FROM AC1 PLM — SKM — THIRD LOCAL OSC. (50MHz, 10dBm)

C63 10p — L9 680n — C30 82p — R15 47R

L10 100n — C64 100p — R16 2k7 — −15V — C35 100n

BUFFER

+15V — R17 100R — L6 220n — C31 100n

TR3 BFY90 — R18 51R

C32 18p — C33 2p0-22p — C34 47p — TUNE

R19 3k6 — TP2 — R20 100R

SINGLE BALANCED MIXER

T2 (1, 2, 3, 4, 5)

L7 47µ — +15V — R34 3k0 — R32 51R — R33 51R

C43 68p — TR8 BFY90 — D1 6·8V — C42 100n

TR6(a) U431 — R30 100R — T1 — R31 100R

AMP

+15V — R3 100R — R4 330R — C1 100n

52·6MHz NOTCH FILTER

NULL NOTCH — R21 50R — R22 2k0 — C2 10p — C3 10p

BANDPASS FILTER

47·4MHz IF FROM AA3a PLY — PLA — R2 100R — TR1 BFY90

R1 51R — R5 36R — C18 10n — R6 680R — −15V

L1 820n — C4 2p0-10p — C5 15p

C8 100p

L2 — L3 — L4 — L5

C9 — C10 8p2 — C11 — C12 8p2 — C13 — C14 8p2 — C15 — C16 10p

R7 100k — TP1

C9, C11, C13, C15 ARE 2p0-10p

C17 100p — R26 100R — TR5 BFY90 — TP3

R27 75R

R23 330R — R24 1k0 — R28 330R — C40 100n — R25 3k6 — R29 500R — −15V — −15V

+15V — R13 20k — R14 10k — R36 1M0

FROM AD3 PLM 16 — PLD 6 — TP11 — 0/20dB CONTROL LOW SELECTS −20dB

R37 1M0

FROM AD3 PLM 1 — 7 — TP10 — 0/10dB CONTROL LOW SELECTS −10dB

R35 1M0

FROM AD3 PLM 2 — 5 — TP12 — 0/20dB CONTROL LOW SELECTS −20dB

✱ SEE CIRCUIT ACO FOR CONNECTION DE

Drg. No. Z44828-473K
Sh. 1 Iss. 3

AC2: 47.4MHz I.F

AC 2
44828 – 473K

SINGLE BALANCED MIXER

0/20dB ATTEN.

0/10dB ATTEN.

30dB AMP.

0/20dB ATTEN.

OUTPUT BUFFER

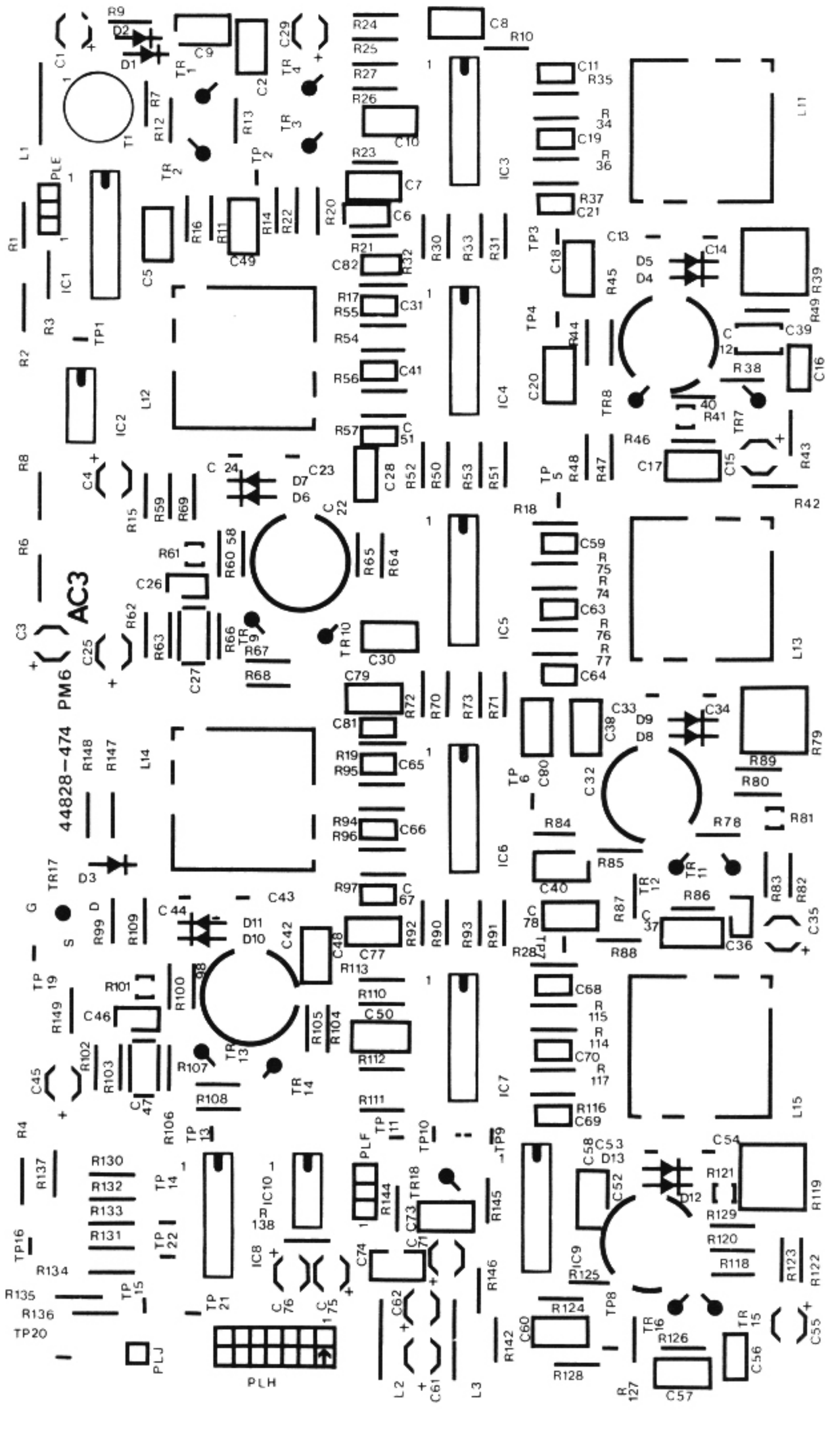
+15V
-15V
R46 100R
R47 100R
R53 100R
R52 100R
R60 100R
R70 100R
R39 360R
R48 3k6
R49 180R
R50 1k800
R51 200R0
R54 3k6
R55 200R
R56 649R0
R57 300R0
R63 3k6
R64 120R
R58 3k9
R59 2k0
R61 2k7
R65 100R
R62 1k0
R66 180R
R67 1k800
R68 200R0
R69 100R
R71 3k0
R8 100R
R9 51R
R10 100R
R11 22R
R12 1k5
C52 3µ3
C54 3µ3
C58 3µ3
C61 3µ3
C53 100n
C55 100n
C56 100n
C57 100n
C59 100n
C60 100n
C62 100n
C25 100n
C27 10n
C29 10n
C44 68p
C42 100n
C41 100n
C40 100n
C17 100p
L7 47µ
L8 47µ
R32 51R
R33 51R
R34 3k0
R30 100R
R31 100R
R26 100R
R27 75R
R23 330R
R24 1k0
R25 3k6
R28 330R
R29 500R
T1
T2
D1 6·8V
TR5 BFY90
TR6(b) U431
TR7 BFY90
TR8 Y90
TR11 BC209C
TR12 BC209C
TR15 BC308B
TR16 2N3904
TR17 BC209C
TR2 BFY90
IC1(a) SD5002
IC1(b)
IC1(c)
IC1(d)
IC3(a) SD5002
IC3(b)
IC4 (a) TLO74
IC4 (b)
IC4 (c) TLO74
IC4(d)
IC2(b) TLO72
IC2 (a)
Vb
TP3
TP4
TP5
TP6
TP7
TP8
PLC
2·6MHz IF TO AC3 PLE 2
PLB
47·4MHz TO BACK PANEL

SUPPLY LINE TABLE		
IC	-15V	GROUND
IC1	2	7, 10, 15
IC3	2, 5, 6, 8, 9, 11, 12	7, 10, 15

CUIT ACO FOR CONNECTION DETAILS

AC2

2:47.4MHz I.F.amplifier



Component layout for AC3

Fig. 22

May 86

30dB NOM. VAR. GAIN AMPLIFIER

BUFFER

FIRST SWITCHED B.W. FI

GAIN VARYING NETWORK

0-30dB ATTENUATOR

FROM AB1 PLD4

PLH 6

GAIN ADJUST

TP16

R6 2k0

C3 3µ3

C1 3µ3

R8 3k9

L1 680µ

C2 100n

D1 5082-3379

D2

C9 100n

R7 1k0

C83 47n

R9 1k0

R150 240R

+15V

R15 10R

C4 3µ3

R12 3k6

R151 20k

R13 9k1

SET GAIN

R14 2k7

R20 100R

C6 56p

TP2

2·6MHz I.F. FROM AC2 PLC

PLE

T1

R3 100R

TP1

IC1a SD5002

IC1b

R1 3k09

R2 100R9

TR1 BC308B

C49 100n

R22 100R

TR2 2N3904

R21 10k

C5 100n

R11 2k0

R16 1k0

-15V

TR3 BC209C

R23 20k

C7 100n

TR4 BC209C

R26 100R

R25 100R

R24 620R

C8 100n

R27 5k1

C29 3µ3

C10 100n

TP3

R34 4k7

SD5002 IC3(a)

R35 2k4

C11 3p9

R30 10k

IC3(b)

R36 510R

30kHz

C19 4p7

R31 10k

100kHz

IC3(c)

R37 150R

C21 15p

R32 10k

300kHz

IC3(d)

R10 18R

R33 10k

1MHz

R38 100R

R41 470R

D4, D5 = BB809

D4

D5

C12 200p

C13 2n2

C14 2n2

L11 3µ2

R49 1M0

TUNE

FROM AD3 PLH 10

PLM 15

TP20

R4 1M0

Va

+15V

IC2(a) TL072

Vb

IC2(b)

-15V

+15V

TP19

R147 100k

TR17 BF245B

C39 100n

R148 68k

R149 470k

D3 1N4148

FROM AB1 PLD 3

9

CENTRE FREQ. ADJ

FROM AD3 PLM

5

TP15

OUTPUT ROUTING

13

TP13

30kHz SELECT

R130 1M0

IC8(a) TL074

30 kHz

C77 100n

4

12

TP22

100kHz SELECT

R131 1M0

IC8(b)

100 kHz

C78 100n

14

4

TP14

300kHz SELECT

R132 1M0

IC8(c)

300kHz

C79 100n

3

11

TP21

1MHz SELECT

R133 1M0

IC8(d)

1MHz

C80 100n

FILTER SWITCHING DRIV

FROM AC0

13

1

2

L2 33µH

C75 3µ3

C61 3µ3

+15V

R137 100k

R135 20k

Vb (+1·5V)

Va (+5V)

R138 11k

R136 10k

L3 33µH

C76 3µ3

C62 3µ3

-15V

Drg. No. Z44828-474A

Sh. 1 Iss. 4

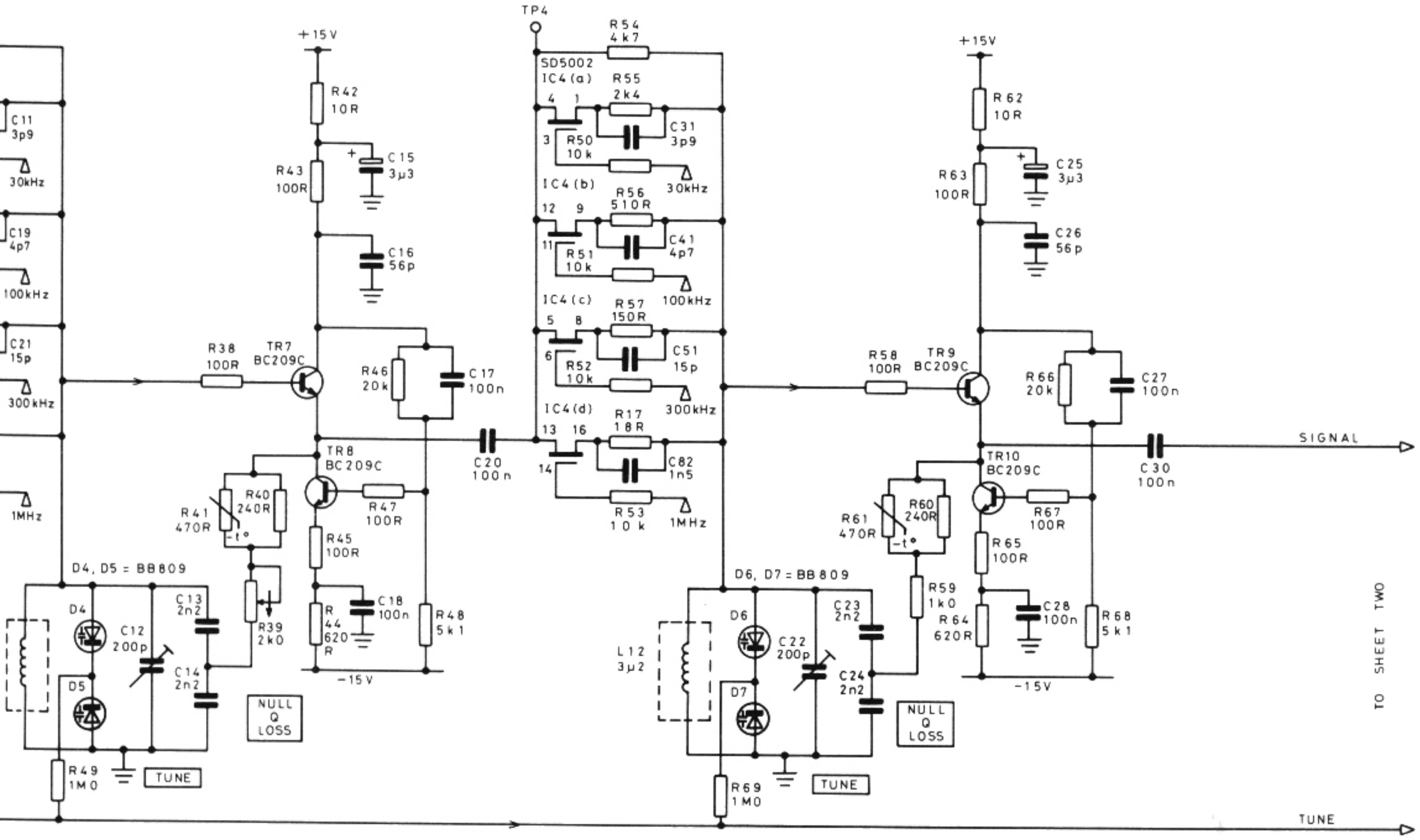
‡ SEE CIRCUIT AC0 FOR CONNECTION DE

AC3: 2.6MHz LC filte

FIRST SWITCHED B.W. FILTER

SECOND SWITCHED B.W. FILTER

PART OF
AC3
44828-474A



FILTER SWITCHING DRIVES

BANDWIDTH SELECTION TABLE				
B.W.	PLH 3	PLH 12	PLH 4	PLH 11
10 kHz	HIGH	HIGH	HIGH	HIGH
30 kHz	LOW	HIGH	HIGH	HIGH
100 kHz	HIGH	LOW	HIGH	HIGH
300 kHz	HIGH	HIGH	LOW	HIGH
1MHz	HIGH	HIGH	HIGH	LOW

SUPPLY LINE TABLE FOR SD5002		
I.C. NUMBER	-15V LINE	GROUND
IC1	2	7, 9 - 16
IC3	2	7, 10, 15
IC4	2	7, 10, 15
IC5	2	7, 10, 15
IC6	2	7, 10, 15
IC7	2	7, 10, 15
IC9	2	7, 10, 15

AC3

CUIT ACO FOR CONNECTION DETAILS

MHz LC filter

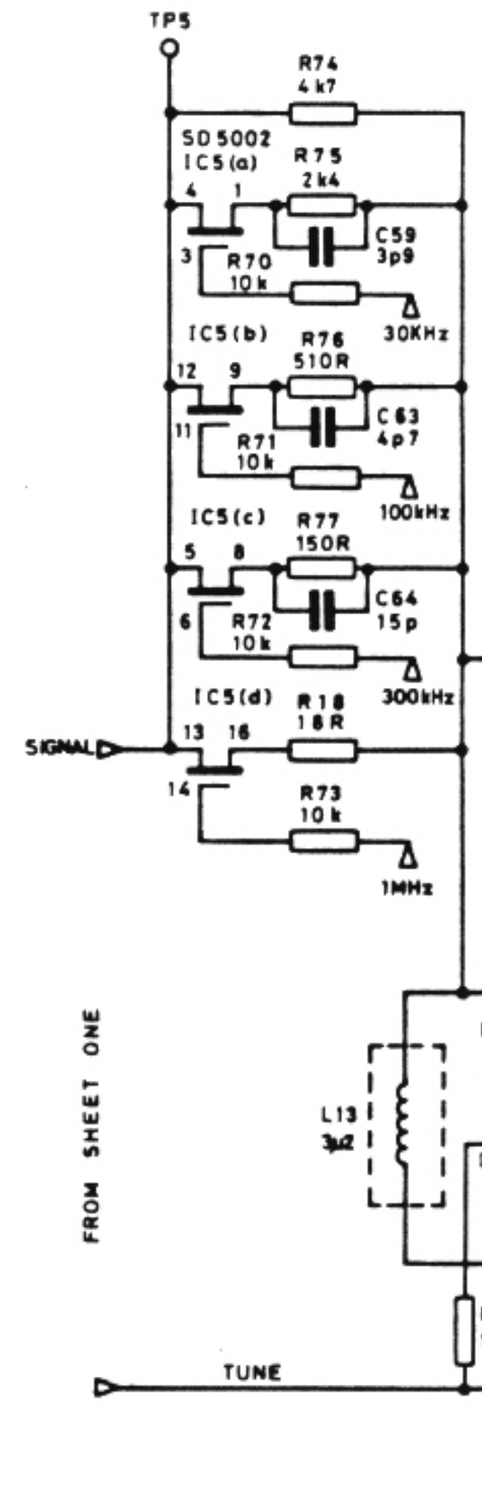
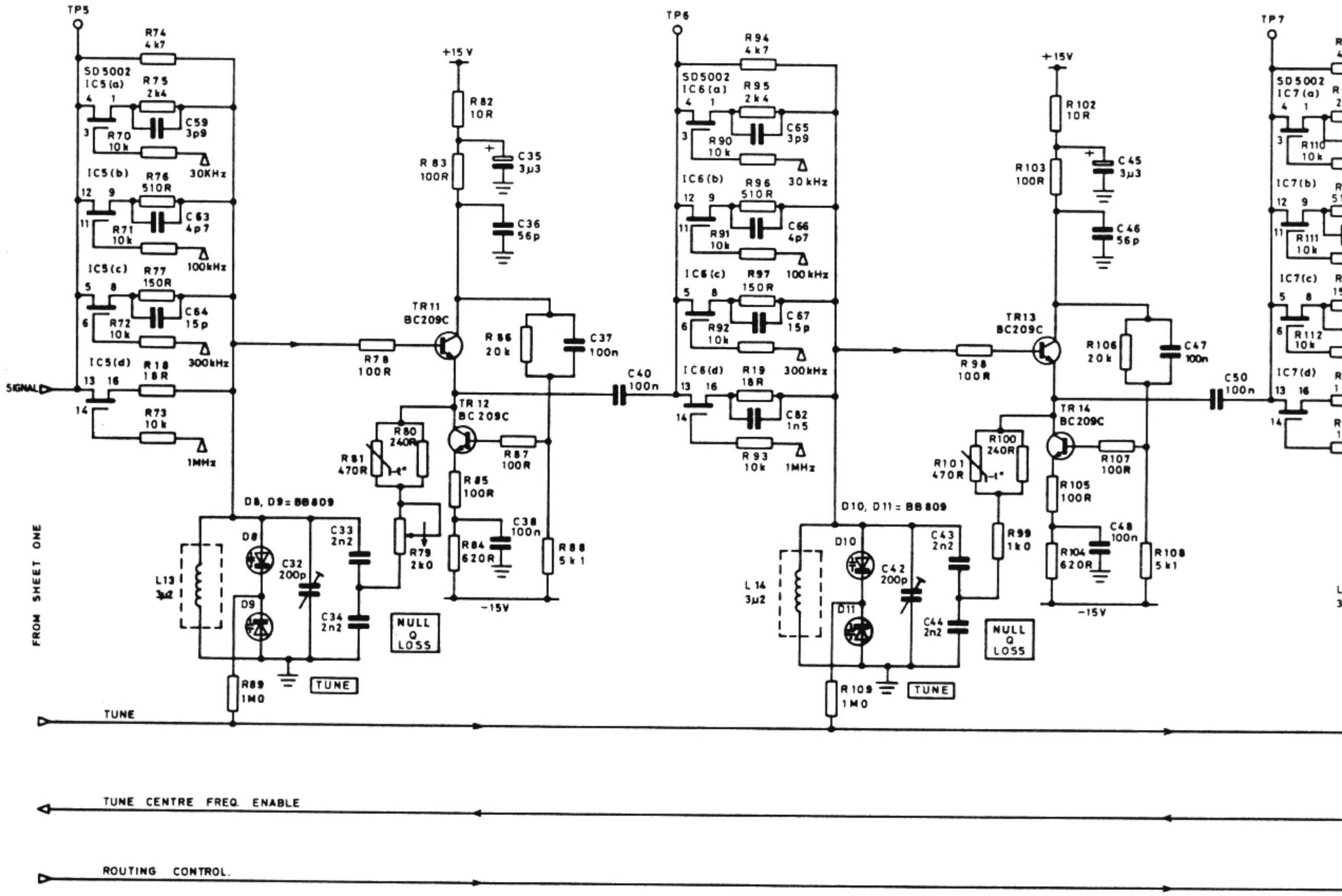

THIRD SW
TP5
R74
4k7
SD5002
IC5(a)
R75
2k4
4
1
C59
3p9
3
R70
10k
IC5(b)
R76
510R
30KHz
12
9
C63
4p7
11
R71
10k
IC5(c)
R77
150R
100kHz
5
8
C64
15p
6
R72
10k
IC5(d)
R18
18R
300kHz
SIGNAL
13
16
14
R73
10k
1MHz
D8.
D8
L13
3µ2
D9
R89
1MO
TUNE
FROM SHEET ONE
TUNE CENTRE FREQ. EN
ROUTING CONTROL.

Fig. 23

May 86

THIRD SWITCHED B.W. FILTER

FOURTH SWITCHED B.W. FILTER



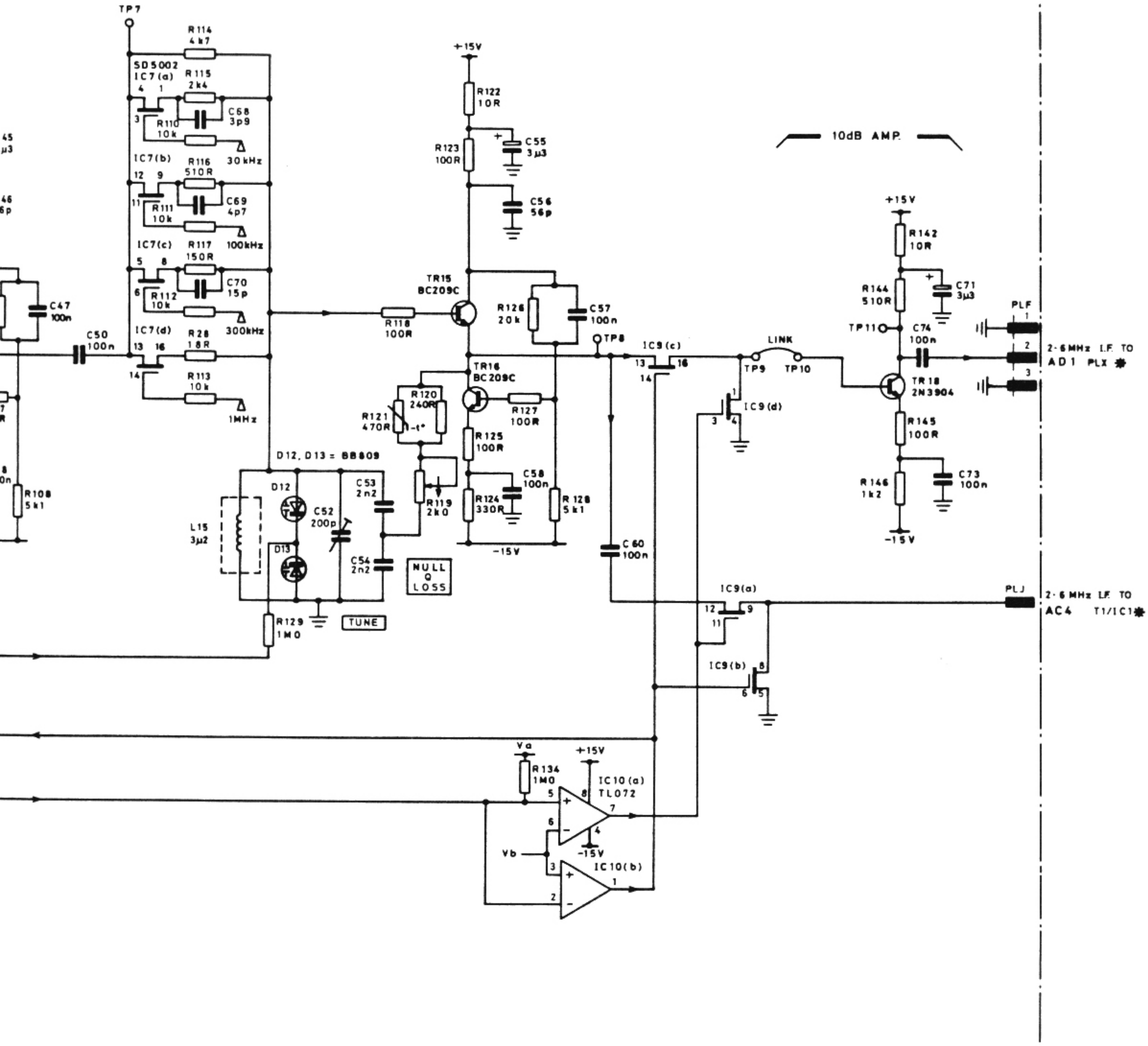
* SEE CIRCUIT AC0 FOR CONNECTION DETAILS.

Drg.No. Z44828-474A
Sh.2 Iss.3

AC3:2.6MHz LC filt

FIFTH SWITCHED BW FILTER

PART OF
AC3
44828-474A

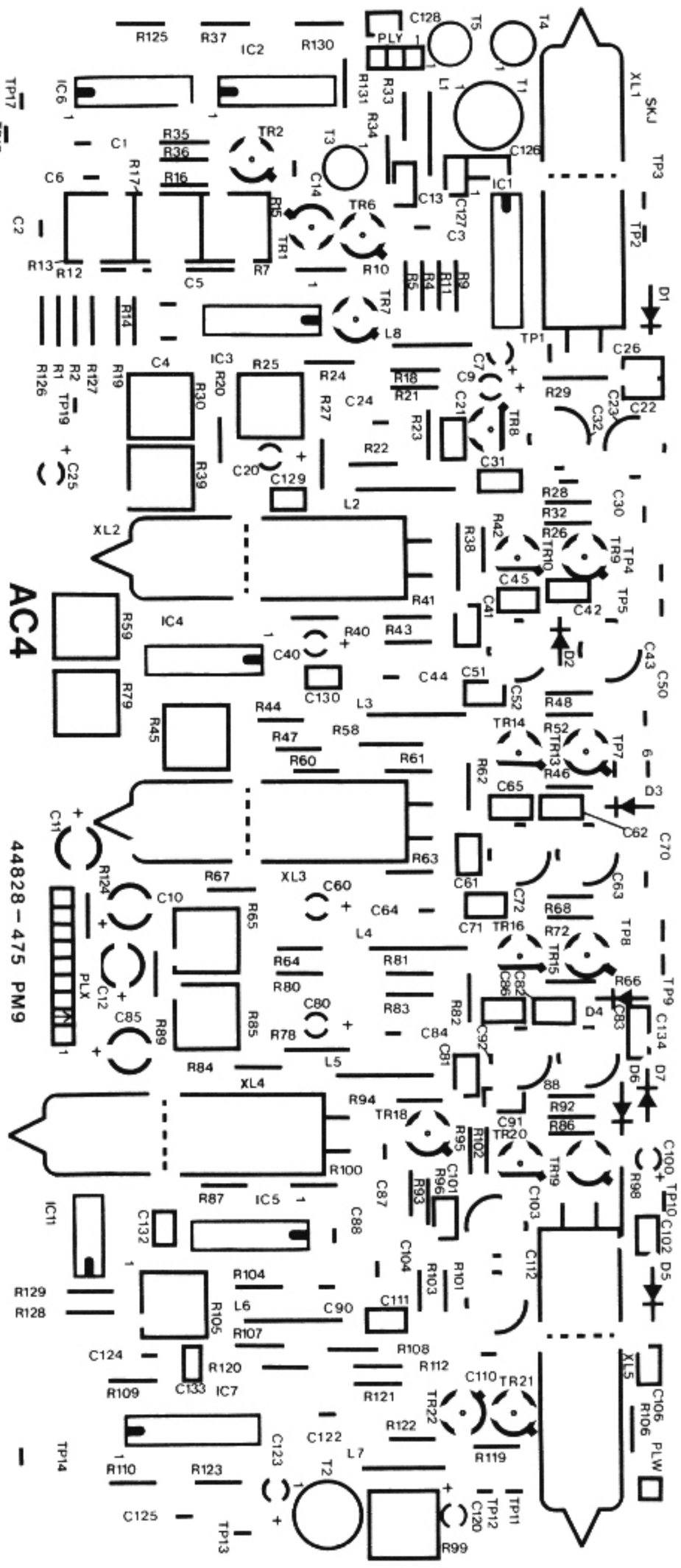


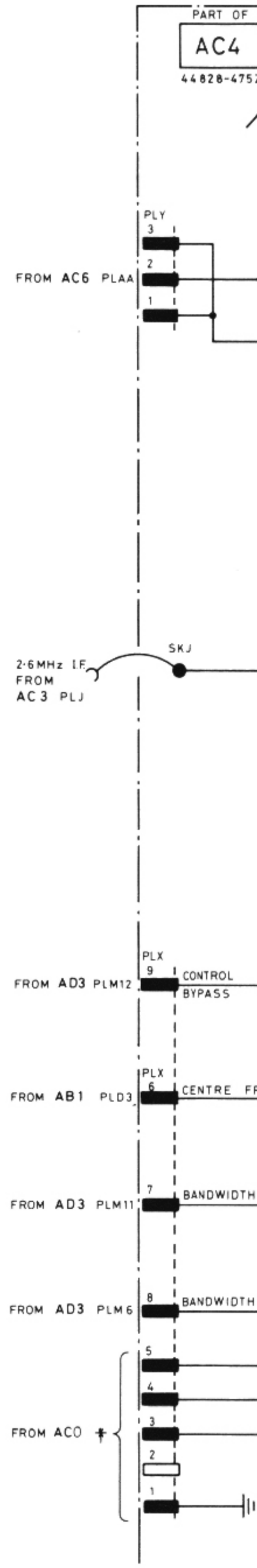
10dB AMP.

AC3

CTION DETAILS.

.6MHz LC filter





Component layout for AC4

Fig. 24
May 86

Drg.
Sh.1

PART OF
AC4
44828-475Z

H.P. FILTER
TTL DRIVER
DIVIDE BY TWO'S
AMP GAIN SWITCHING
GAIN COMPONEN

FROM AC6 PLAA
PLY
R33 3K3
C13 150p
L1 150µ
R34 330R
T3
C14 100n
R35 33k
R36 820R
TR2 2N2369
+5V
R37 1k0
IC2(b) 74S74
IC2(a)
A
B
LOCAL OSC DRIVE TO UP MIXER TO SHEET 2
C127 2n2
C126 2n2
T4
T5
R130 2k0
R131 4k7
C128 2n2
DOWN MIXER
IC1(b) SD5002
IC1(a) SD 5002
T1
TP1
2·6MHz I.F. FROM AC3 PLJ
SKJ
BYPASS INPUT SWITCH
IC1(c) SD5002
IC1(d) SD5002
C1 100n
R1 10k
R2 10k
C2 100n
R128 27k
R129 12k
IC11(a) TL072
IC11(b)
SIGNAL BYPASS TO SHEET 2.
R19 1k0
C6 100n
30Hz GAIN
R17 50k
R16 1k0
IC3(a) LS03
R15 50k
C5 220n
10Hz GAIN
IC3(b)
R14 22k
C4 220n
3Hz GAIN
R13 5k0
SET R13, R17, R15, IN THAT ORDER TO AVOID INTEREACTION.
R12 330R
R7 2k0
TR1 BC308B
R5 12k
R4 1k2
C7 3µ3
L8 1m0
R18 1k2
-15V
C10 33µ
R10 2k0
C3 100n
TR6 BC20
FROM AD3 PLM12
PLX 9
CONTROL BYPASS
R127 10k
TP19
IC6(c) HCT04
IC6(d) HCT04
BYPASS CONTROL LINES TO SHEET 2
FROM AB1 PLD3
PLX 6
CENTRE FREQ. ADJUST
FROM AD3 PLM11
7
BANDWIDTH 1
R125 10k
TP17
IC6(b) HCT04
FROM AD3 PLM6
8
BANDWIDTH 2
R126 10k
TP18
IC6(a) HCT04
FROM AC0 ‡
5 + 15V
4 + 5V
3 - 15V
2
1

SUPPLY LINE TABLE			
I.C. NUMBER	+5V LINE	-15V LINE	GR
IC 1		2	7
IC 2	14		7
IC 3	14		7
IC 4	14		7
IC 5	14		7
IC 6	14		7
IC 7		2	7

‡ SEE CIRCUIT AC0 FOR CONNECTI

Drg.No. Z44828-475Z
Sh.1 Iss.5

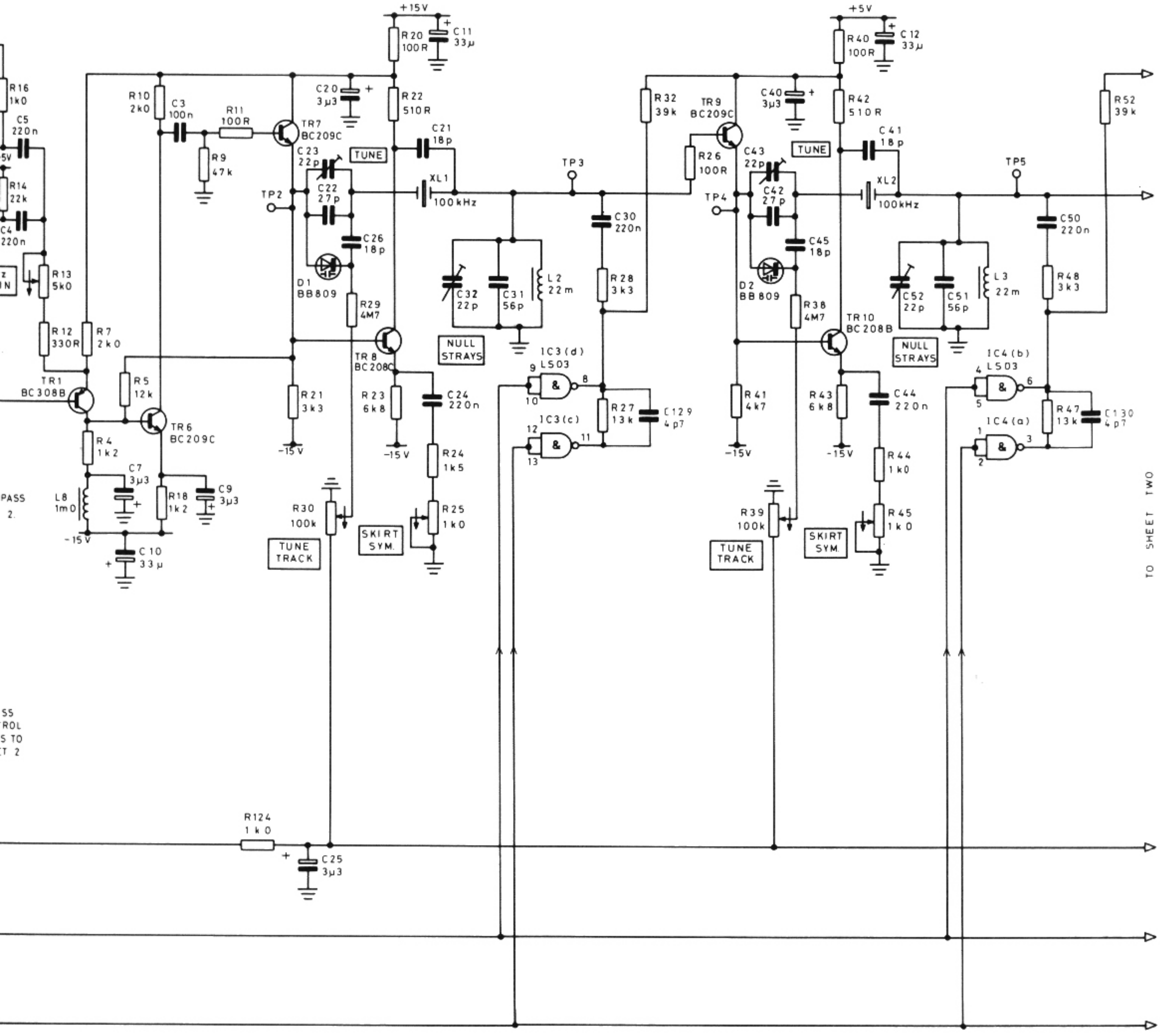
AC4: 100kHZ I.F

WITCHING

FIRST SWITCHED B.W. FILTER

SECOND SWITCHED B.W. FILTER

GAIN COMPONENT AMPLIFIER



SUPPLY LINE TABLE			
BER	+5V LINE	-15V LINE	GROUND
		2	7 10 15
	14		7
	14		7
	14		7
	14		7
	14		7
		2	7 10 15

BANDWIDTH SELECTION TABLE		
B.W.	PLX 7	PLX 8
30 Hz	HIGH	HIGH
10 Hz	HIGH	LOW
3 Hz	LOW	LOW

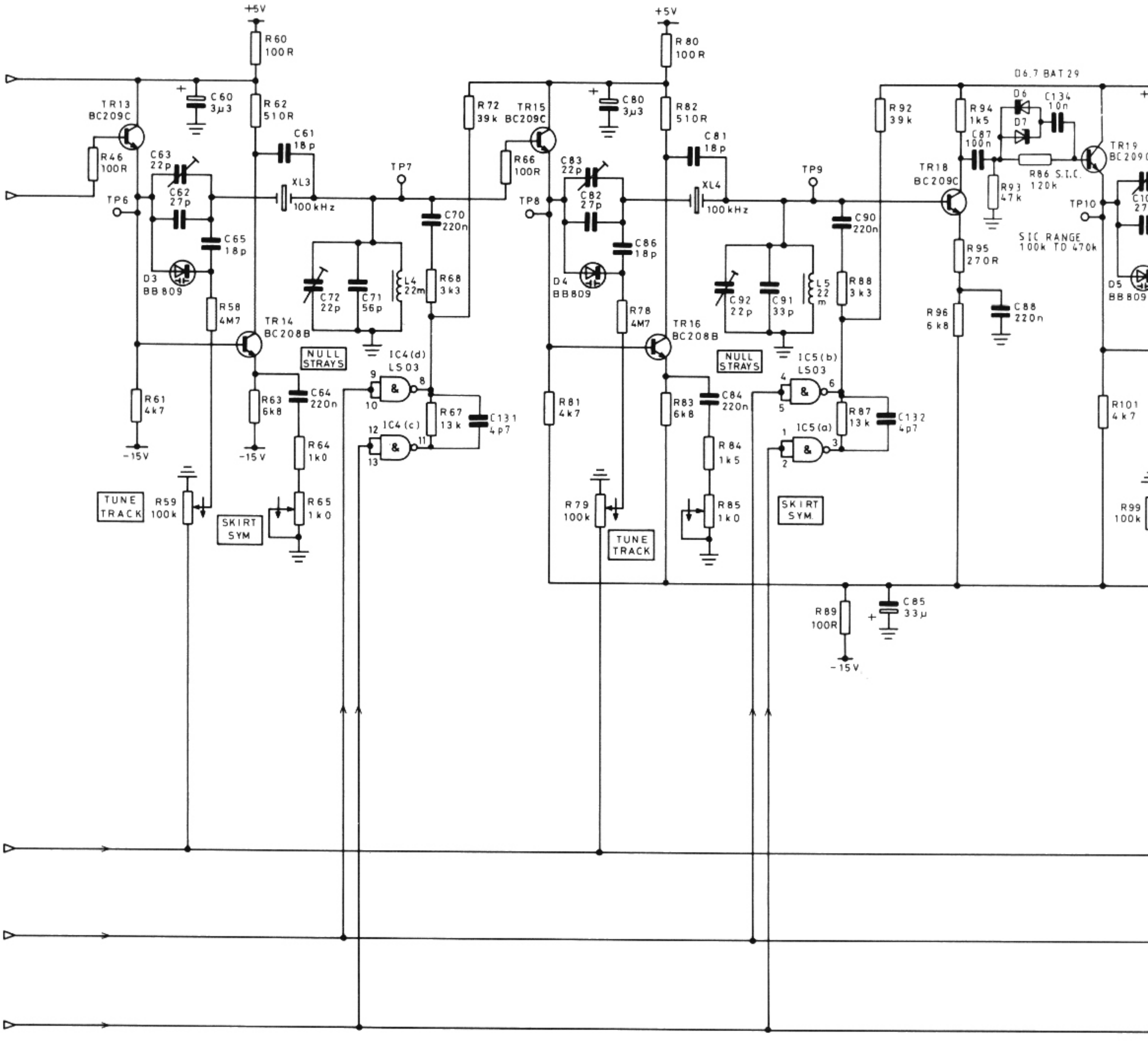
EE CIRCUIT AC0 FOR CONNECTION DETAILS.

C4 : 100kHZ I.F. crystal filter

THIRD SWITCHED B.W. FILTER

FOURTH SWITCHED B.W. FILTER

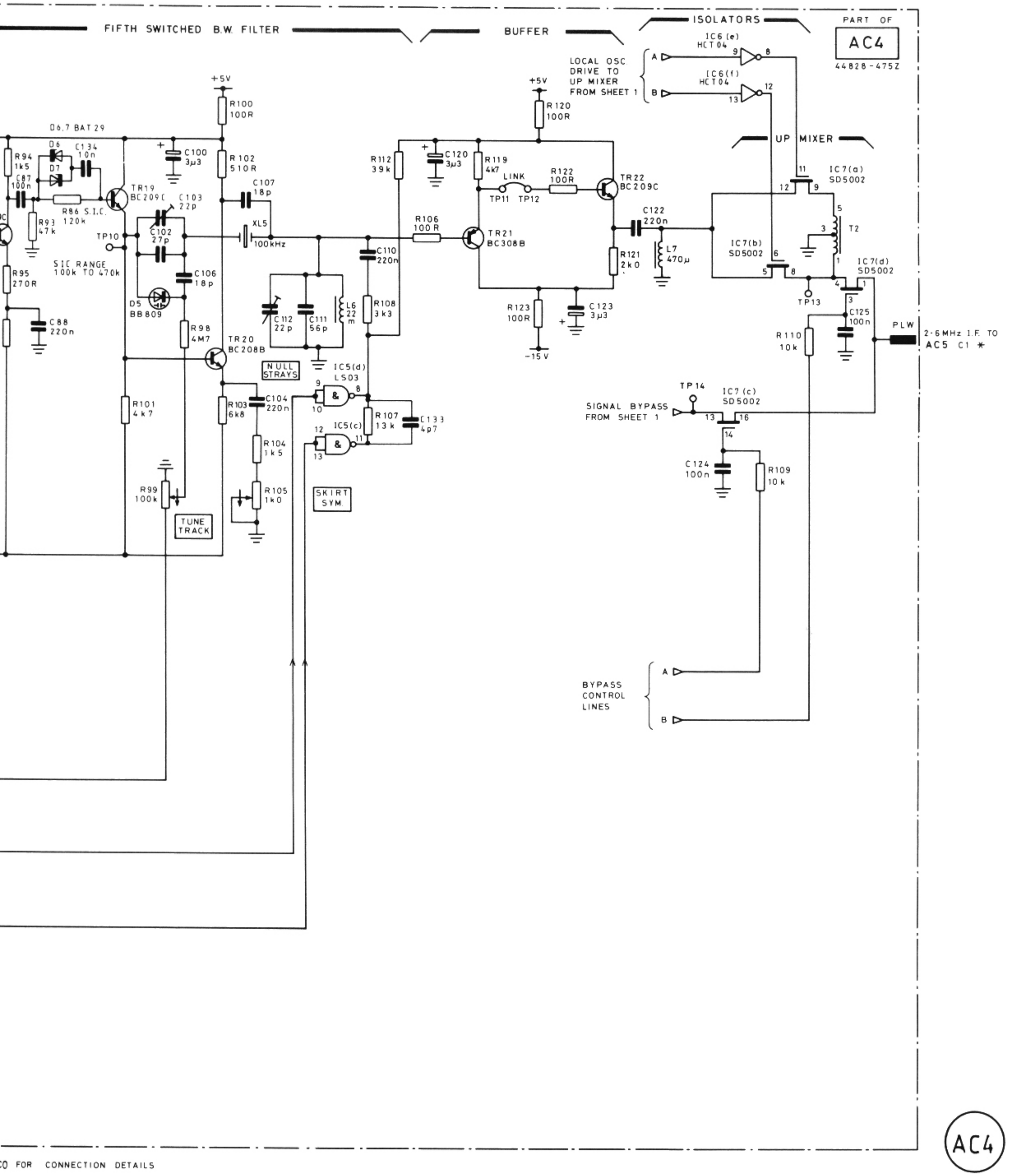
FIFTH SWI



* SEE CIRCUIT AC0 FOR CONNECTION DETAILS

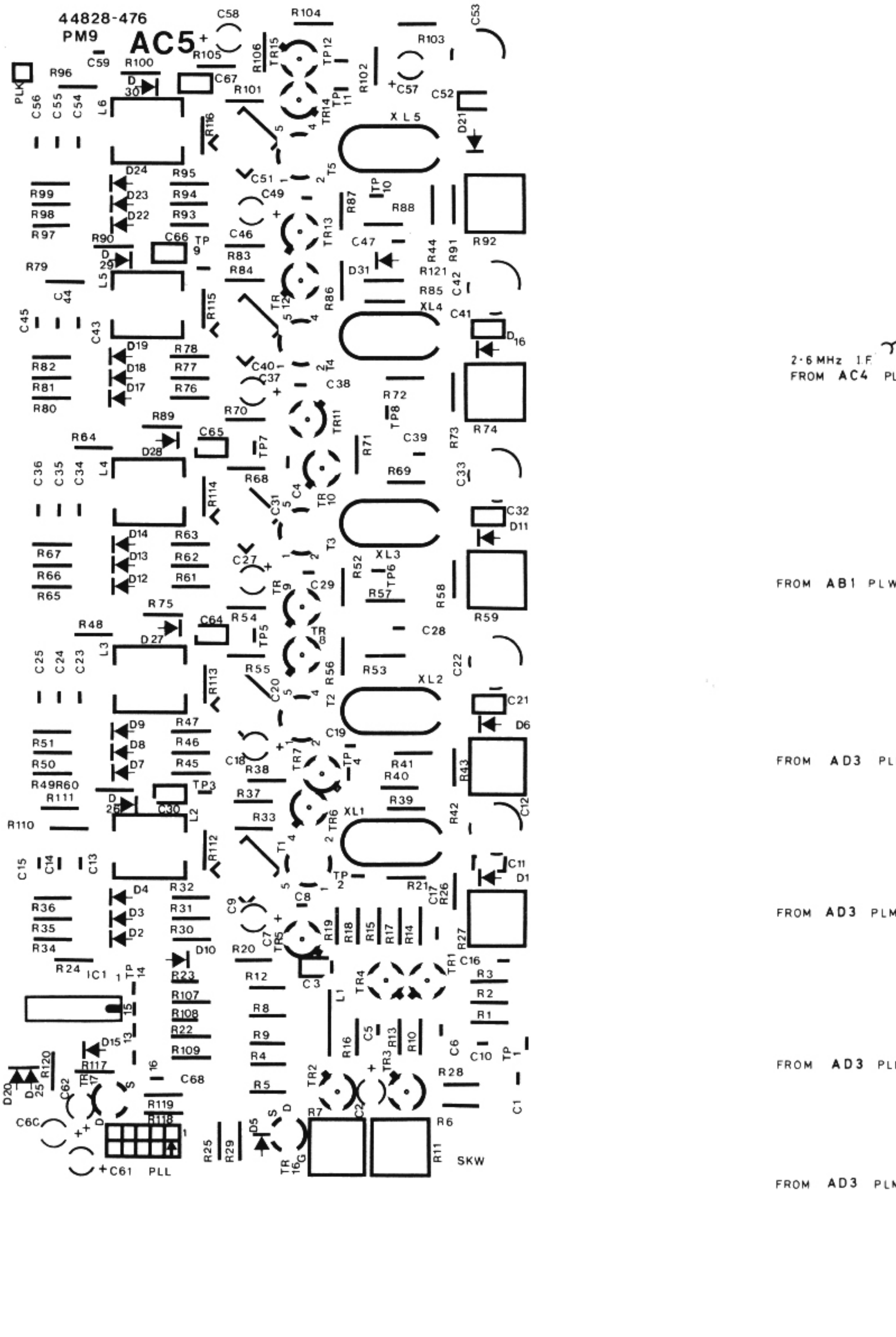
Drg.No. Z44828-475Z
Sh.2 Iss.5

AC4: 100kHZ I.F.



CO FOR CONNECTION DETAILS

: 100kHZ I.F. crystal filter



Component layout for AC5

Fig. 26

May 86

Drg. No
Sh. 1

PART OF
AC5
44828-476X

VARIABLE GAIN AMP

FIRST SWITCHED B.W. FILTER

GAIN SWITCHING

+5V
+15V
R12 10R
D10 1N4148
C2 3µ3
R5 47k
R9 47k
TR2 MPSL08
TR3 MPSL08
R4 33k
R8 33k
R7 2k0
R11 5k0
100Hz GAIN
300Hz GAIN
R16 2k0
L1 100µ
C3 27p
R19 100R
TR5 BC209C
R20 10R
C7 3µ3
SKIRT SYM.
C9 5p5
NULL STRAYS
R6 1k6
C6 100n
R10 3k3
R13 2k2
R28 100k
TP2
C8 100n
R18 4k7
C17 100n
R21 2k2
-15V
T1
R33 43k
L2 125µ
R30 820R
R31 2k7
R1 10k
TR1 BFR99
TP1
SKW
2·6MHz IF FROM AC4 PLW
R3 100R
R15 100R
TR4 BFY90
C30 10p
D2 1N3062
D3 1N3062
XL1 2·6MHz
(B)
C1 100n
R2 39k
R14 1k8
C5 100n
R17 1k0
C10 100n
D26 BB 405B
C15 100n
C14 100n
R26 1M0
D1 BB405B
C11 10p
C12 22p
R60 1M0
R34 2k7
R35 2k4
TUNE
TUNE TRACK
R27 100k
PLL
1
FROM AB1 PLW 3
CENTRE FREQ ADJUST
R25 1k0
TR16 BF245
R29 470k
C16 100n
D5 1N4148
+5V
+5V
+15V
R108 1M0
R23 27k
IC1(c) TL074
TP15
2
SELECT 100Hz
FROM AD3 PLM 8
9
10
8
11
-15V
R118 1k0
TR17 BF245
+15V
R110 56k
R119 470k
D20 1N4148
C68 100n
R111 20k
D25 1N4148
+5V
TP14
R107 1M0
IC1 (b)
6
7
9
SELECT 300Hz
FROM AD3 PLM10
5
R117 1M0
+5V
TP13
R22 1M0
IC1(a)
2
1
3
FROM AD3 PLM7
SELECT 1KHz
R24 12k
+5V
R109 1M0
R120 100k
TP16
6
C.F ADJUST ENABLE
FROM AD3 PLM12
D15 1N4148
13
12
IC1(d)
14

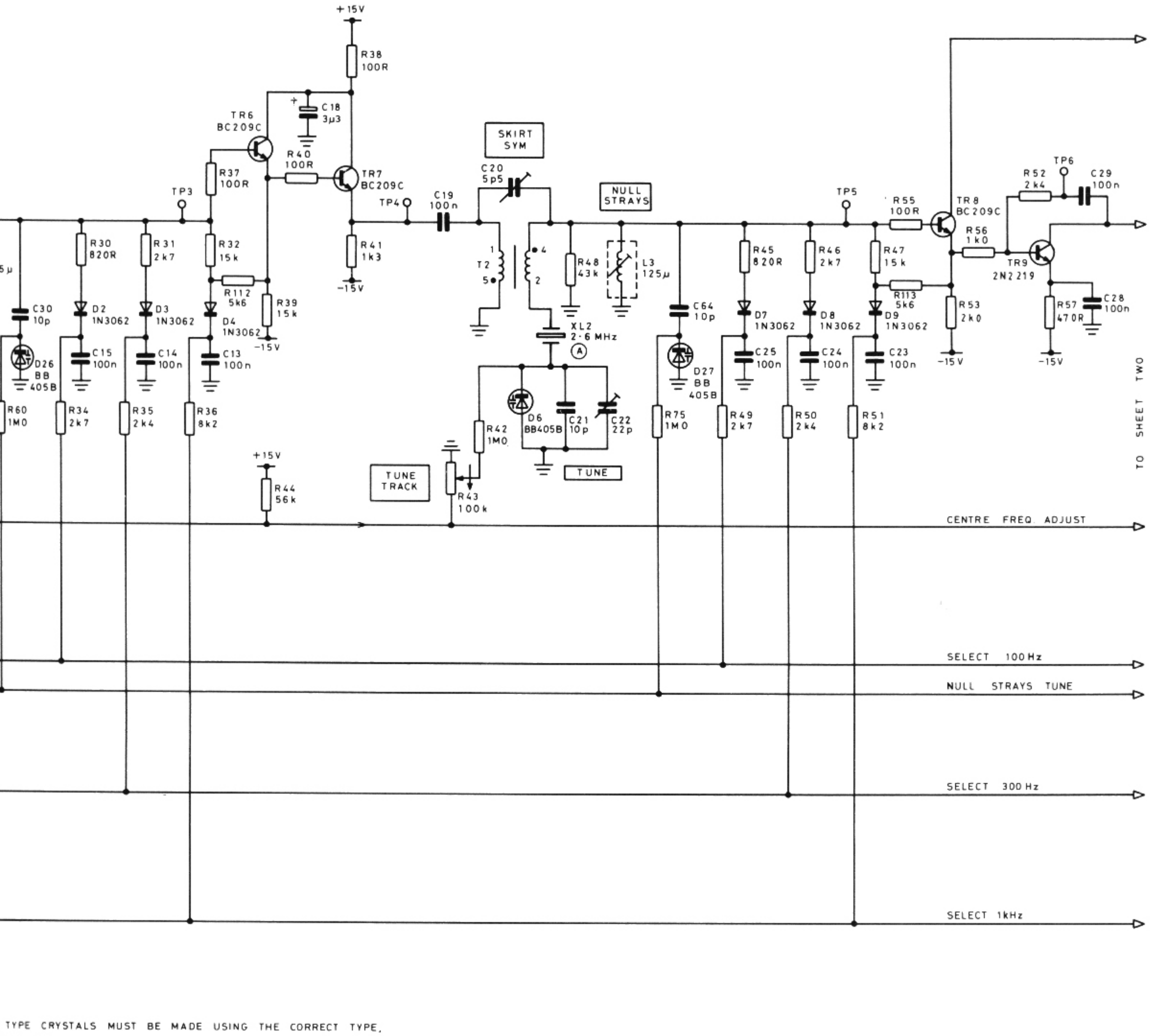
REPLACEMENT OF (A) OR (B) TYPE CRYSTALS MUST BE MA
OTHERWISE SPURIOUS RESPONSES 200kHz HIGHER THAN TH

Drg.No.Z44828-476X
Sh.1 Iss.5

* SEE CIRCUIT AC0 FOR CONNECTION DETAILS.

AC5:2.6MHz crystal fil

B.W. FILTER | BUFFER | SECOND SWITCHED B.W. FILTER | BUFFER



TYPE CRYSTALS MUST BE MADE USING THE CORRECT TYPE,
SES 200 kHz HIGHER THAN THE WANTED RESPONSE MAY OCCUR.

AC5

FOR CONNECTION DETAILS.

lz crystal filters

Fig. 26
Chap. 7
Page 61/62

THIRD SWITCHED B.W. FILTER

BUFFER

FOURTH SWITCHED B.W. FILTER

PART OF
AC5
44828-476X

+15V

R54
100R

C27
3µ3

SKIRT SYM

C31
5p0

NULL STRAYS

T3

R64
43k

L4
125µ

XL3
2·6MHz
(B)

D11
BB405B

C32
10p

C33
22p

R58
1M0

TUNE

TUNE TRACK

R59
100k

CENTRE FREQ. ADJUST

FROM SHEET ONE

C65
10p

D28
BB
405B

R89
1M0

R61
820R

D12
1N3062

C36
100n

R65
2k7

R62
2k7

D13
1N3062

C35
100n

R66
2k4

TP7

R68
100R

R63
15k

D14
1N3062

C34
100n

R67
8k2

TR10
BC209C

C37
3µ3

R71
100R

TR11
BC209C

R114
5k6

R69
15k

−15V

C39
100n

TP8

C38
100n

R72
2k7

+15V

C4
100n

R70
100R

SKIRT SYM.

C40
5p5

T4

R79
43k

L5
125µ

XL4
2·6MHz
(A)

D16
BB405B

C41
10p

C42
22p

R73
1M0

TUNE

TUNE TRACK

R74
100k

NULL STRAYS

C66
10p

D29
BB
405B

R90
1M0

R76
820R

D17
1N3062

C45
100n

R80
2k7

R77
2k7

D18
1N3062

C44
100n

R81
2k4

TP9

R84
100R

R78
15k

R115
5k6

D19
1N3062

C43
100n

R82
8k2

SELECT 100Hz

NULL STRAYS TUNE

SELECT 300Hz

SELECT 1KHz

FILTER

OF
5
-476X

BUFFER

FIFTH SWITCHED B.W. FILTER

BUFFER

+15V

R 83
100R

C46
3µ3

SKIRT
SYM.

TP
10

C49
100n

R87
2k7

C51
5p5

NULL
STRAYS

TP9

R84
100R

TR12
BC 209C

R121
16k

D31
1N4148

TR13
2N2219

T5
1
4
2
5

R96
43k

L6
125µ

R76
820R

R77
2k7

R78
15k

R115
5k6

R86
1k0

R85
2k0

D17
1N3062

D18
1N3062

D19
1N3062

C45
100n

C44
100n

C43
100n

R80
2k7

R81
2k4

R82
8k2

-15V

R88
470R

C47
100n

XL5
2·6 MHz

B

C67
10p

D30
BB
405B

R100
1M0

R97
2k0

R98
2k4

R99
8k2

D21
BB405B

C52
10p

C53
22p

R91
1M0

TUNE
TRACK

R92
100k

TUNE

R93
820R

R94
2k7

R95
15k

D22
1N3062

D23
1N3062

D24
1N3062

C56
100n

C55
100n

C54
100n

R116
5k6

R101
100R

R102
3k6

TP11

TP12

R104
100R

TR14
BCY71

TR15
2N2219

C59
100n

PLK

2·6 MHz I.F. TO
AD1 PLY

C57
3µ3

R106
470R

C58
3µ3

R105
10R

-15V

PLL
5

+15V

C60
3µ3

7

+5V

C61
3µ3

FROM
ACØ

4

-15V

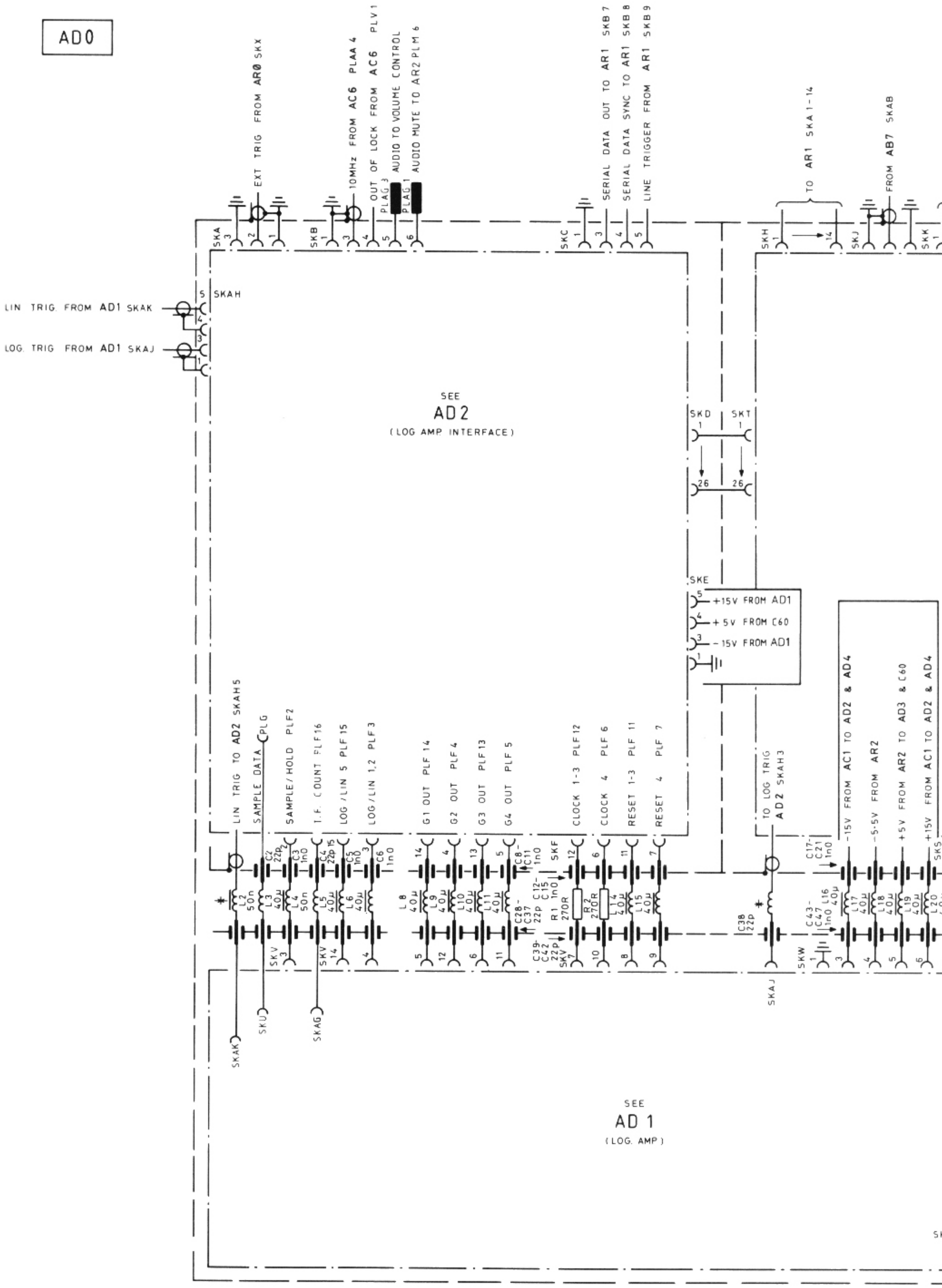
C62
3µ3

8

AC5

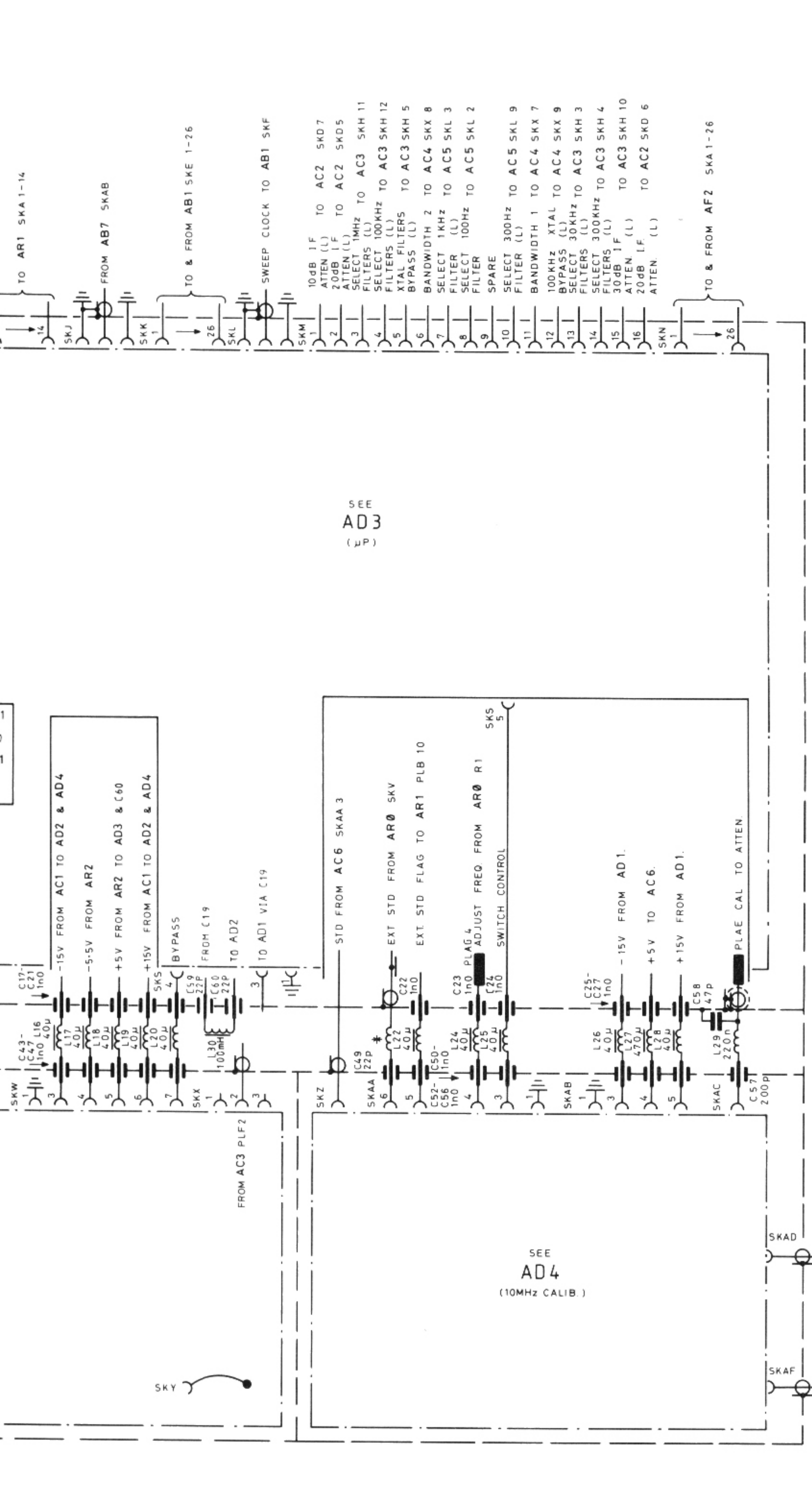
Hz crystal filters

AD0



Drg. No. Z44990-451
Sh. 2 Iss. 4

AD0 : AD t

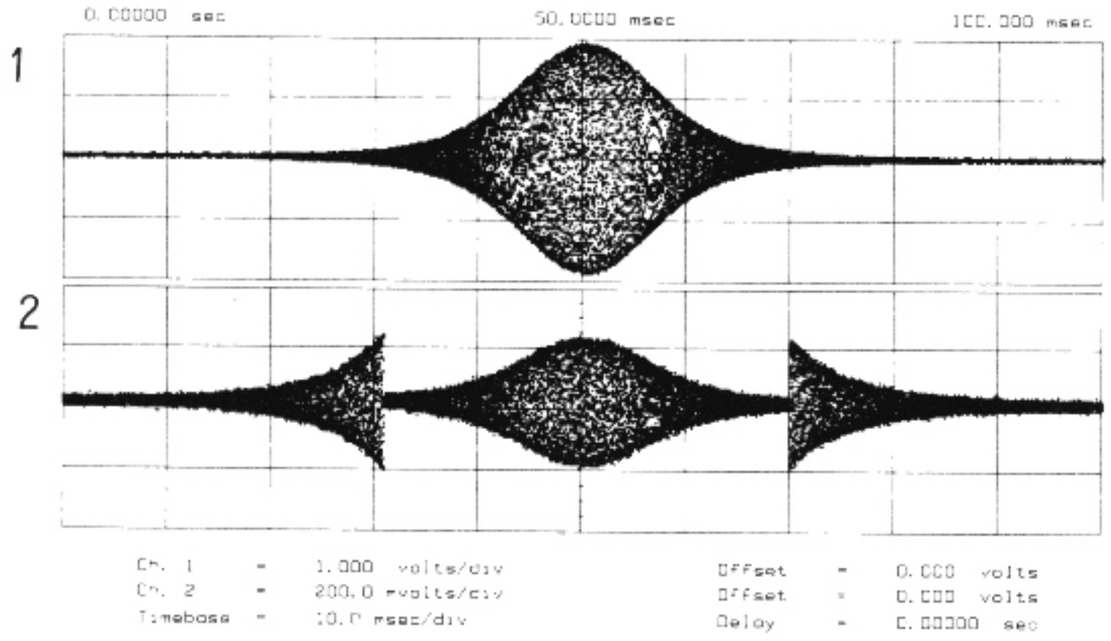


ADO: AD tray interconnection

1
2

BOARD : AD1

TEST POINT : TP1 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : TP2 for Ch. 2

PROCEDURE :

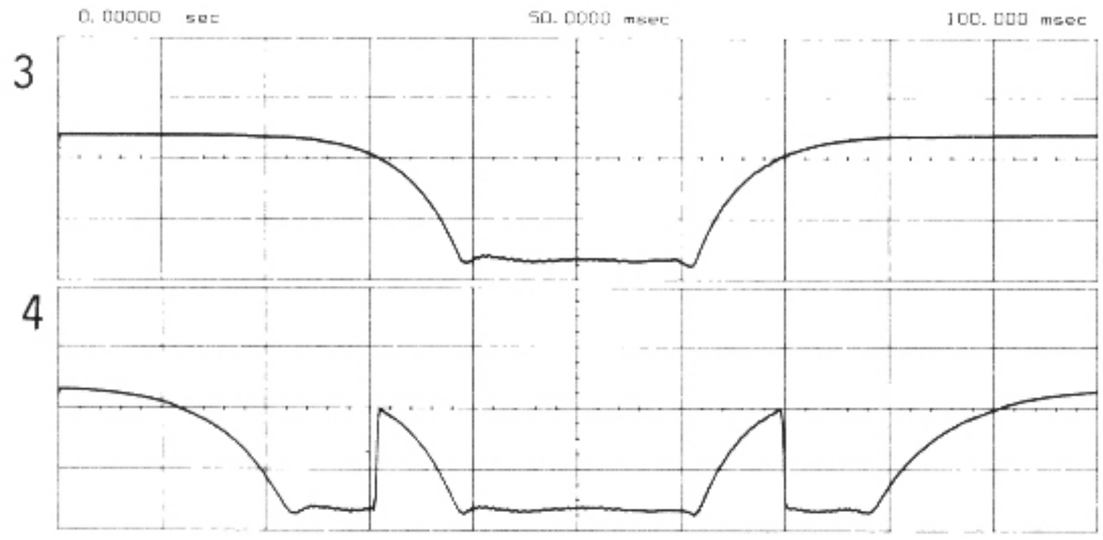
1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

3
4

BOARD : AD1

TEST POINT : TP3 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : TP6 for Ch. 2

PROCEDURE :

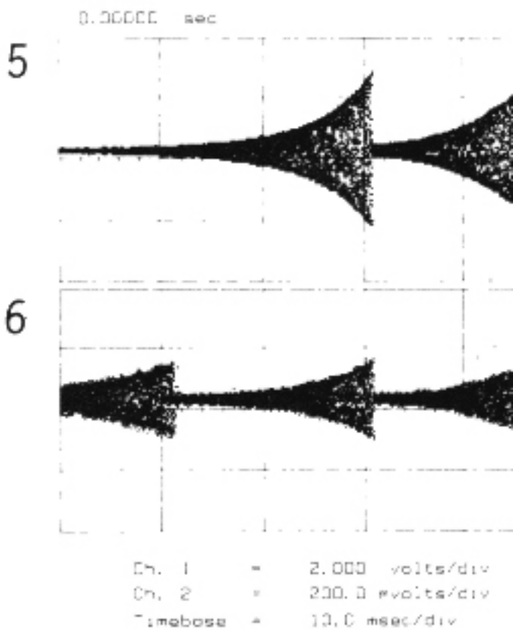
1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

5
6

BOARD : AD1

TEST POINT : TP4 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : TP5 for Ch. 2

PROCEDURE :

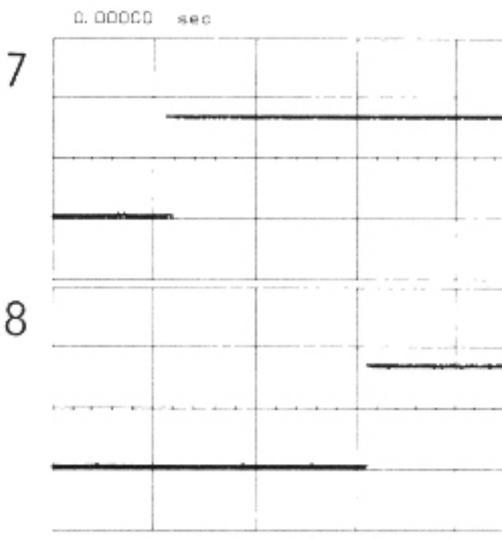
1. Press PRESET then select the

Span	1 k
Filter bandwidth	1 k
Ref. freq.	10
Ref. level	-10
Input	10

7
8

BOARD : AD1

TEST POINT : PLV12 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : PLV5 for Ch. 2

PROCEDURE :

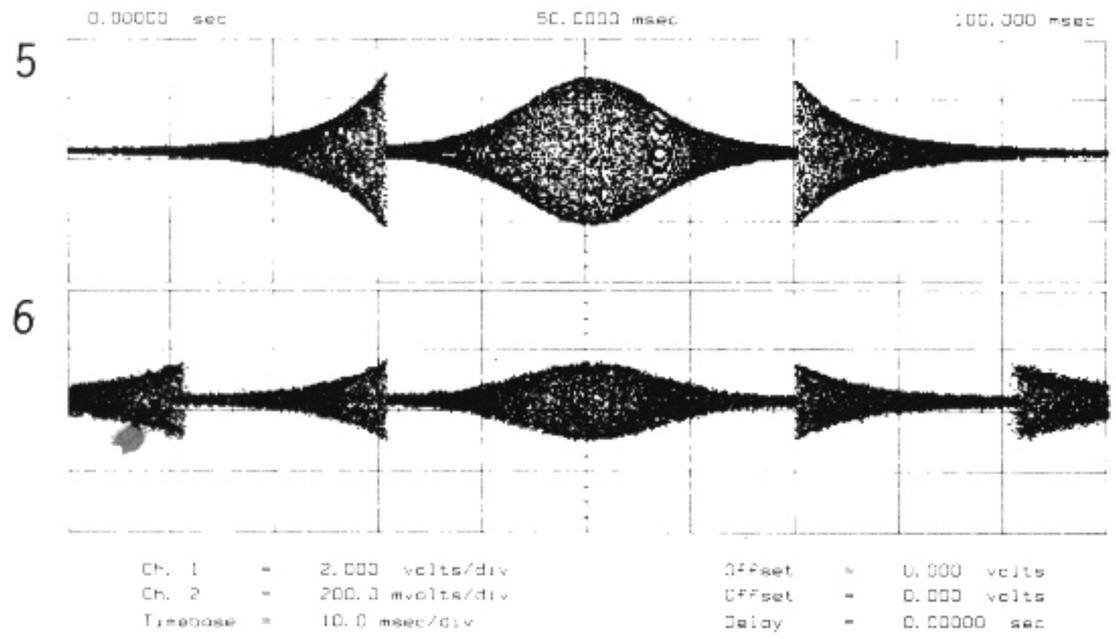
1. Press PRESET then select the

Span	1 k
Filter bandwidth	1 k
Ref. freq.	10
Ref. level	-10
Input	10

Fig. 29a
Chap. 7
Page 66

5
6 BOARD : AD1

TEST POINT : TP4 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : TP5 for Ch. 2

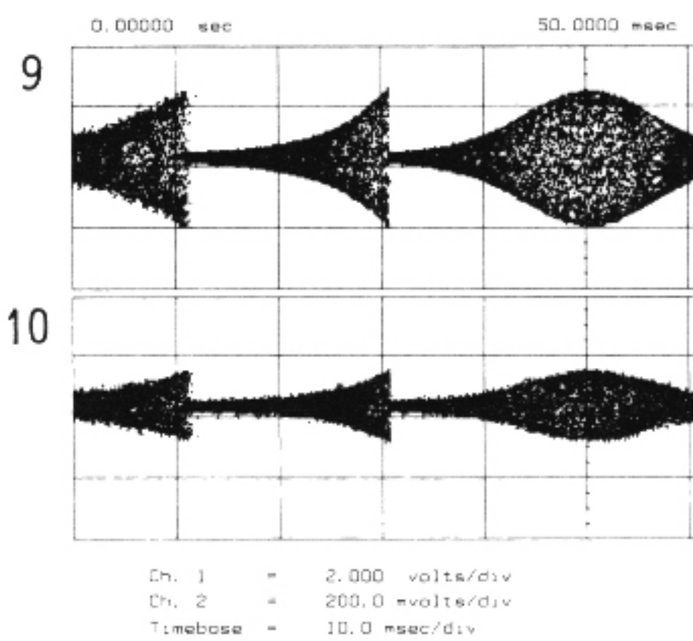
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

9
10 * BOARD : AD1

TEST POINT : TP7 (Fig. 29) for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : TP8 (Fig. 30) for Ch. 2

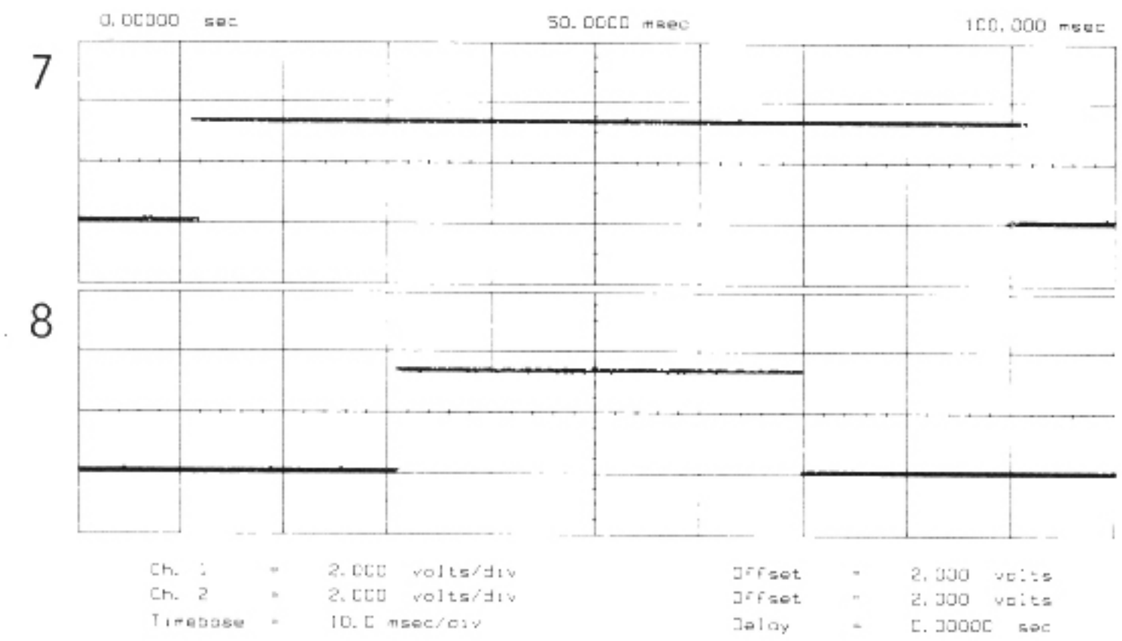
PROCEDURE :

1. Press PRESET then select the following

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz stand

7
8 BOARD : AD1

TEST POINT : PLV12 for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



TEST POINT : PLV5 for Ch. 2

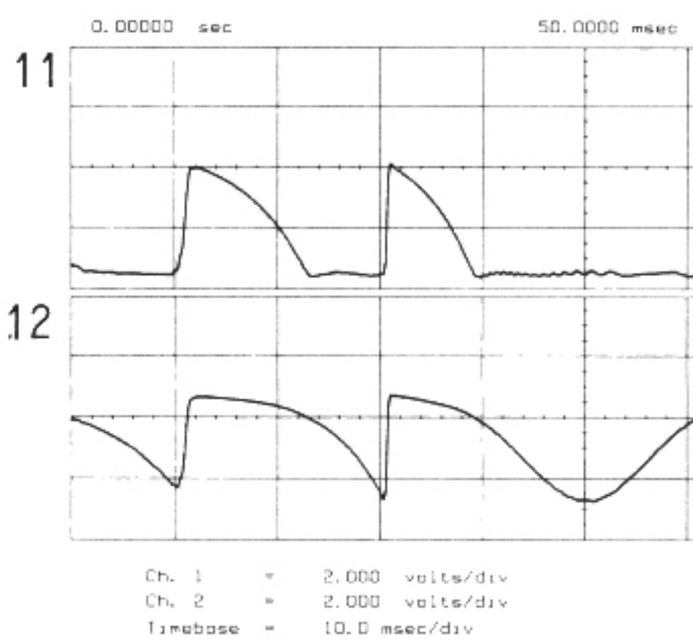
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

11
12 * * BOARD : AD1

TEST POINT : TP9 (Fig. 30) for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



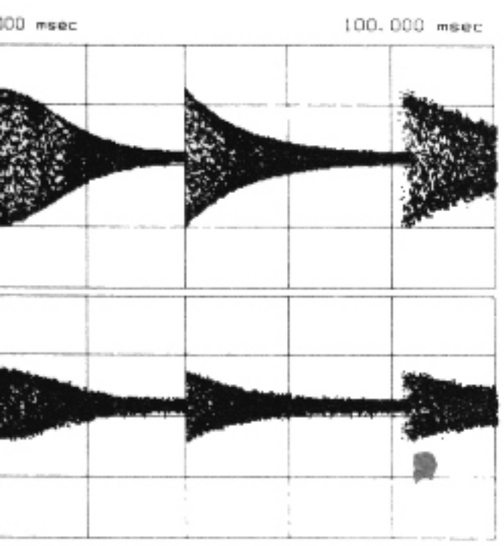
TEST POINT : TP12 (Fig. 30) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz stand

Waveforms for AD1



cct. drg. Fig. 30 refers

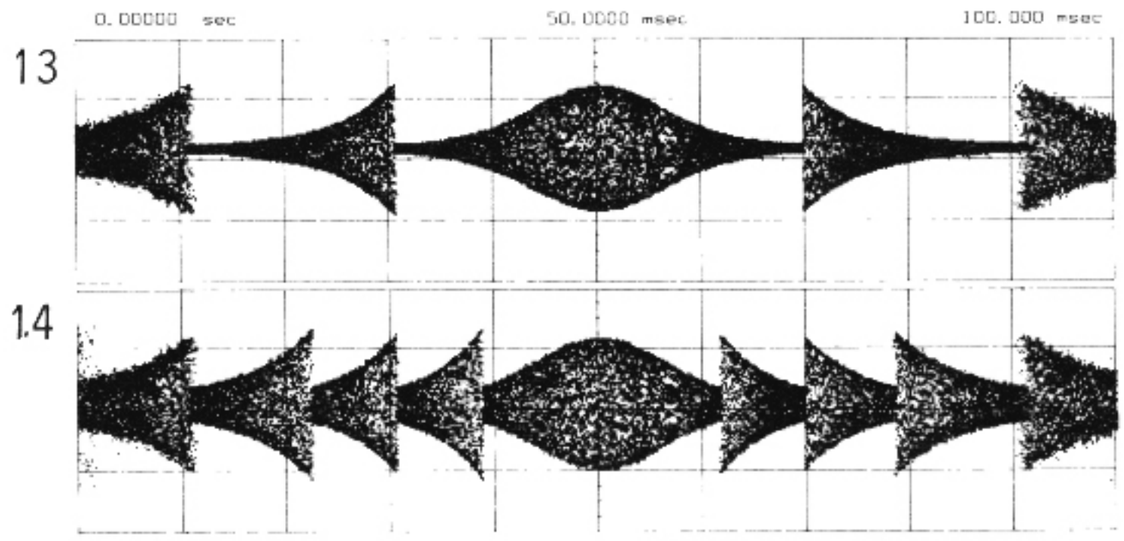
lowing 2382 settings:

DIV

m
standard cal. signal

13 * BOARD : AD1
14 *

TEST POINT : TP10 (Fig. 30) for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



cct. drg. Fig. 30 refers

TEST POINT : TP11 (Fig. 30) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

cct. drg. Fig. 30 refers

2

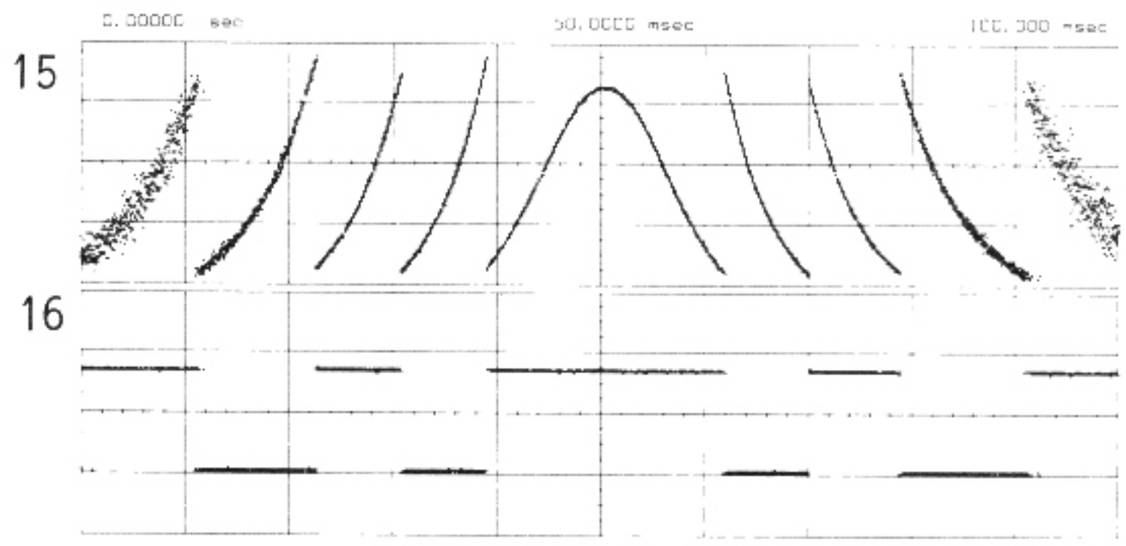
lowing 2382 settings:

/DIV

z
Bm
z standard cal. signal

15 * BOARD : AD1
16 *

TEST POINT : PLU (Fig. 30) for Ch. 1
SCOPE SETTING
TRIGGER PT : AD3 TP3 falling edge



cct. drg. Fig. 30 refers

TEST POINT : PLV11 (Fig. 30) for Ch. 2

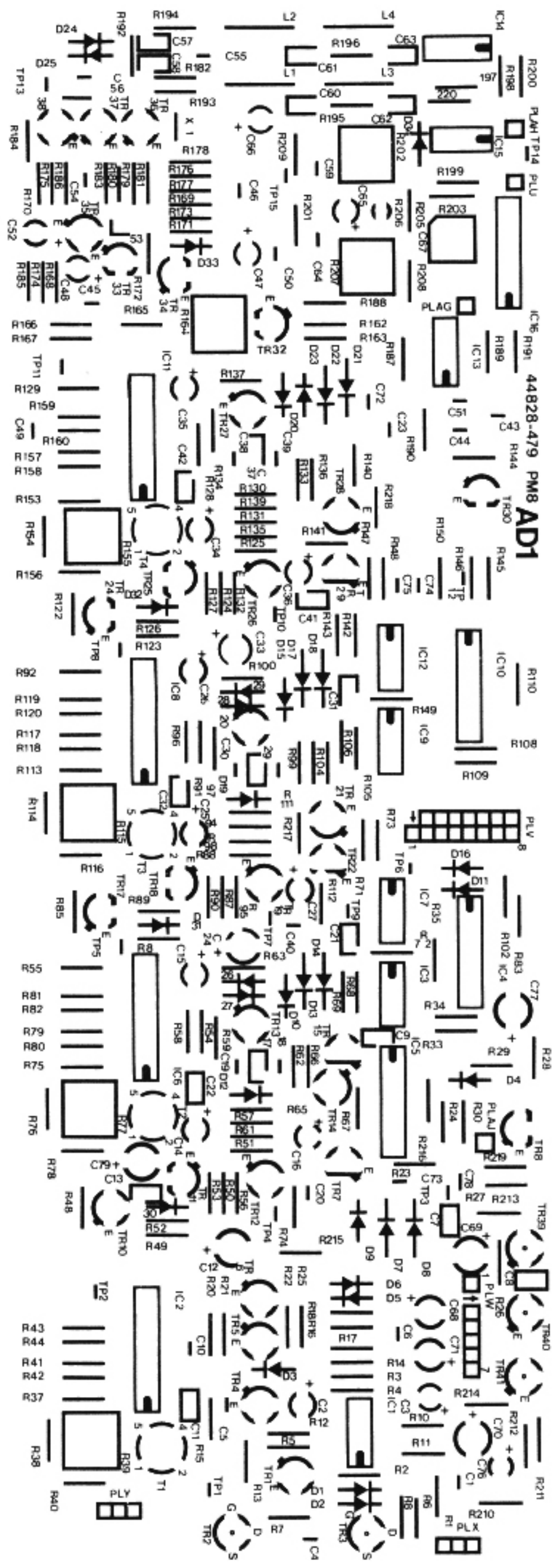
PROCEDURE :

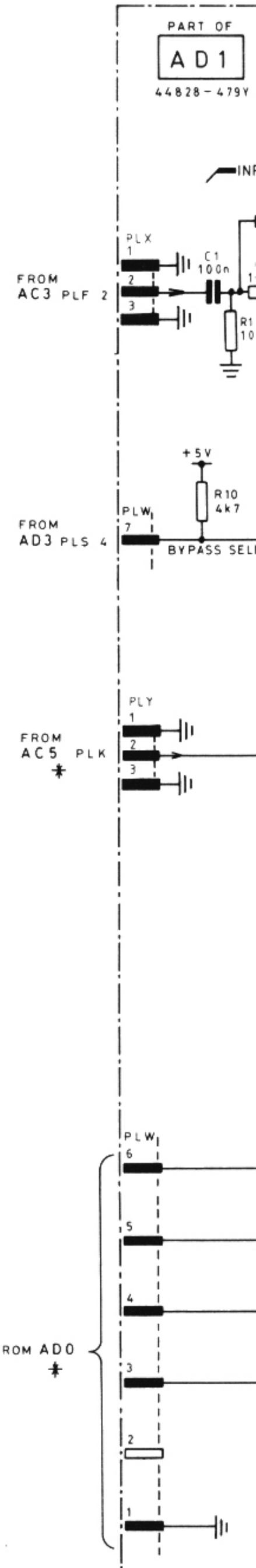
1. Press PRESET then select the following 2382 settings:

Span	1 kHz/DIV
Filter bandwidth	1 kHz
Ref. freq.	10 MHz
Ref. level	-10 dBm
Input	10 MHz standard cal. signal

Fig. 29a

May 86





Component layout for AD1

Drg.No
Sh.1

Fig. 29

May 86

PART OF
AD1
44828-479Y

INPUT SOURCE SELECTION

FROM AC3 PLF 2

PLX
1
2
3
C1 100n
R1 10k
R2 100R
TR1 BC209C
R5 300R
C4 100n
TR3 2N4857
R8 470k
D2 1N4148
R6 6k2
+5V
R11 27K
+15V
R10 4k7
PLW
7
FROM AD3 PLS 4
BYPASS SELECT
IC1(b) TLO72 IC1(a)
R12 12k
D1 1N4148
R7 470k
PLY
FROM AC5 PLK *
TR2 2N4857

20dB AMPLIFIER

1
TP1
R13 100R
TR4 BC209C
C5 10n
R14 2k7
R15 27k
TR5 BC209C
R16 1k0
R18 180R
D5 D6 1N 4148
C6 10n
C3 3µ3
R4 10R
-15V
+15V
R3 10R
C2 3µ3
R17 5k6
D9 1N4148
R20 62k
C10 100n
D3 1N 4148
R21 100R
TR6 BC209C
R25 4k7
R22 6k2
R215 470R

0/25·6dB ATTENUATOR

25·6dB AMPLIFIER

T1
R40 54R2
R38 4R7
R37 1k0
FINE ADJ
R39 10R
IC2(b) SD5002
R42 4k7
IC2(a) SD5002
R41 4k7
C11 12p
R48 100R
TR10 BCY71
2
TP2
R50 3k6
C12 100µ
R49 150R
C13 4p7
R52 4k3
D30 BAT42
R53 2k0
C14 1µ0
C79 3u3
IC2(d) SD5002
R44 18k
IC2(c) SD5002
R43 18k
D7 6V

LEVEL DETECTOR

GATED SCHMITT

+15V
R24 560k
R33 470R
R23 10R
TR7 BC308B
TP3
C9 1n0
D4 1N4148
R29 1k5
3
IC3 LM311
R34 22k
C23 100n
R35 1k6
IC4(a) HCT74
S
D
CLK
R
Q
8

TRIGGER DRIVE DETECTOR

+5V
R210 10R
C76 10µ
R211 1k2
R212 100R
TR39 2N2369
TR41 MPSL08
C7 1n0
TR40 2N2369
R213 10k
R214 15k
C8 100p
R26 10k
-15V

+5V
R219 10R
C78 100n
R27 1k0
TR8 MPSL08
C77 3µ3
R28 2k7
R30 4k7

FROM AD0 *
PLW
6
5
4
3
2
1
+15V
C71 33µ
+5V
C70 33µ
-5V
C69 33µ
-15V
C68 33µ

SUPPLY LINE TABLE

IC NUMBER	+5V	-5V	GROUND
IC2		2	
IC3	8	4	1
IC4	14		7
IC5	14		7
IC6		2	
IC7	8	4	1
IC8		2	
IC9	8	4	1
IC10	14		7
IC11		2	
IC12	8		1
IC16			13

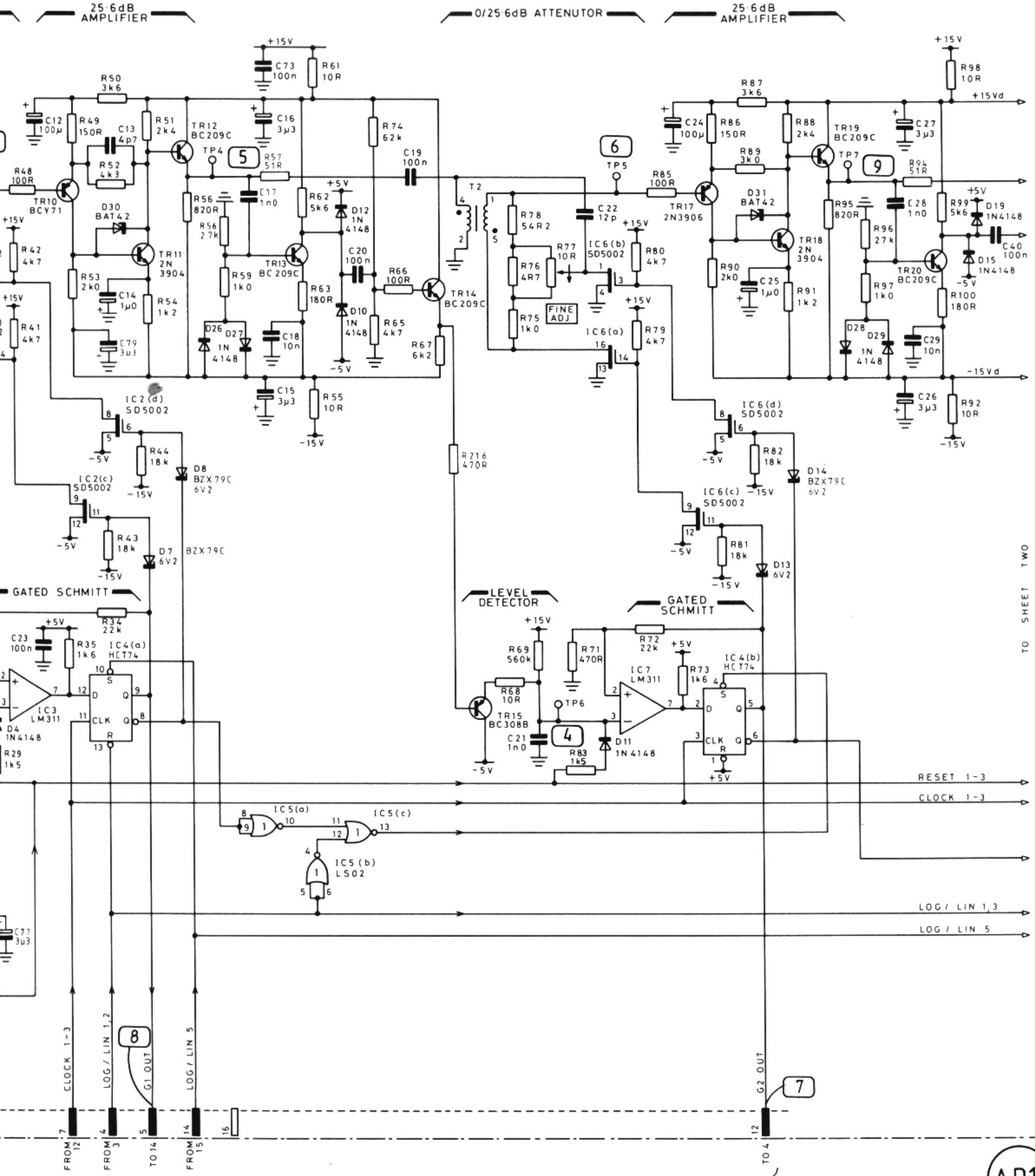
PLAJ LOG TRIG
PLV RESET 1-3
CLOCK 1-3
LOG/LIN 1,2
8
G1 OUT

TO AD2 PLAH 3
FROM 11
FROM 12
FROM 3
TO 14

* SEE CIRCUIT AD0 FOR CONNECTION DETAILS

Drg.No.Z44828-479Y
Sh.1 Iss.4

AD1: Log. amp.



AD1 : Log. amp.

Fig. 29
Chap. 7
Page 67/68

PART OF
AD1
44828-479Y

0/25·6dB ATTENUATOR

25·6dB AMPLIFIER

12·8dB ATTENUATOR

+15Vd
R112 6k2
C30 100n
R103 100R
TR21 BC209C
R111 4k7
R104 6k2
-15Vd
T3
R116 54R2
R115 10R
R114 4R7
R113 1k0
FINE ADJ
C32 12p
R122 100R
TR24 2N3906
IC8(b) SD5002
IC8(a)
R117 4k7
R118 4k7
R217 470R
IC8(d) SD5002
R120 18k
D18 BZX79C 6V2
R119 18k
D17 6V2
BZX79C
10
TP8
+15V
R124 3k6
C33 100µ
R123 150R
R125 2k4
TR26 BC209C
R126 3k0
D32 BAT42
TR25 2N3904
R127 2k0
C34 1µ0
R128 1k2
TP10
13
R131 51R
R132 820R
R133 11k
C37 1n0
R134 4k3
TR27 BC209C
C39 10n
C35 3µ3
R129 10R
-15V
R135 10R
C36 3µ3
R136 3k3
D23 1N4148
C72 100n
D20 1N4148
R137 750R
R140 100R
TR28 BC209C
R130 4k7
R141 6k2
+5V
-5V
R139 62k
C38 100n
R218 470R
14
TP11
T4
R156 294R
R155 20R
R154 22R
R153 1k0
FINE ADJ
C42 12p
IC11(b) SD5002
IC11(a)
R158 4k7
R157 4k7
IC11(d) SD5002
R160 18k
IC11(c)
R159 18k
D21 6V2
B...

FROM SHEET TWO

LEVEL DETECTOR

GATED SCHMITT

+15V
R106 560k
R108 470R
R105 10R
TR22 BC308B
TP9
C31 1n0
11
D16 1N4148
R102 1k5
-5V
R109 22k
+5V
IC9 LM311
R110 1k6
IC10(a) HCT74
S
D
CLK
R
Q
RESET 1-3
CLOCK 1-3

LEVEL DETECTOR

GATED SCHMITT

+15V
R143 560k
R148 470R
R142 10R
TR29 BC308B
TP12
12
C41 1n0
C74 100n
R147 10R
C75 100n
-5V
R149 22k
+5V
IC12 LM311
R150 1k6
IC10(b) HCT74
LOG / LIN 1,3
LOG / LIN 5

+5V
R144 1k0
TR30 MPSL08
R145 2k7
R146 1k5

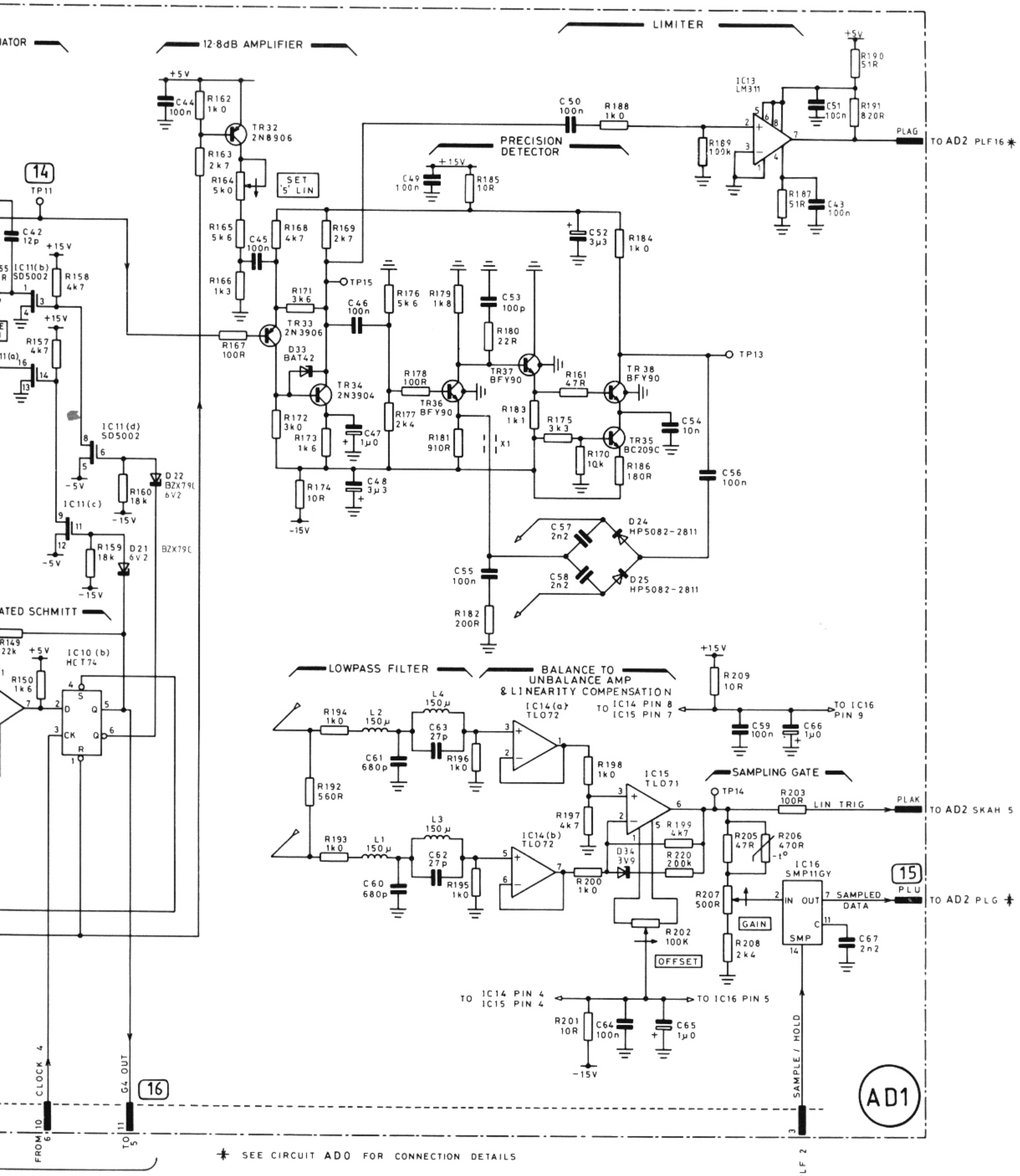
G3 OUT
RESET 4
CLOCK 4
G4 OUT
16

PLV 6 TO 13
9 FROM
10 FROM 6
11 TO 5

AD2 PLF

Drg.No. Z44828-479Y
Sh.2 Iss.3

AD1 : Log. amp.

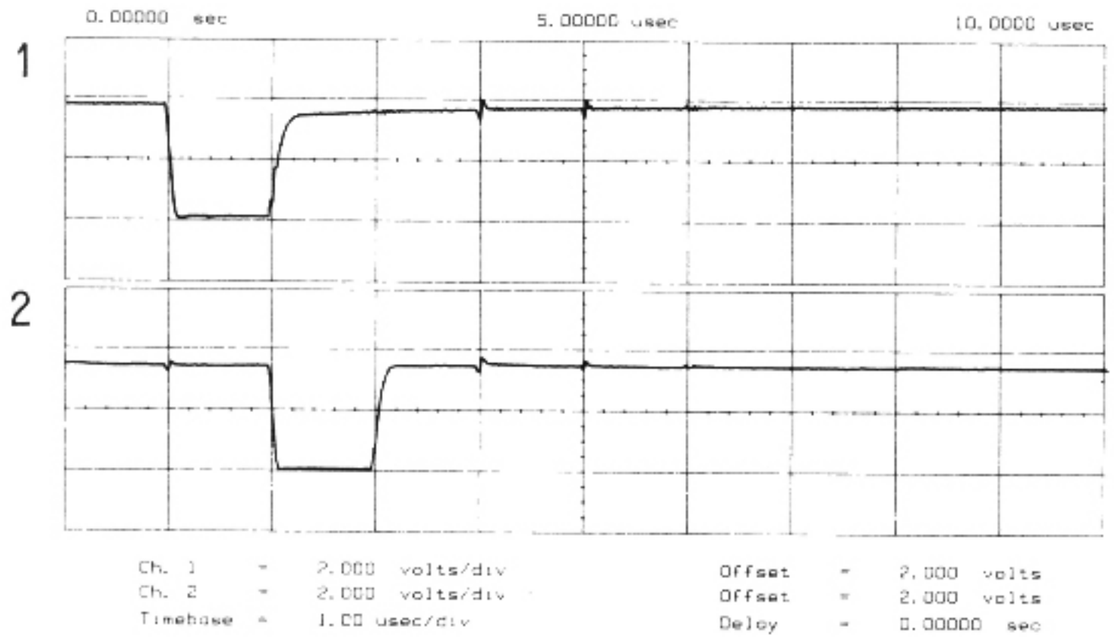

IATOR
12-8dB AMPLIFIER
LIMITER
PRECISION DETECTOR
+5V
C44 100n
R162 1k0
TR32 2N8906
R163 2k7
R164 5k0
SET '5' LIN
R165 5k6
C45 100n
R168 4k7
R169 2k7
R166 1k3
R167 100R
TP15
R171 3k6
C46 100n
TR33 2N3906
D33 BAT42
TR34 2N3904
R172 3k0
R173 1k6
C47 1µ0
R174 10R
C48 3µ3
-15V
C50 100n
R188 1k0
+15V
C49 100n
R185 10R
C52 3µ3
R184 1k0
R176 5k6
R177 2k4
R178 100R
TR36 BFY90
R179 1k8
C53 100p
R180 22R
TR37 BFY90
R181 910R
X1
R183 1k1
R175 3k3
R170 10k
R186 180R
TR38 BFY90
R161 47R
TR35 BC209C
C54 10n
C56 100n
TP13
IC13 LM311
R190 51R
C51 100n
R191 820R
R189 100k
R187 51R
C43 100n
PLAG
TO AD2 PLF16 *
14
TP11
C42 12p
+15V
IC11(b) SD5002
R158 4k7
R157 4k7
IC11(a)
IC11(d) SD5002
IC11(c)
R160 18k
D22 BZX79C 6V2
R159 18k
D21 6V2
BZX79C
-5V
-15V
C57 2n2
C58 2n2
D24 HP5082-2811
D25 HP5082-2811
C55 100n
R182 200R
ATED SCHMITT
R149 22k
IC10 (b) HCT74
R150 1k6
LOWPASS FILTER
BALANCE TO UNBALANCE AMP & LINEARITY COMPENSATION
SAMPLING GATE
L4 150µ
L2 150µ
C63 27p
R194 1k0
C61 680p
R196 1k0
IC14(a) TL072
TO IC14 PIN 8 IC15 PIN 7
R209 10R
C59 100n
C66 1µ0
TO IC16 PIN 9
R198 1k0
IC15 TL071
R192 560R
R197 4k7
L3 150µ
L1 150µ
C62 27p
R193 1k0
C60 680p
R195 1k0
IC14(b) TL072
R200 1k0
D34 3V9
R199 4k7
R220 200k
R202 100K
OFFSET
TP14
R203 100R
LIN TRIG
PLAK
TO AD2 SKAH 5
R205 47R
R206 470R -t°
IC16 SMP11GY
R207 500R
GAIN
R208 2k4
SAMPLED DATA
PLU
TO AD2 PLG *
C67 2n2
TO IC14 PIN 4 IC15 PIN 4
TO IC16 PIN 5
R201 10R
C64 100n
C65 1µ0
-15V
SAMPLE / HOLD
AD1
FROM AD2 PLF 2
CLOCK 4
G4 OUT
16
FROM 10 6
TO 11 5
* SEE CIRCUIT AD0 FOR CONNECTION DETAILS

1: Log. amp.

1
2

BOARD : AD2 *Fig. 31 refers.*

TEST POINT : IC9 pin 1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC9 pin 2 for Ch. 2

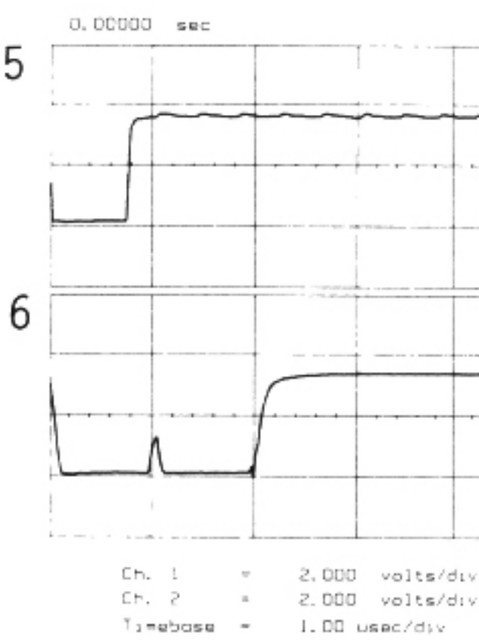
PROCEDURE :

1 Press PRESET.

5
6

BOARD : AD2

TEST POINT : TP3 (IC55a pin 11) fo
SCOPE SETTING [DEFAULT]



TEST POINT : IC56a pin 8 for Ch. 2

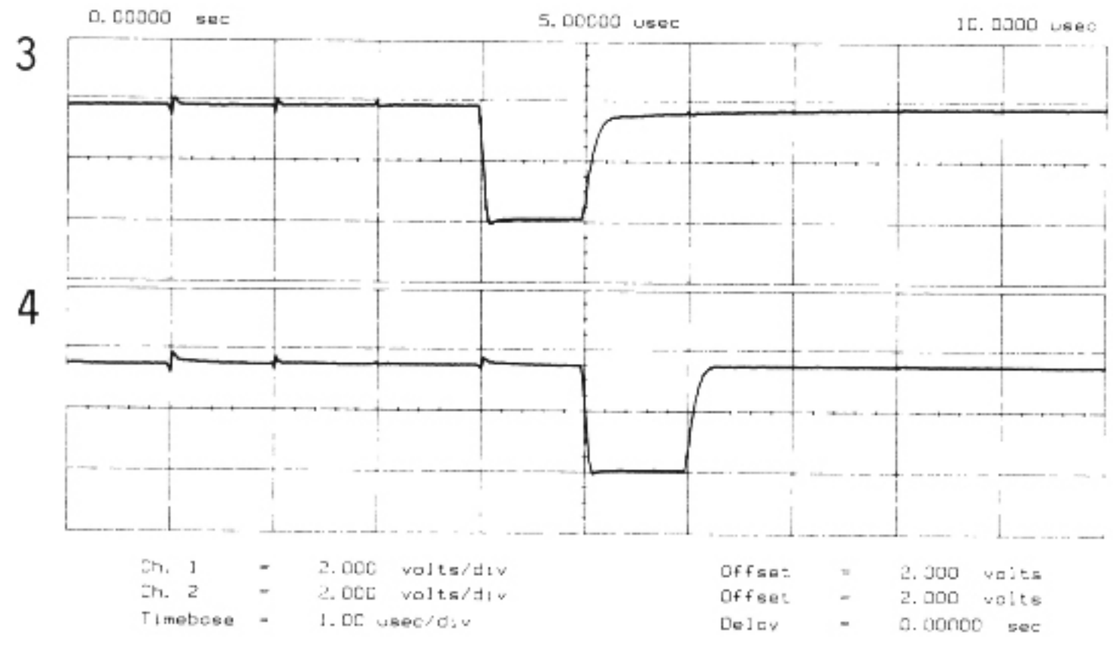
PROCEDURE :

1. Press PRESET.

3
4

BOARD : AD2

TEST POINT : IC9 pin 4 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC9 pin 5 for Ch. 2

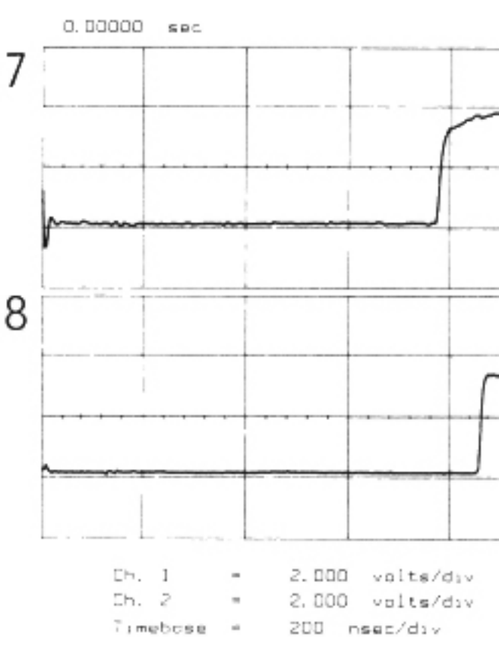
PROCEDURE :

1. Press PRESET.

7
8

BOARD : AD2

TEST POINT : TP3 (IC55a pin 11) fo
SCOPE SETTING [DEFAULT]



TEST POINT : IC13b pin 9 for Ch. 2

PROCEDURE :

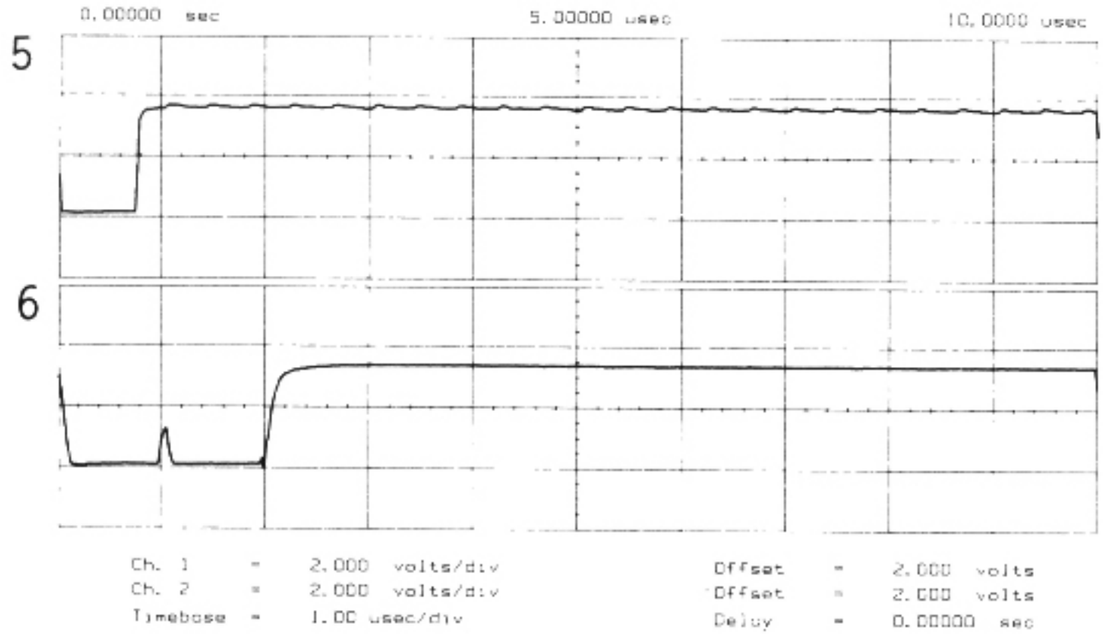
1. Press PRESET.

Fig. 31a
Chap. 7
Page 70

5
6

BOARD : AD2

TEST POINT : TP3 (IC55a pin 11) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC56a pin 8 for Ch. 2

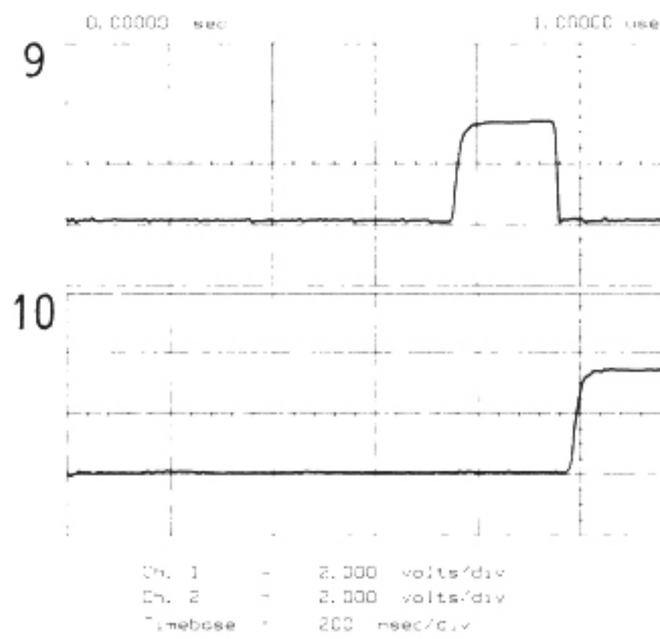
PROCEDURE :

1. Press PRESET.

9
10

BOARD : AD2

TEST POINT : IC13a pin 3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC55a pin 13 for Ch. 2

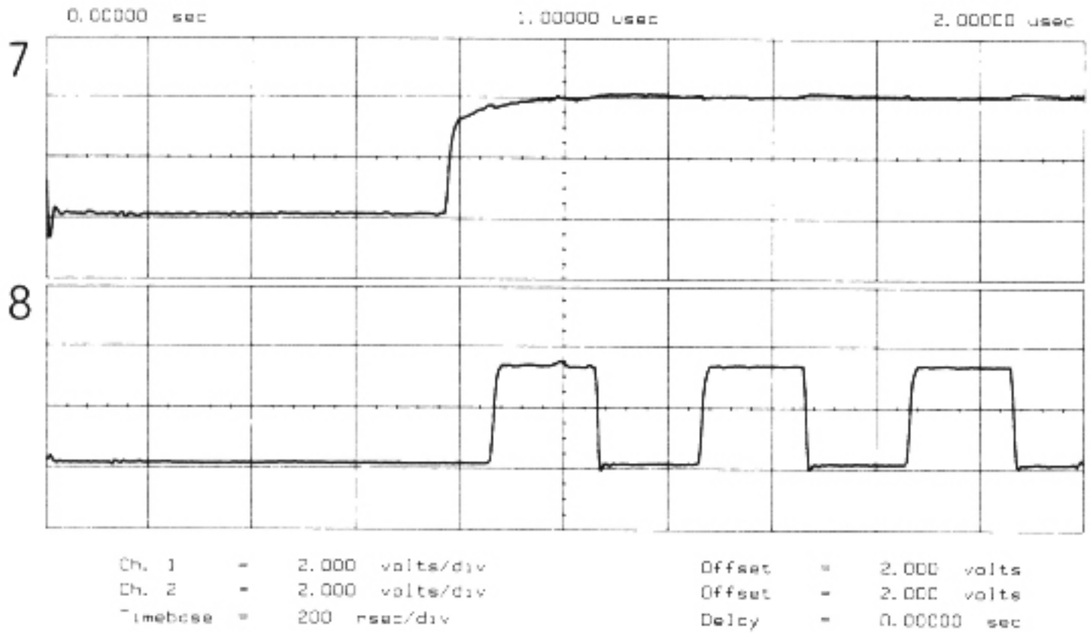
PROCEDURE :

1. Press PRESET.

7
8

BOARD : AD2

TEST POINT : TP3 (IC55a pin 11) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC13b pin 9 for Ch. 2

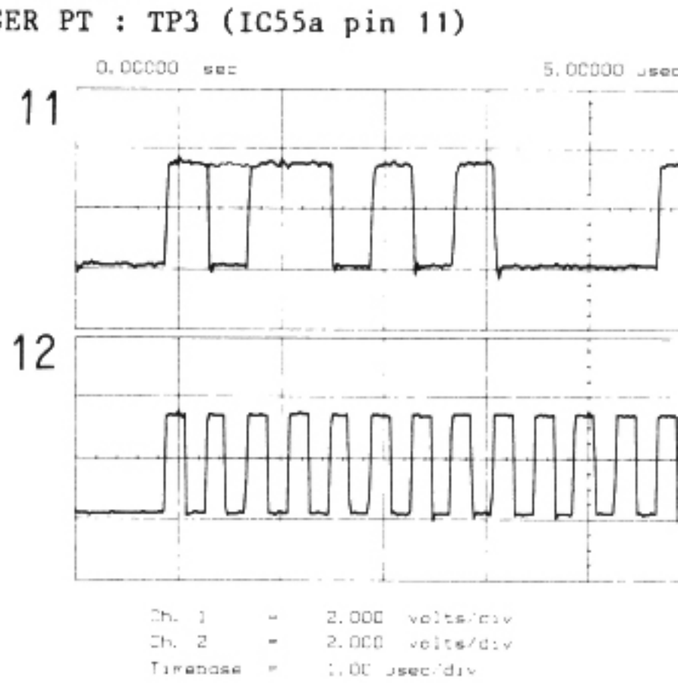
PROCEDURE :

1. Press PRESET.

11
12

BOARD : AD2

TEST POINT : IC20 pin 13 for Ch. 1 typical
SCOPE SETTING
TRIGGER PT : TP3 (IC55a pin 11)

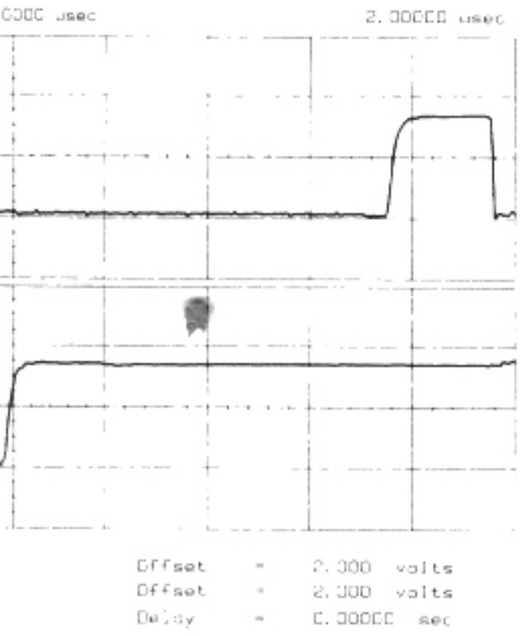


TEST POINT : IC13b pin 9 for Ch. 2

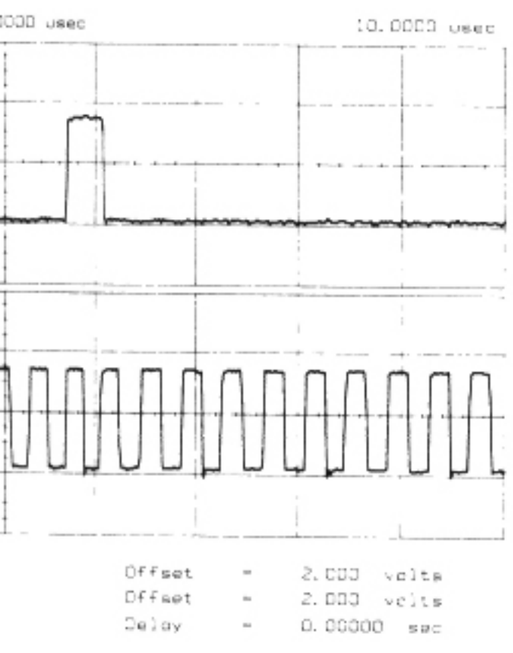
PROCEDURE :

1. Press PRESET then select the following

Span	1 kHz/DIV
Ref. freq.	10 MHz
Ref. level	-10 dBm
Mode	meter
Input	10 MHz stand



pical waveform



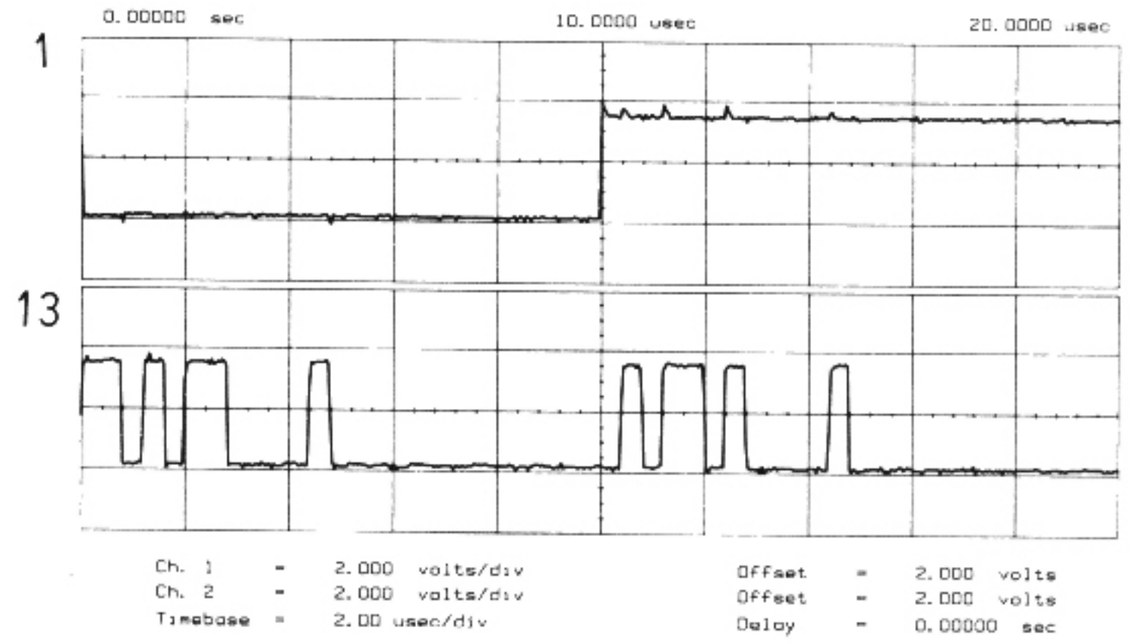
lowing 2382 settings:

DIV

standard cal. signal

1 * BOARD : AD2
13

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2, typical data

PROCEDURE :

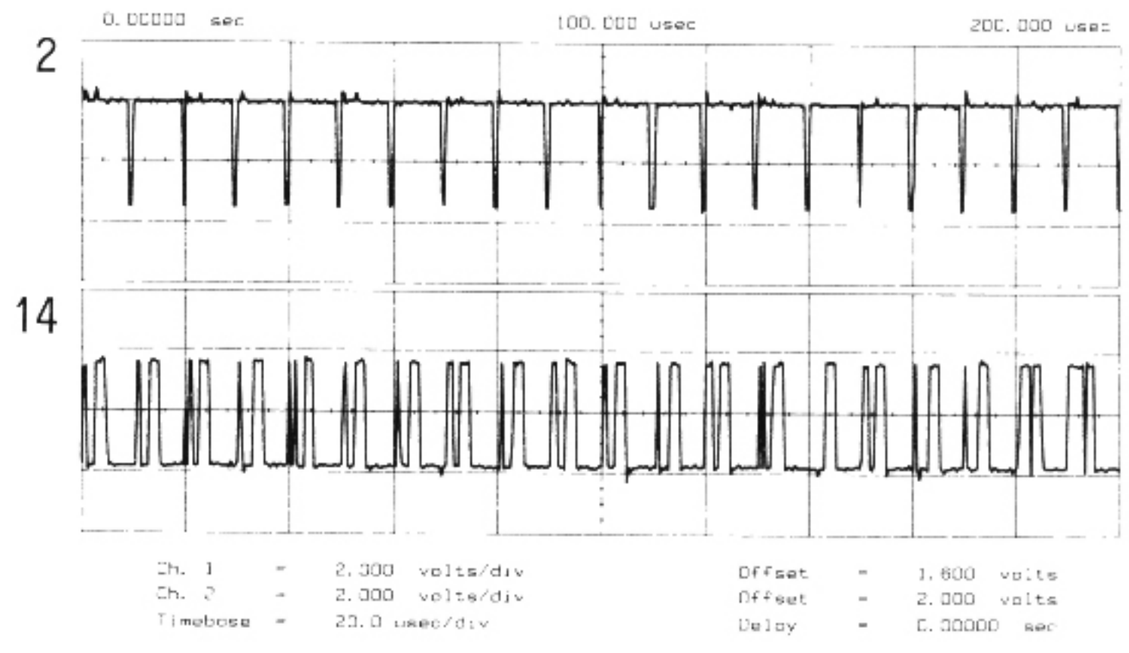
1. Press PRESET then select the following 2382 settings:

   Zero span
   Sweep time 50 µs/DIV

**cct. drg. Fig. 34 refers*

2 * BOARD : AD2
14

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2

PROCEDURE :

1. Press PRESET.

**cct. drg. Fig. 34 refers*

Fig. 31a

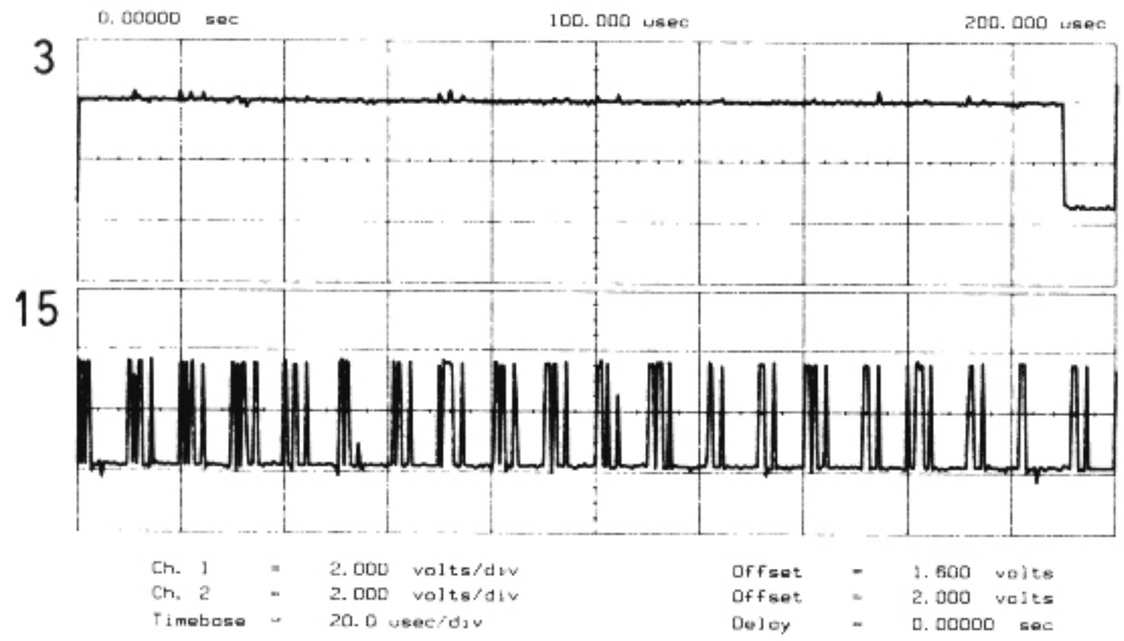
May 86

3 * BOARD : AD2

15

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1

SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 setting:

   Zero span

**cct. drg. Fig. 34 refers*

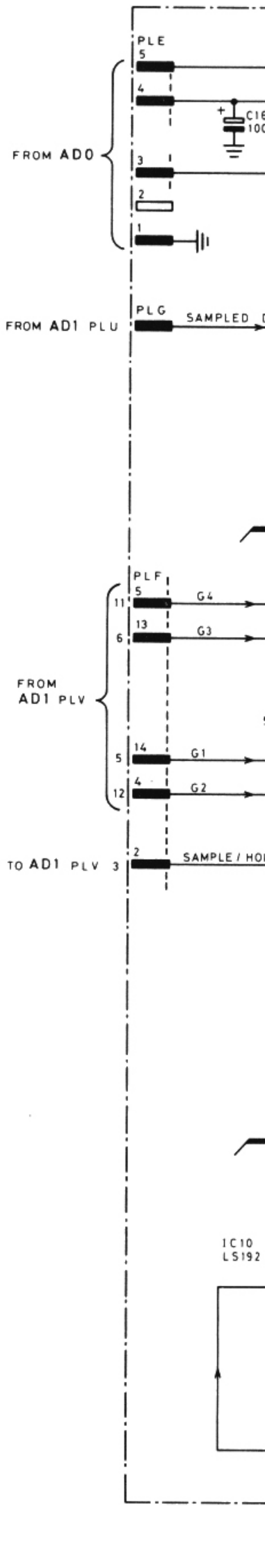


Fig. 31 Waveforms for AD2

May 86

Drg
Sh.

20dB RANG
LIN LOOK

12 BIT A-D CONVERTER

FROM AD0 PLE

5 +15V
4 +5V
C16 100µ
3 -15V
2
1

FROM AD1 PLU

PLG SAMPLED DATA

+15V
C11 10µ
C10 100n
+5V
C14 100n
C15 10µ
31 +15V
16 +5V
24 REF OUT
C9 10µ
25 REF IN
26 OFFSET
27 INPUT
21 CONVERSION START
ANA GND
-15V
CLK OUT
CLK IN
DIG GND
30 32 18 19 15
C12 10µ
C13 100n
-15V
BIT 12
BIT 11
BIT 10
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
IC12 AD578
A0
A11
A10
11
LOG / LIN
SAMPLE / HOLD
CS
18

LATCH 5V OVERLOAD

IC55(d) LS32
IC8(a) LS74
S
D
CLK
Q
R

BINARY CONVERSION

FROM AD1 PLV

PLF
5 G4
13 G3
14 G1
4 G2
IC16 LS00
(a) (b) (c) (d)

TO AD1 PLV 3

SAMPLE / HOLD

IC51(a) LS04

SERIAL DATA OUTPUT CLOCK PHASING

IC56(a) LS08

5MHz

C62 120p

LOG AMP MEASUREMENT CYCLE SEQUENCE GENERATOR

SEQUENCE START
SEQUENCE END

IC13(b) LS74
IC13(a) LS74
IC55(a) LS32
DATA SYNC
TP3
TO IC

1MHz

÷2 ÷5 ÷2 ÷5

IC9 LS42
IC10 LS192
IC11 LS192
CLR
CY
+5V

IC51(b) LS04

TO SHEET 4 IC46 PIN 11
C61 120p
C63 120p
SEQUENCE END

ENABLE DATA CONVERSION (L) FROM SHEET 4 IC56 PIN 3

GATED 10MHz FROM SHEET 3 IC53 PIN 6

FROM SHEET 2
LOG / LIN
I P IDENT

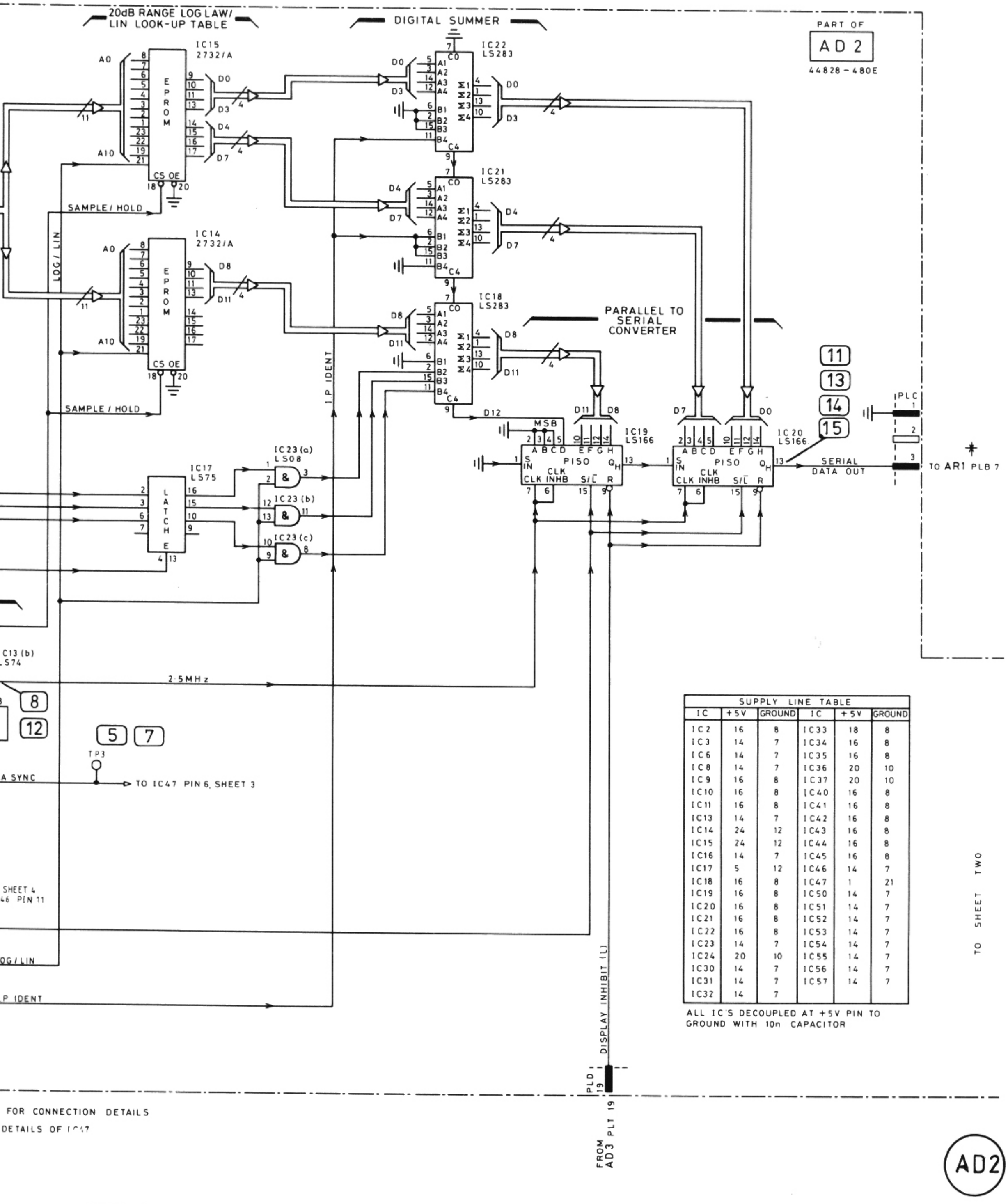
PLF
CLK 4
RESET 4
CLK 1-3
RESET 1-3

TO AD1 PLV

SEE CIRCUIT AD0 FOR CONNECTION DETAILS
SEE SHEET 3 FOR DETAILS OF IC47

Drg. No. Z44828-480E
Sh. 1 Iss. 3

AD2 : Lo



SUPPLY LINE TABLE					
IC	+5V	GROUND	IC	+5V	GROUND
IC2	16	8	IC33	18	8
IC3	14	7	IC34	16	8
IC6	14	7	IC35	16	8
IC8	14	7	IC36	20	10
IC9	16	8	IC37	20	10
IC10	16	8	IC40	16	8
IC11	16	8	IC41	16	8
IC13	14	7	IC42	16	8
IC14	24	12	IC43	16	8
IC15	24	12	IC44	16	8
IC16	14	7	IC45	16	8
IC17	5	12	IC46	14	7
IC18	16	8	IC47	1	21
IC19	16	8	IC50	14	7
IC20	16	8	IC51	14	7
IC21	16	8	IC52	14	7
IC22	16	8	IC53	14	7
IC23	14	7	IC54	14	7
IC24	20	10	IC55	14	7
IC30	14	7	IC56	14	7
IC31	14	7	IC57	14	7
IC32	14	7			

ALL IC'S DECOUPLED AT +5V PIN TO GROUND WITH 10n CAPACITOR

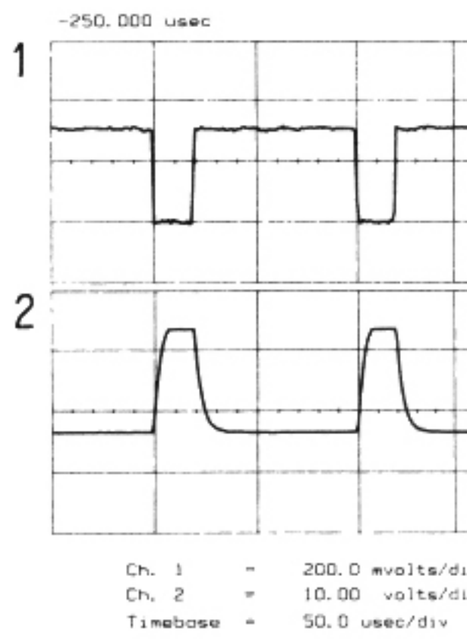
AD2

AD2: Log. amp. interface

1 BOARD : AD2 *Fig. 32 refers*

2

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC4 pin 1 for Ch. 2

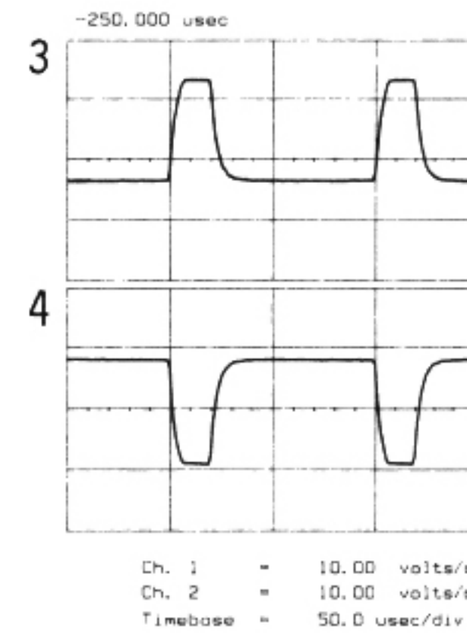
PROCEDURE :

1. Press PRESET and set trigger
2. Connect an external pulse ge
3. Set pulse generator to p.r.f
   mark:
   switc

3 BOARD : AD2

4

TEST POINT : IC4 pin 1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC4 pin 7 for Ch. 2

PROCEDURE :

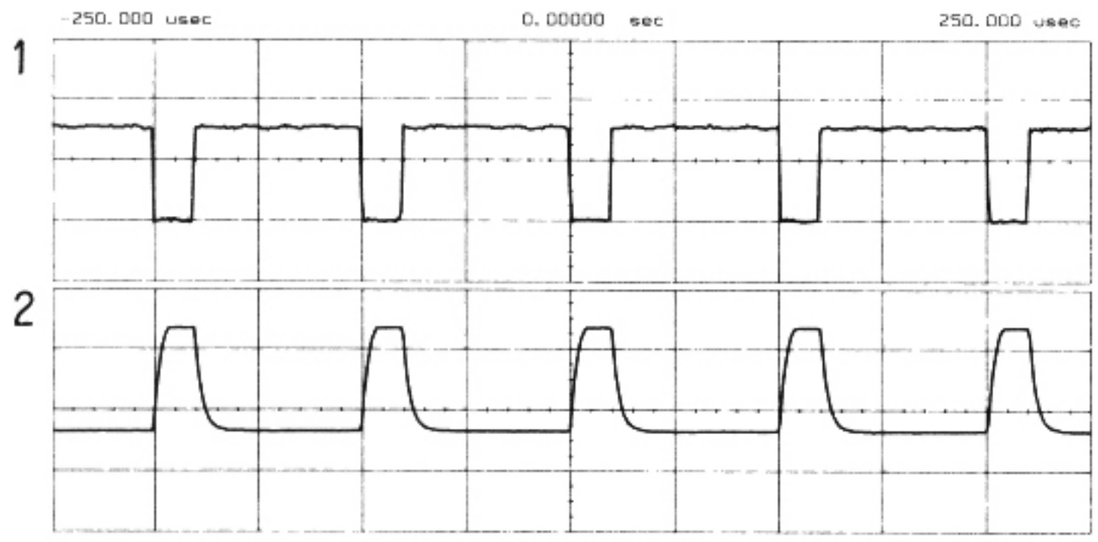
1. Press PRESET and set trigger
2. Connect an external pulse ge
3. Set pulse generator to p.r.f
   mark:
   switc

Fig. 32a
Chap. 7
Page 72

1
2

BOARD : AD2 *Fig. 32 refers*

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC4 pin 1 for Ch. 2

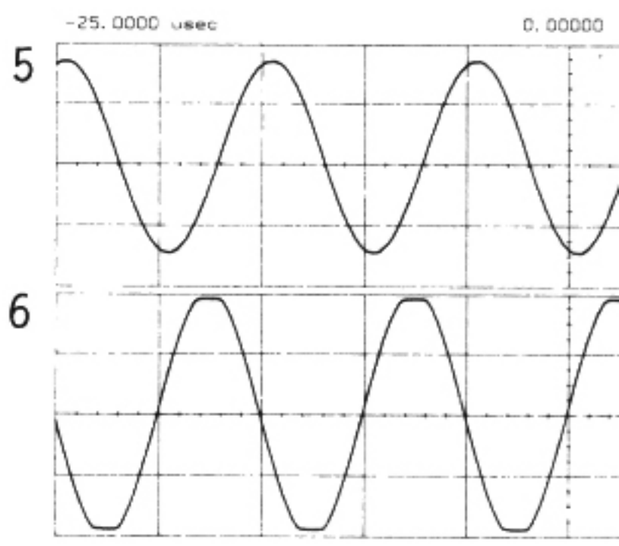
PROCEDURE :

1. Press PRESET and set trigger source to EXT.
2. Connect an external pulse generator to EXT TRIG socket on the 2382.
3. Set pulse generator to p.r.f. 10 kHz
   mark:space = 4:1
   switching levels 0 and 300 mV

5
6

BOARD : AD2

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC4 pin 1 for Ch. 2

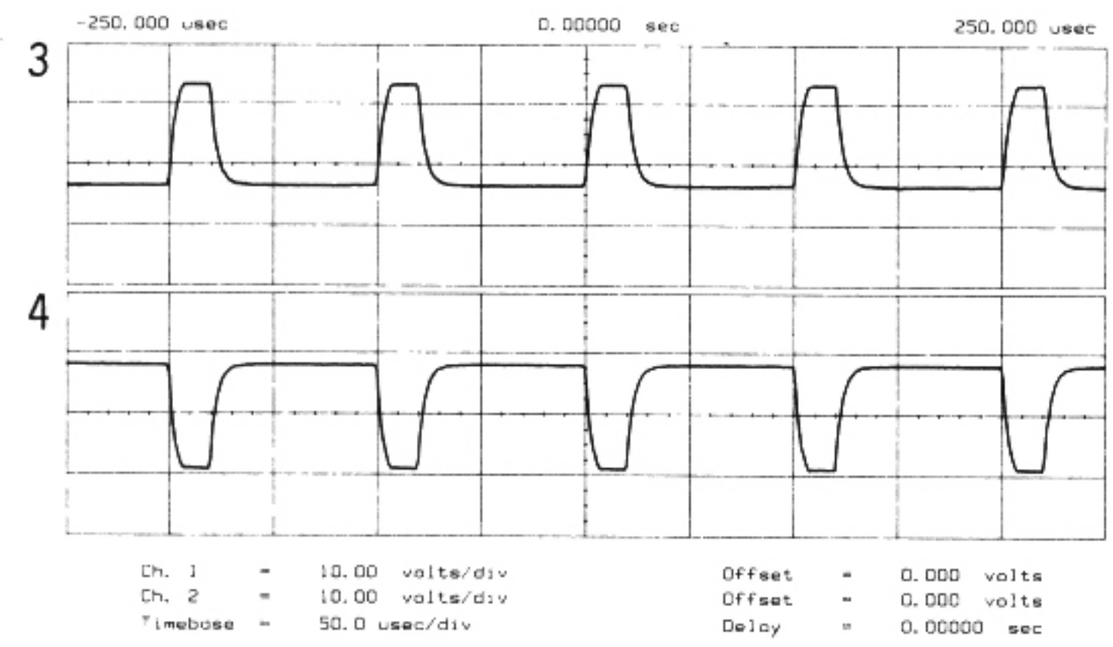
PROCEDURE :

1. Press PRESET and set 'trigger source'
2. Connect an external pulse generator
   a 50 Ω through load in line.
3. Set pulse generator to p.r.f. 100 kH

3
4

BOARD : AD2

TEST POINT : IC4 pin 1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC4 pin 7 for Ch. 2

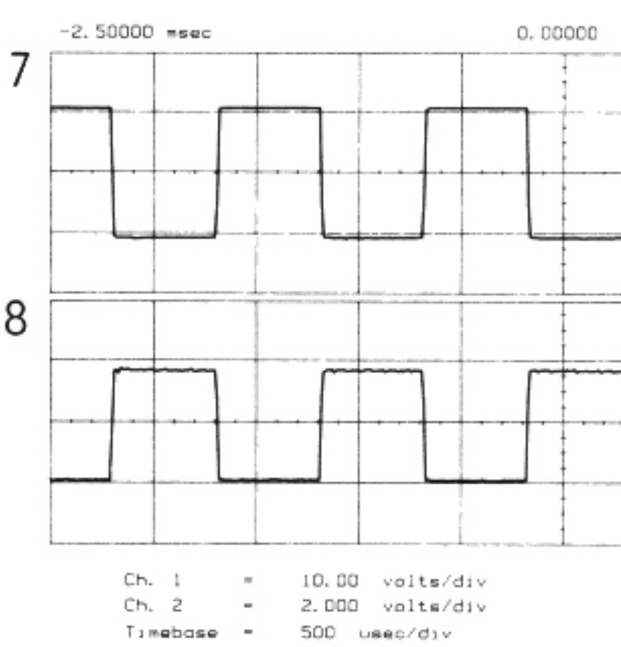
PROCEDURE :

1. Press PRESET and set trigger source to EXT.
2. Connect an external pulse generator to EXT TRIG socket.
3. Set pulse generator to p.r.f. 10 kHz
   mark:space = 4:1
   switching levels 0 and 300 mV

7
8

BOARD : AD2

TEST POINT : IC5 pin 6 for Ch. 1
SCOPE SETTING
TRIGGER PT : signal generator output

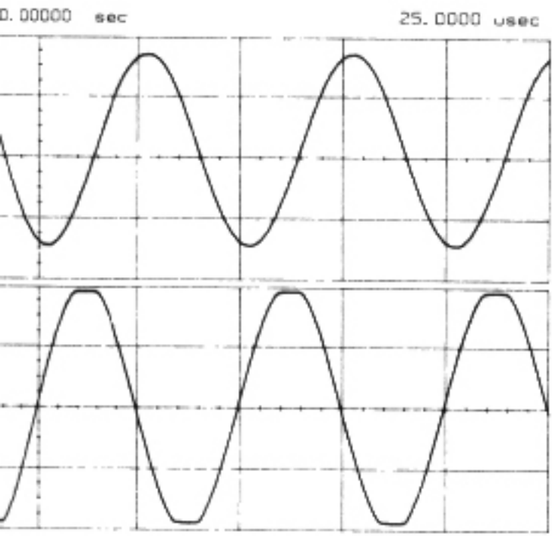


TEST POINT : TR2 collector for Ch. 2

PROCEDURE :

1. Press PRESET then select the followin
   Span 1 kHz/DIV,
   1 ms/DIV in
2. Connect signal generator audio output
3. Set signal generator to 200 MHz at 0
   at 1 kHz.

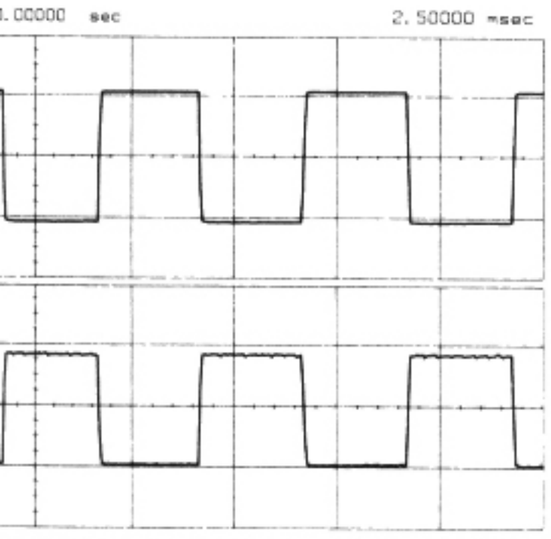
Waveforms for AD2



ource' to EXT.

ator to EXT TRIG socket on the 2382 with

00 kHz at 0 dBm.



llowing 2382 settings:

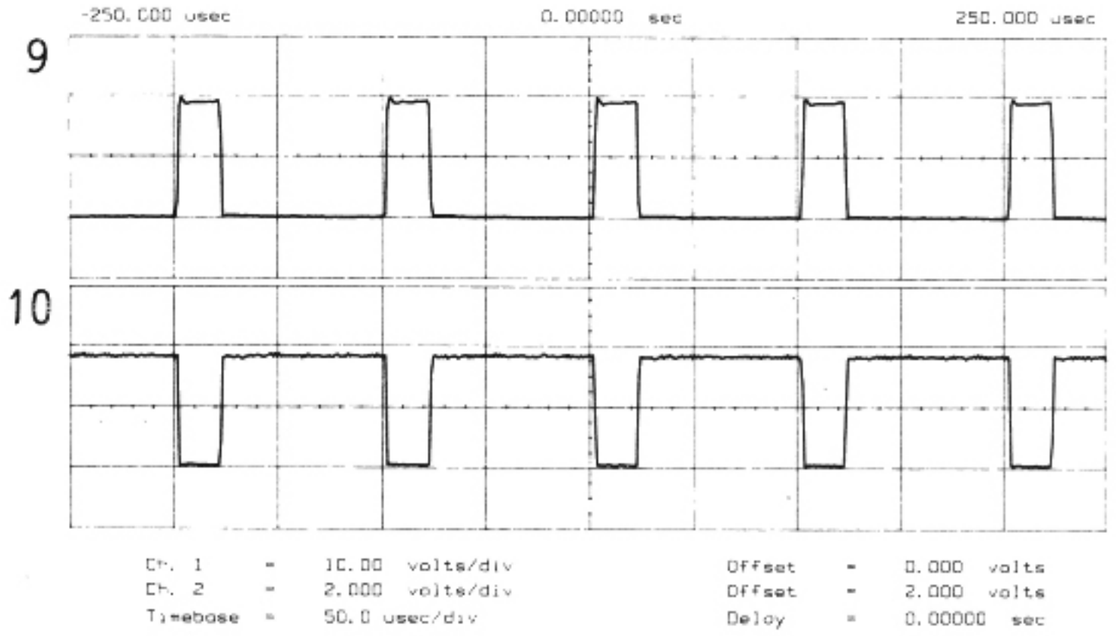
/DIV, 100 mV/DIV, zero span then
DIV in sequence.

output to 2382 INPUT.

at 0 dBm, 50% amplitude modulated

9
10 BOARD : AD2

TEST POINT : IC5 pin 6 for Ch. 1
SCOPE SETTING



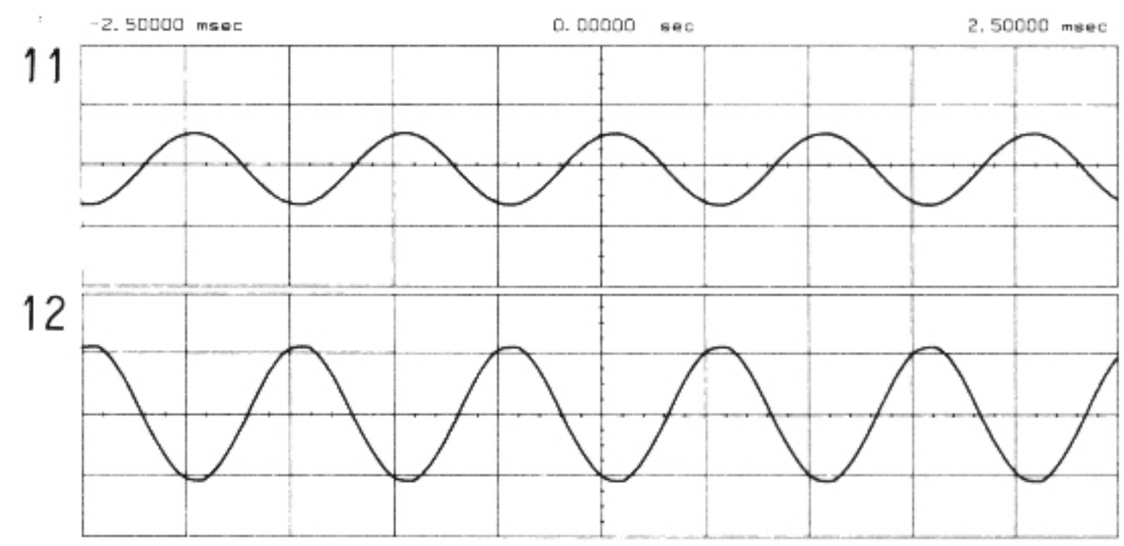
TEST POINT : TR2 collector for Ch. 2

PROCEDURE :

1. Press PRESET and set 'trigger source' to EXT.
2. Connect an external pulse generator to EXT TRIG socket on the 2382.
3. Set pulse generator to p.r.f. 10 kHz
   mark:space = 4:1
   switching levels 0 and 300 mV

11
12 BOARD : AD2

TEST POINT : PLAH 5 for Ch. 1
SCOPE SETTING
TRIGGER PT : signal generator audio output



TEST POINT : IC4 for Ch. 2

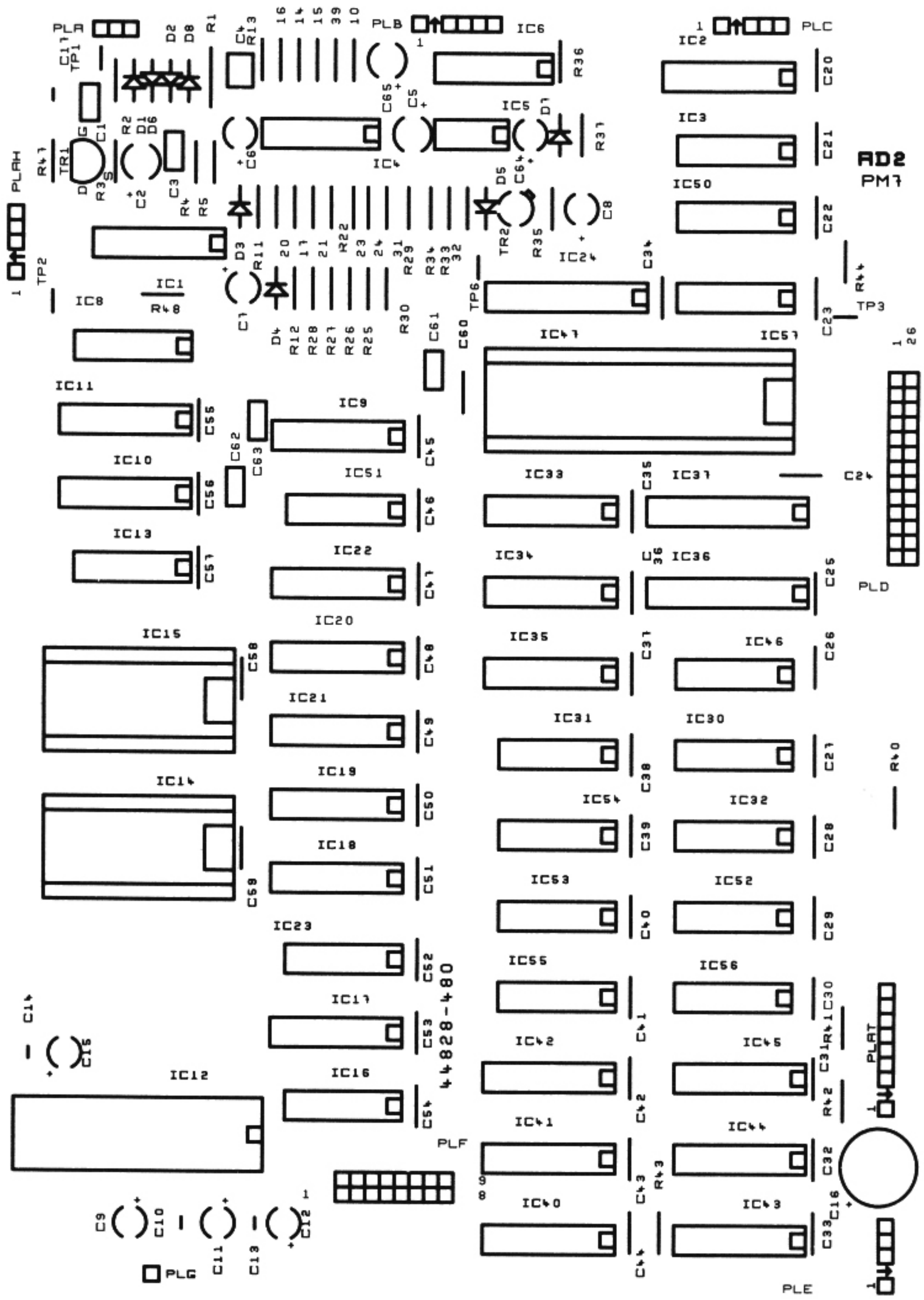
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Span 1 kHz/DIV, 100 mV/DIV, zero span
   Sweep time 1 ms/DIV
2. Connect signal generator audio output to input.
3. Set signal generator to 200 MHz at 0 dBm, 50% amplitude modulated at 1 kHz.

Fig. 32a

May 86



Component layout for AD2

Fig. 32

May 86

Drg.No. Z448
Sh.2 Iss.

INPUT OVERLOAD PROTECTION

5
1

PLA
1
2
3
FROM AR0
EXT TRIG
TP1
C1
1n0
R2
470k
* D1, D2, D6, D8
1N4148
D1
D2
D6
D8
+15Vd
TR1
BF245B
R1
10M
R3
7k5
-15Vd

PEAK
DETECTOR

C4
2p2
R13
120k
R14
120k

INPUT AMPLIFIER

R5
68k
+15V
R39
10R
+15Vd
C65
33µ
C6
3µ3
R17
1M0
R21
1M0
D3
1N4148
R11
47k
C3
1n5
R4
560R
IC4(a)
TL074
R10
560R
C5
33µ
-15Vd
2
3
6
12
R29
10R
-15V
R23
30k
R22
1M0
R24
120k
-15V
+15V
R26
120k
R27
1M0
R25
30k
D4
1N4148
R12
47k
R28
1M0
C7
3µ3
R30
1M0

PLAH
1
2
FROM AD1 PLAJ
3
LOG TRIG
TP2
4
FROM AD1 PLAK
5
LIN TRIG
11
PLB
TO VOLUME CONTROL BACK PANEL
5
AUDIO
SEE AR0
C17
220n
R47
10k
+5V
IC1(a)
DG211
12
3
2
14
15
16
1
5
VIDEO TRIG
10
IC51(e)
LS04
11
LOG LIN
IC1(b)
DG211
+15V
13
11
10
6
7
8
9
4
-15Vd
C2
33µ
R48
9k1

PLD
5
CS50
1
D0
26
2
25
3
24
4
23
D7
FROM AD3 PLT
8

TRIGGER MODE LATCH

IC24
LS273
11
CLK
D0
D7
8
3
4
7
8
13
14
17
18
1
2 VIDEO (L)
5 LINE (L)
6 EXT (L)
9 AUTO (L)
12 +VE (L)
15
16
19
LATCH
A

TO SHEET 3

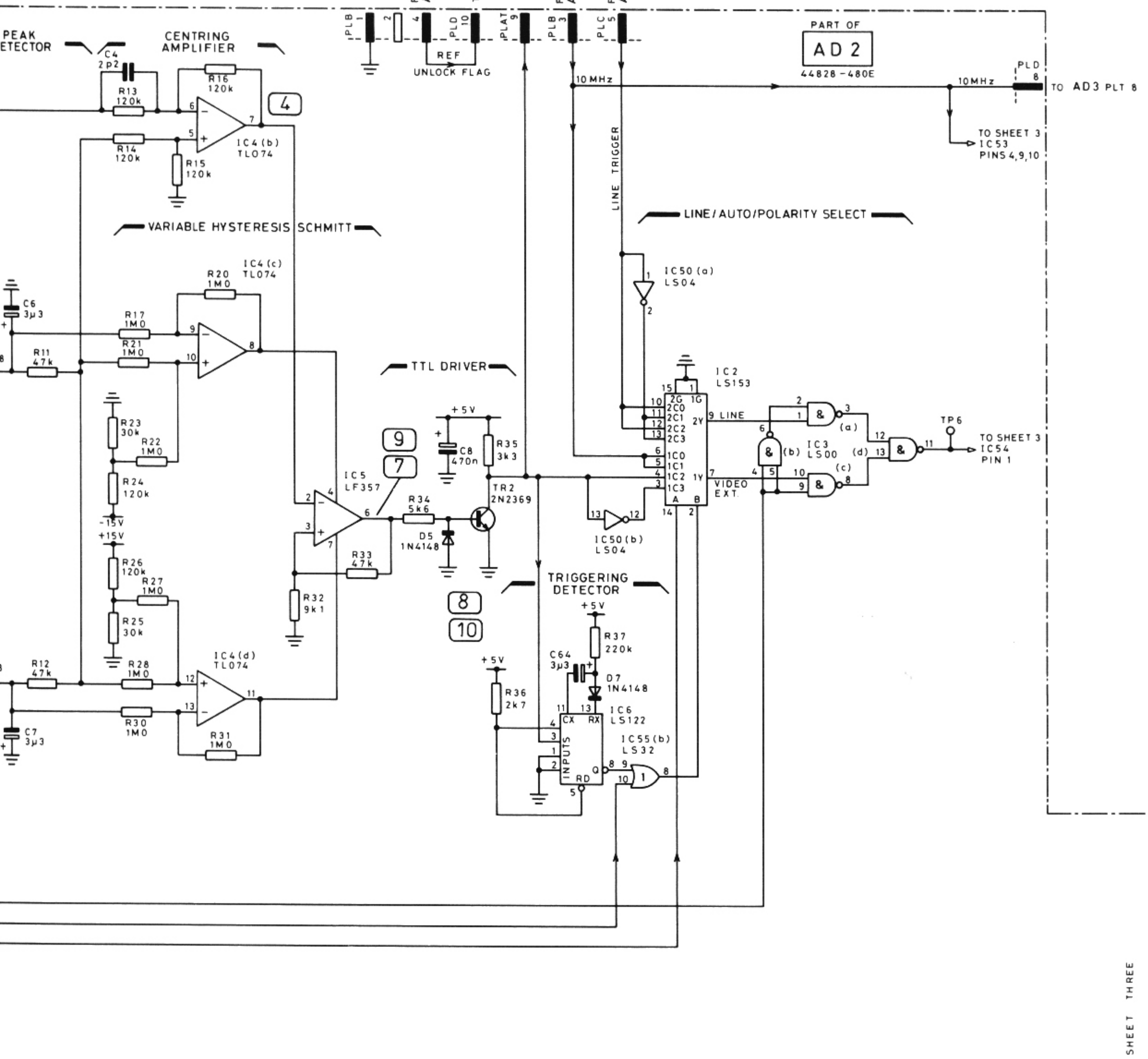
IC23(d)
LS08
5
4
&
6
LOG / LIN
TO SHEET 1
IP IDENT
5
1,2
LOG/LIN
LOG/LIN

PLF
15
3
TO AD1 PLV 14
TO AD1 PLV 4

FROM SHEET ONE

Drg.No. Z44828-480E
Sh.2 Iss.4

AD2



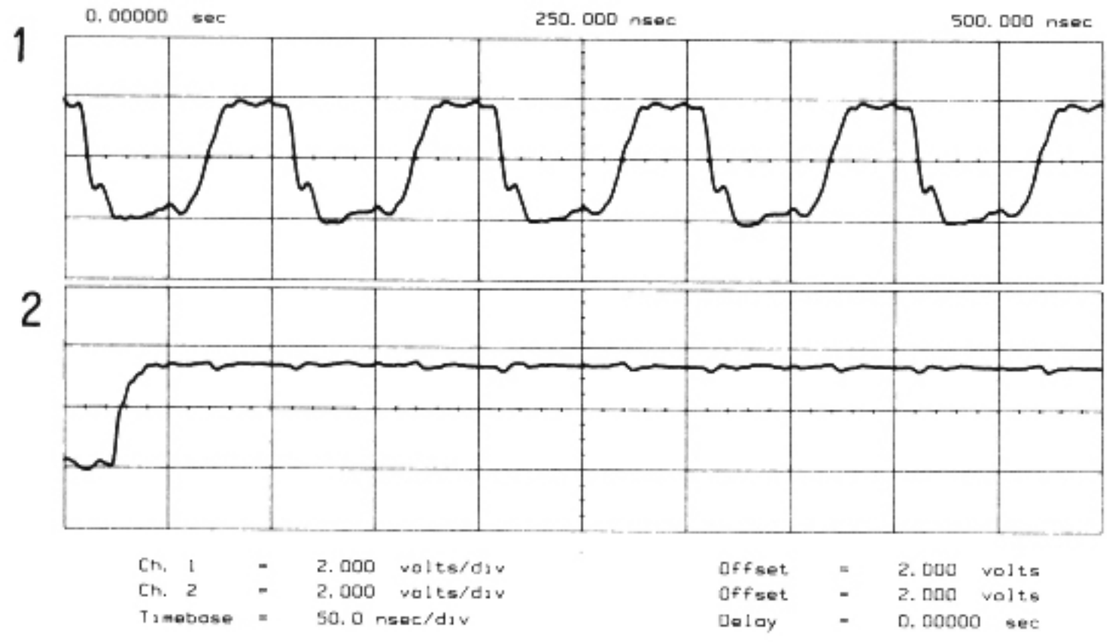
AD2: Log. amp. interface

Fig. 32
Chap. 7
Page 73

1
2

BOARD : AD2 *Fig. 33 refers*

TEST POINT : IC53a pin 9 for Ch. 1
SCOPE SETTING
TRIGGER PT : IC30a pin 5 rising edge



TEST POINT : IC30b pin 9 for Ch. 2

PROCEDURE :

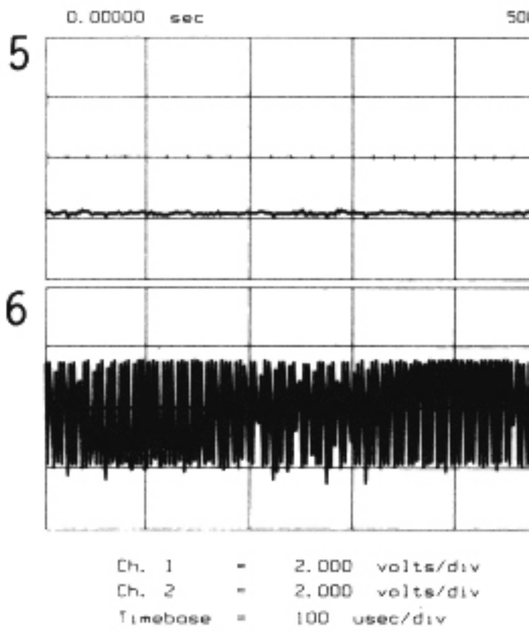
1. Press PRESET then select the following 2382 settings:

Zero span	
Sweep time	100 µs/DIV

5
6

BOARD : AD2

TEST POINT : IC32a pin 6 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC30a pin 3 for Ch. 2

PROCEDURE :

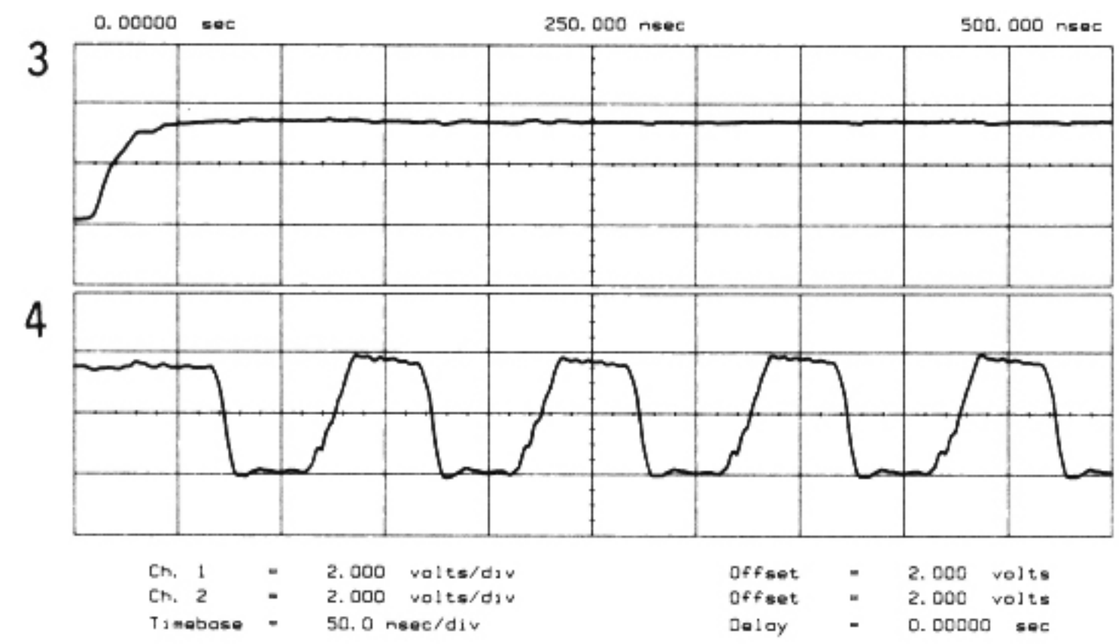
1. Press PRESET then select the fo

Zero span	
Sweep time	100 µ

3
4

BOARD : AD2

TEST POINT : IC31b pin 9 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC53b pin 6 for Ch. 2

PROCEDURE :

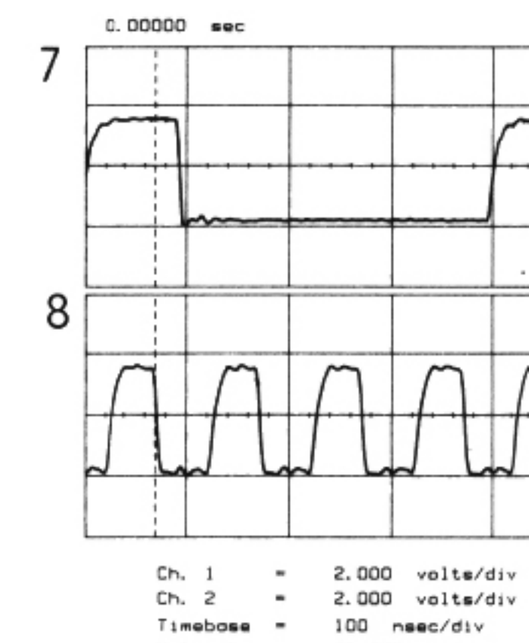
1. Press PRESET then select the following 2382 settings:

Zero span	
Sweep time	100 µs/DIV

7
8

BOARD : AD2

TEST POINT : IC35 pin 15 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC51c pin 2 for Ch. 2

PROCEDURE :

1. Press PRESET then select the fo

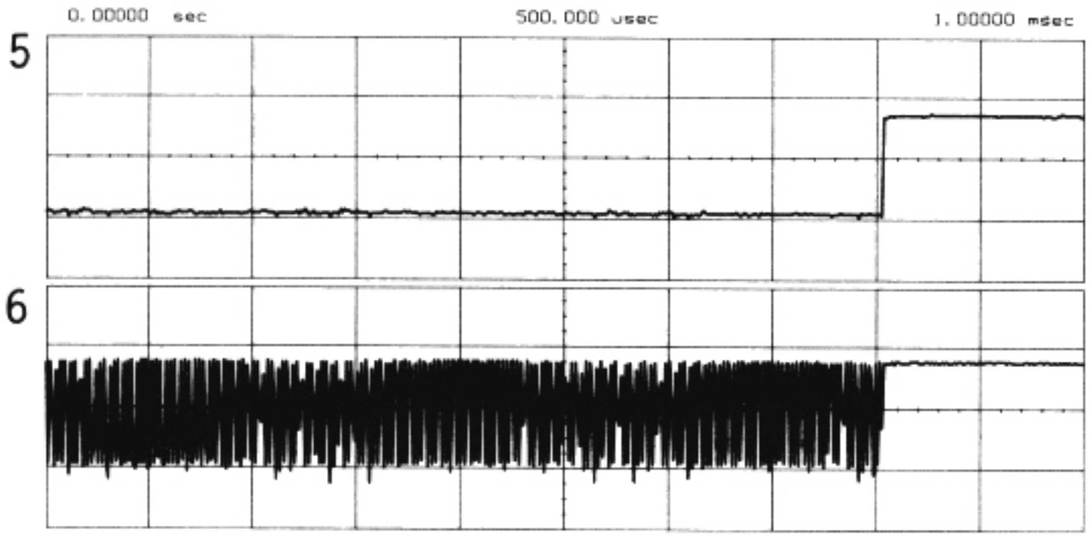
Zero span	
Sweep time	20 µs

Fig. 33a
Chap. 7
Page 74

5
6

BOARD : AD2

TEST POINT : IC32a pin 6 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC30a pin 3 for Ch. 2

PROCEDURE :

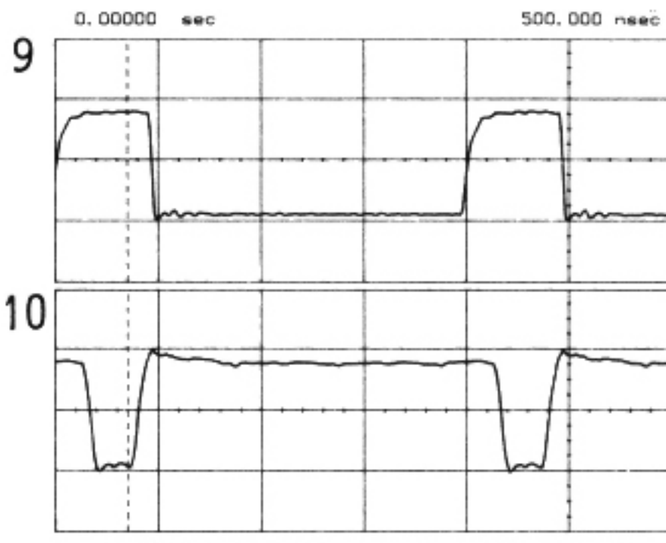
1. Press PRESET then select the following 2382 settings:

   Zero span
   Sweep time 100 µs/DIV

9
10

BOARD : AD2

TEST POINT : IC35 pin 15 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC53c pin 3 for Ch. 2

PROCEDURE :

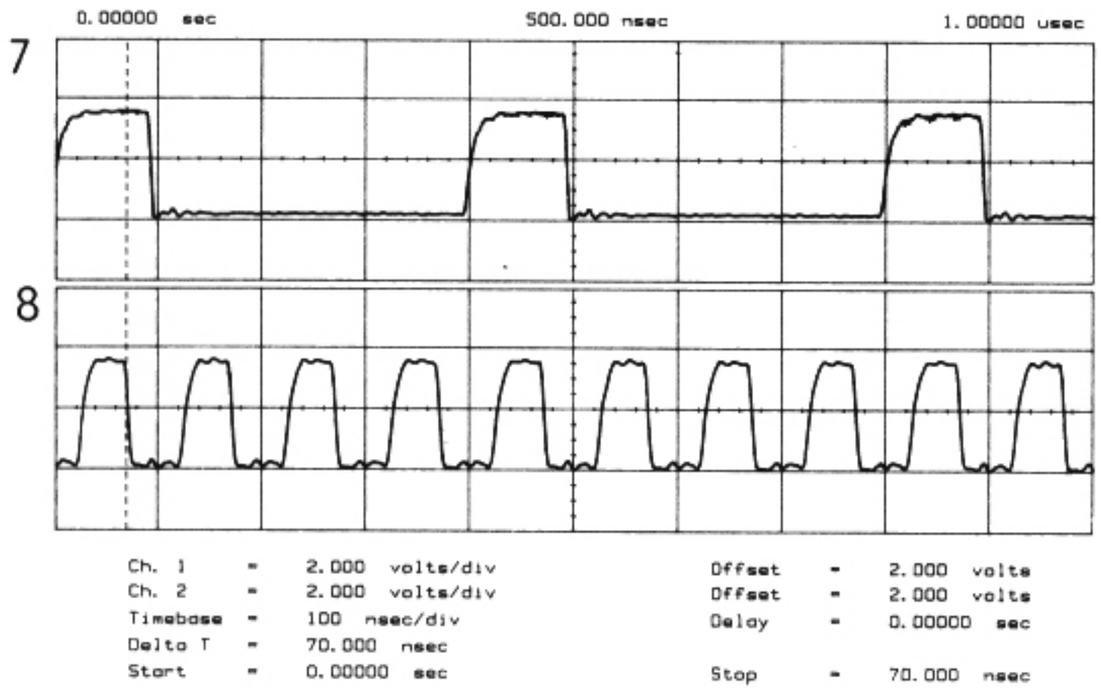
1. Press PRESET then select the following 2

   Zero span
   Sweep time 20 µs/DIV

7
8

BOARD : AD2

TEST POINT : IC35 pin 15 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC51c pin 2 for Ch. 2

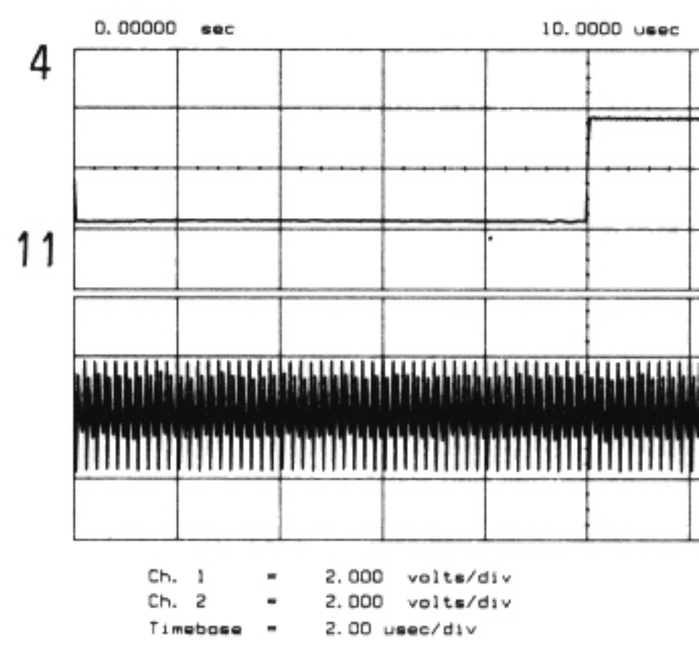
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Zero span
   Sweep time 20 µs/DIV

4 * BOARD : AD2
11

TEST POINT : IC46b pin 10 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]

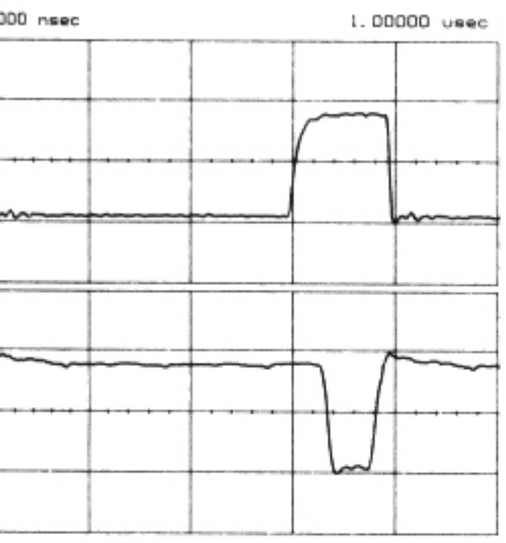


TEST POINT : IC53c pin 3 (Fig. 33) for Ch. 2

PROCEDURE :

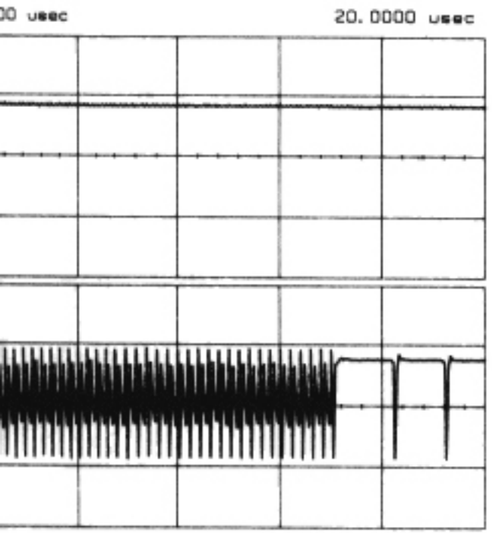
1. Press PRESET then select the following 2

   Zero span
   Sweep time 50 µs/DIV



wing 2382 settings:

Ch. 1



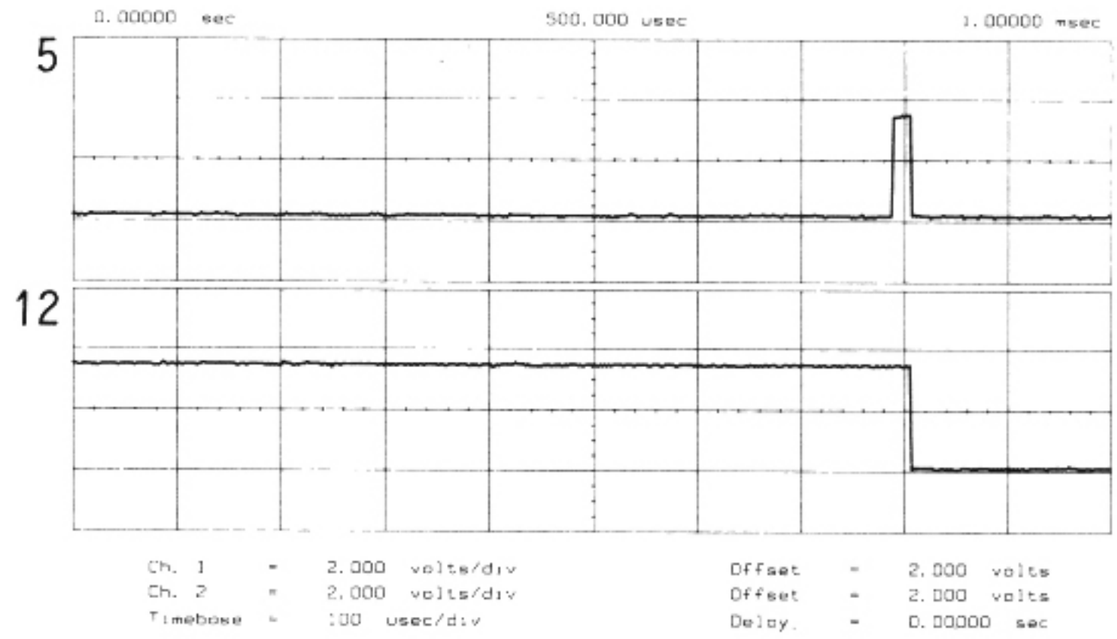
Ch. 2

wing 2382 setting:

*cct. drg. Fig. 34 refers

5 * BOARD : AD2
12

TEST POINT : IC46b pin 9 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC30a pin 5 (Fig. 33) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Zero span
   100 µs/DIV

cct. drg. Fig. 34 refers

Fig. 33a

May 86

FROM AD1 PLAG

PLF 16

IF COUNT 13

IC56(d) LS08

12 & 11

33 IN OUT ① IC47 IN OUT ②

FLYBACK MODE

FROM AD3 PLT 11

PLD 11

GATE

SWEEP MODE

FROM AD3 PLT18

18

32 IN OUT ② IC47

AUTO-TEST INVERTER

+5V

R40 910R

PLAT 1

A

FROM SHEET TWO

FROM AD3 PLT

PLD 12 7 20 15 16

12 8 20 15 16

µP DATA BUS FROM SHEET 1

RD (L) CS54(L) CS55(L) WR (L) A0

5 4

& 6

IC56 (a) LS08

+5V

D7 D0

28 27 26 25 24 23 22 20 19 18 17 16 15 14 13 12 11 10 9 8

5 X1

6 X2

33 SOURCE 1

32 SOURCE 2

31 SOURCE 3

30 SOURCE 4

29 SOURCE 5

GATE 5A GATE 4A GATE 3A GATE 2A GATE 1A

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 RD CS WR A0

F OUT 7

DETAILS OF IC47 9513 (INDIVIDUAL SECTIONS SHOWN WHERE USED)

OUT 1 3

OUT 2 2

OUT 3 40

OUT 4 38

OUT 5 37

GATE 1 GATE 2 GATE 3 GATE 4 GATE 5

1 4 39 36 35 34 21

+5V

LOG AMP ENABLE FROM IC36 PIN 15

FROM SHEET 2 10 MHz

IC53(b) LS00 4

4 5 & 6

TRIG CONTROLS

SAMPLE/REAL FROM IC36 PIN 9

REFRESH RETRACE FROM IC36 PIN 5

SWEEP ARM FROM IC36 PIN 2

FROM SHEET 2 IC3 PIN 11 TRIG

IC53(a) LS00

1

9 10 & 8

+5V

IC30(b) LS74

10 S 12 D 11 CLK 13 R 9 Q 2 Q 8

2

IC54(a) LS32

1 2 1 3

IC54(b) LS32

4 5 1 6

IC30(a) LS74

A

+5V 4 S 2 D 3 CLK 1 R 5 Q 6 Q

12

6

IC31(b) LS74

3

+5V 10 S 12 D 11 CLK 13 R 9 Q 8 Q

ENABLE DIVIDERS

IC32(a) LS74

4 S 2 D 5 CLK 1 R 6 Q

+5V

IC52(b)

5 4 & 6 3

5

IC54(c) LS32

9 10 1 8

IC52(c) LS00

2 1 & 3

IC31(a) LS74

4 S 2 D 3 CLK 1 R 5 Q 6 Q

A

DISABLE PROGRAMMABLE COUNTERS

DISABLE 10MHz CLOCK

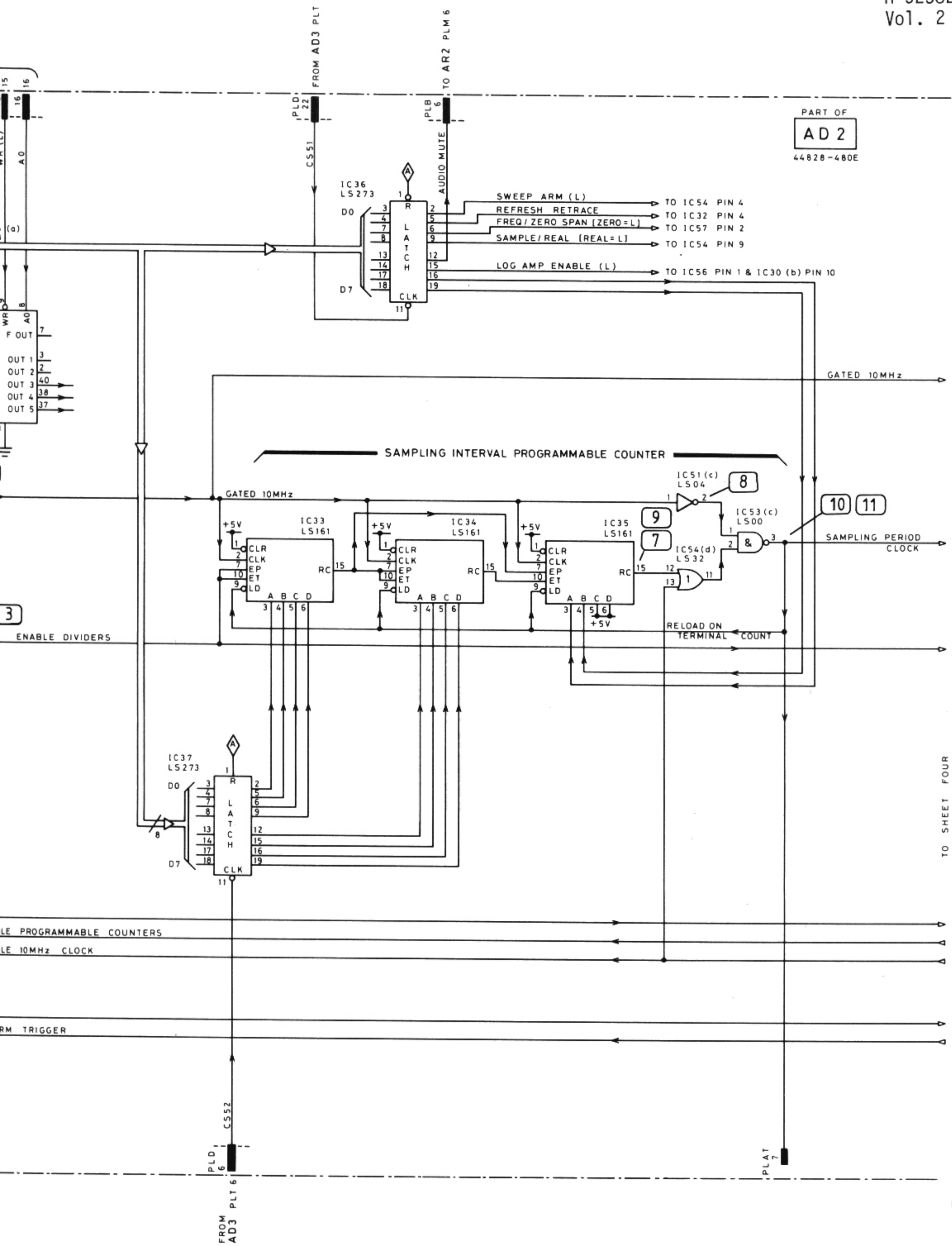
DISARM TRIGGER

PLD 17 SWEEP TRIG

FROM AD3 PLT 17

Drg.No. Z44828-480E
Sh.3 Iss.4

AD2 : Log. amp.

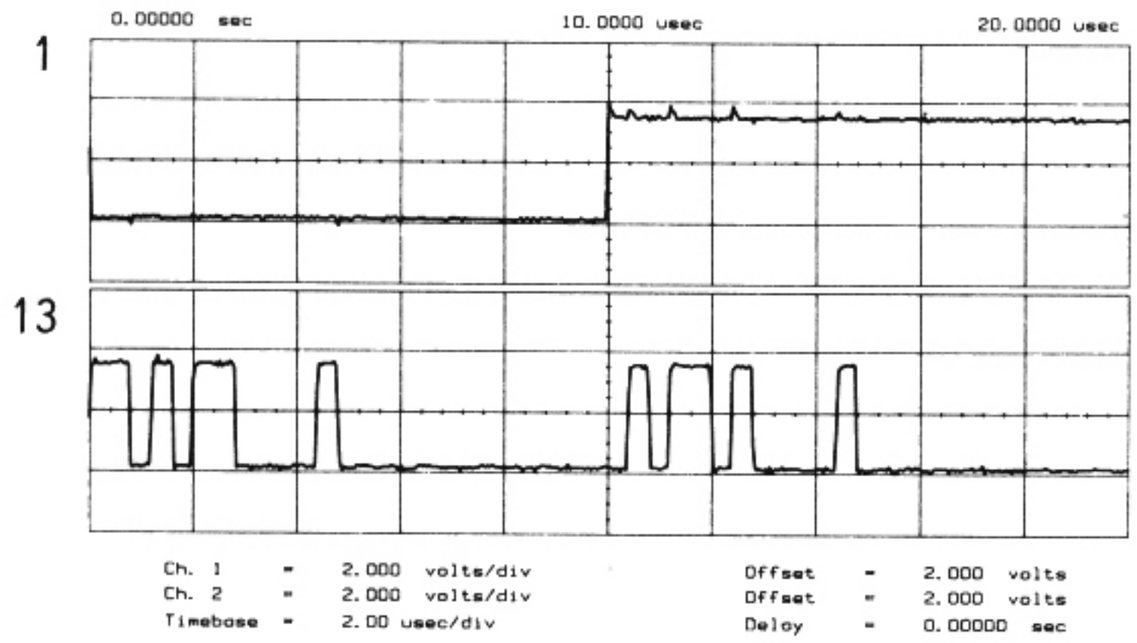


AD2: Log. amp. interface

1
13 *

BOARD : AD2

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2, typical data

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

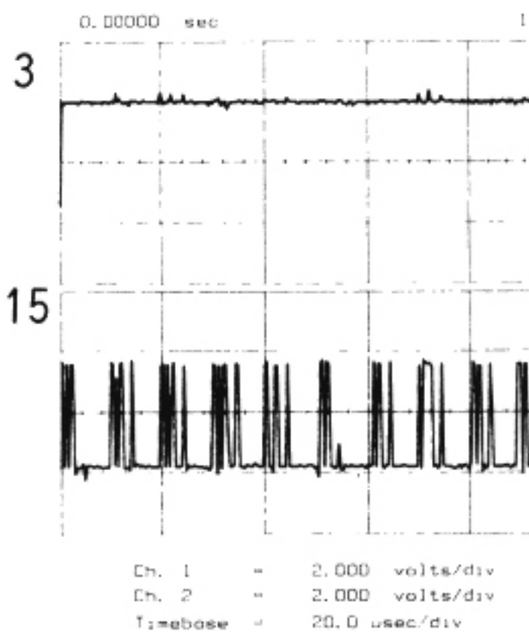
   Zero span
   Sweep time 50 µs/DIV

cct. drg. Fig. 31 refers

3
15 *

BOARD : AD2

TEST POINT : IC57b pin 6 (Fig. 34) f
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) f

PROCEDURE :

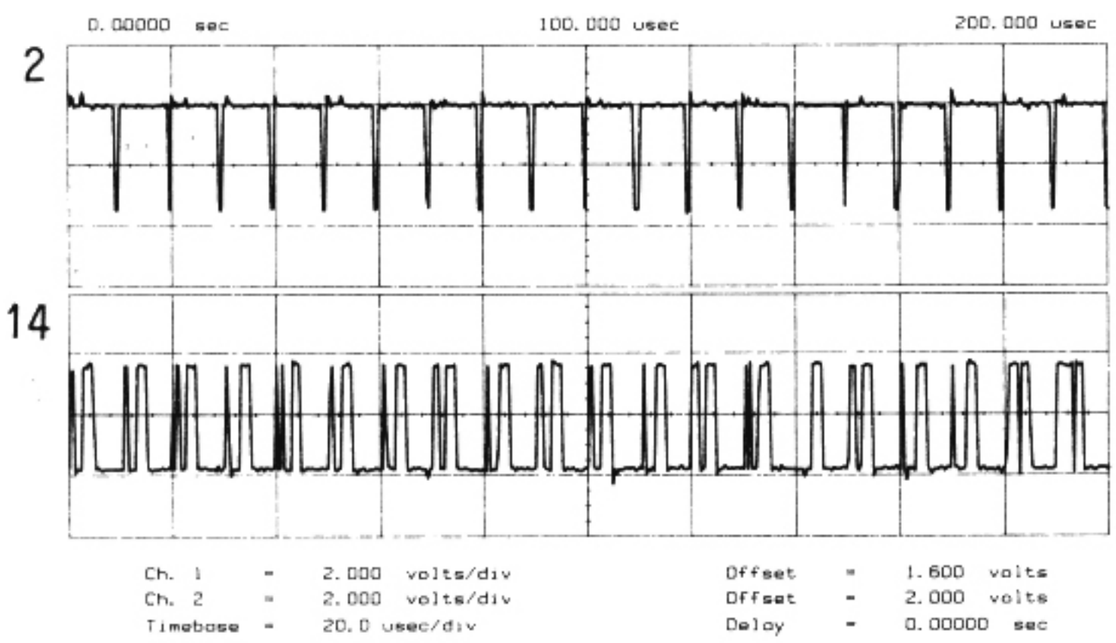
1. Press PRESET then select the fo

   Zero span

2
14 *

BOARD : AD2

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2

PROCEDURE :

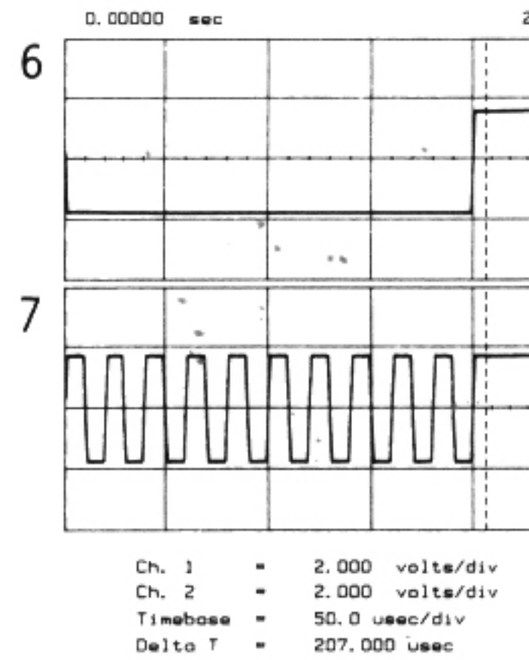
1. Press PRESET.

cct. drg. Fig. 31 refers

6
7

BOARD : AD2

TEST POINT : IC32b pin 11 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC46b pin 10 for Ch. 2

PROCEDURE :

1. Press PRESET.

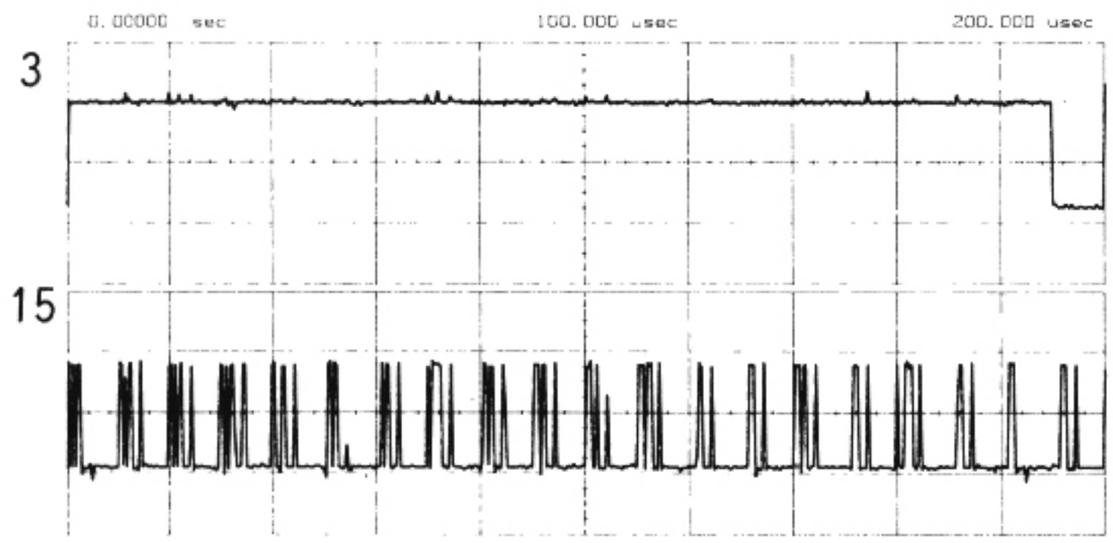
Fig. 34a
Chap. 7
Page 76

(See Fig. 33a for waveforms 4 & 5)

3
15 *

BOARD : AD2

TEST POINT : IC57b pin 6 (Fig. 34) for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC20 pin 13 (Fig. 31) for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 setting:

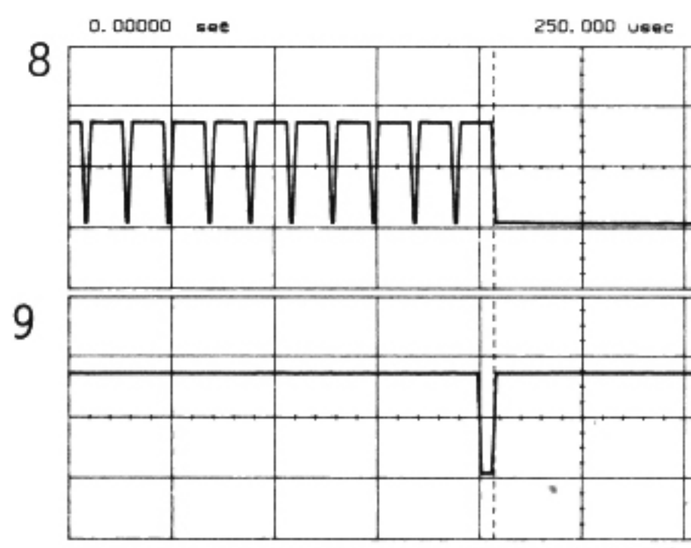
   Zero span

*cct. drg. Fig. 31 refers

8
9

BOARD : AD2

TEST POINT : IC46b pin 9 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC32b pin 8 for Ch. 2

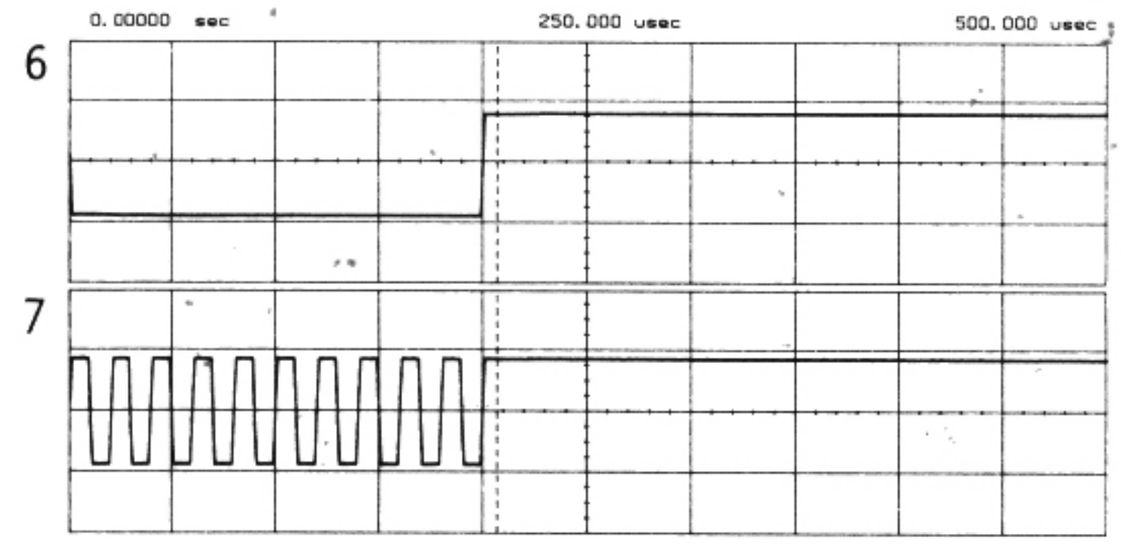
PROCEDURE :

1. Press PRESET.

6
7

BOARD : AD2

TEST POINT : IC32b pin 11 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC46b pin 10 for Ch. 2

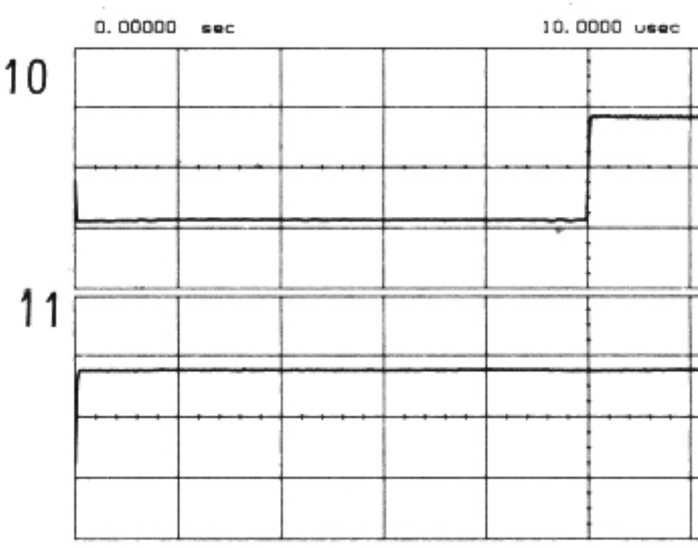
PROCEDURE :

1. Press PRESET.

10
11

BOARD : AD2

TEST POINT : IC46b pin 10 for Ch. 1
SCOPE SETTING [DEFAULT]

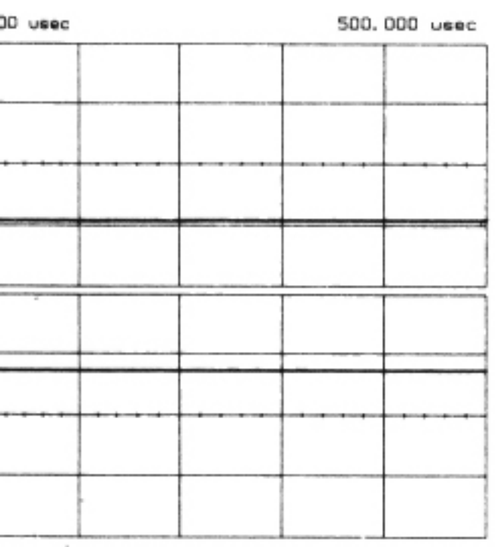


TEST POINT : IC46b pin 9 for Ch. 2

PROCEDURE :

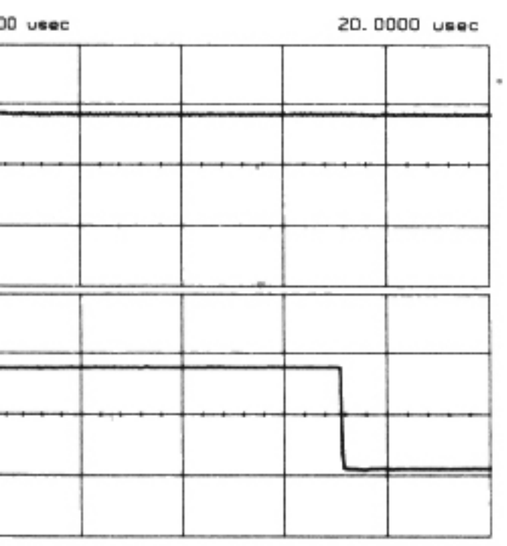
1. Press PRESET then select the following 2

   Zero span
   Sweep time 50 µs/DIV



Offset - 2.000 volts
Offset - 2.000 volts
Delay - 0.00000 sec

Stop - 207.000 usec

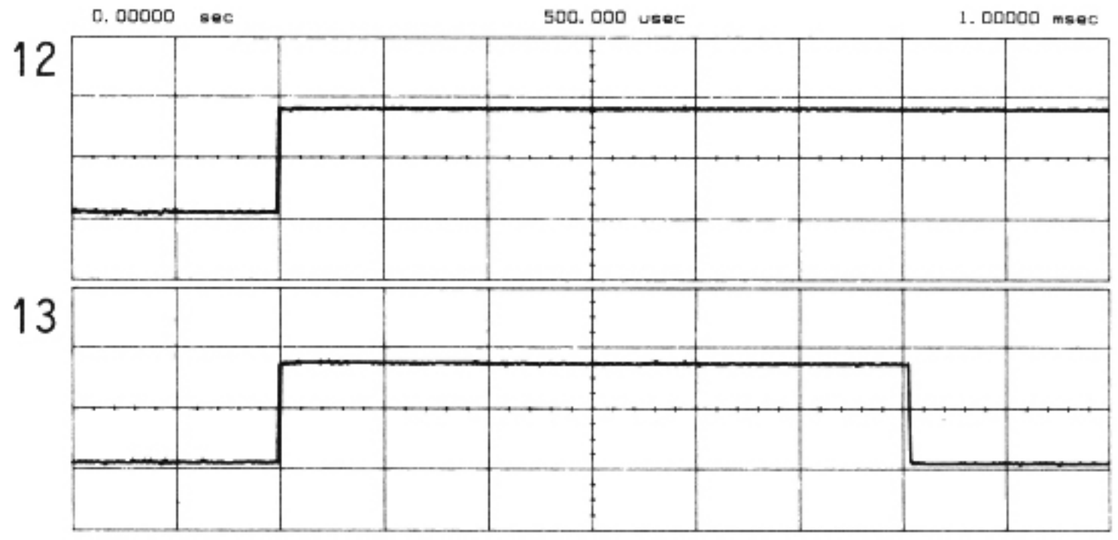


Offset - 2.000 volts
Offset - 2.000 volts
Delay - 0.00000 sec

wing 2382 settings:

12
13 BOARD : AD2

TEST POINT : IC32b pin 11 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 - 2.000 volts/div
Ch. 2 - 2.000 volts/div
Timebase - 100 usec/div

Offset - 2.000 volts
Offset - 2.000 volts
Delay - 0.00000 sec

TEST POINT : IC32b pin 9 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Zero span
   Sweep time 100 µs/DIV

Fig. 34a

May 86

PART OF
AD 2
44828-480E

FROM SHEET THREE

GATED 10MHz

IC10
÷ 10

SAMPLING INCREMENTAL DELAY GENERATOR

SAMPLING PERIOD CLOCK

ENABLE DIVIDERS

IC40 LS161
IC41 LS161
IC42 LS161
IC43 LS193
IC44 LS193
IC45 LS193

CLR, CLK, EP, ET, LD, RC, A B C D, DOWN, UP, LOAD, CLR, BW, Q A Q B Q C Q D, +5V

IC51(d) LS04
IC53(d) LS00
IC55(c) LS32
IC46(a) LS74
IC56(b) LS08
IC52(a) LS00

RELOAD ON TERMINAL COUNT

ENABLE DATA CONVERSION

FROM IC36 PIN 15 LOG AMP ENABLE (L)

DISABLE

DISABLE

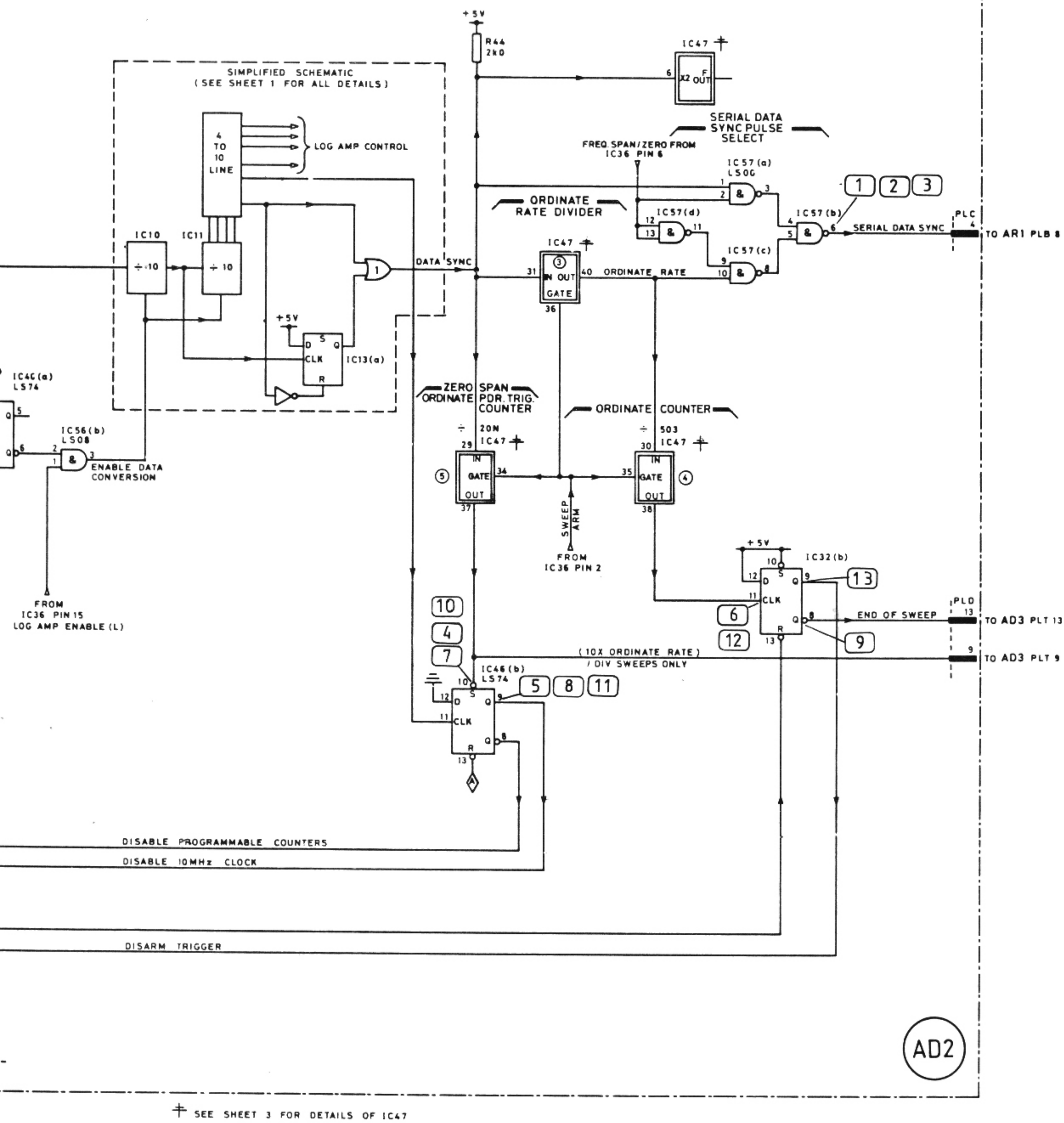
DISARM

R43 4k7
R42 4k7
R41 4k7

PLAT 7 3 4 5 6 2

Drg.No. Z44828-480E
Sh.4 Iss.1

AD2 : Log. amp.

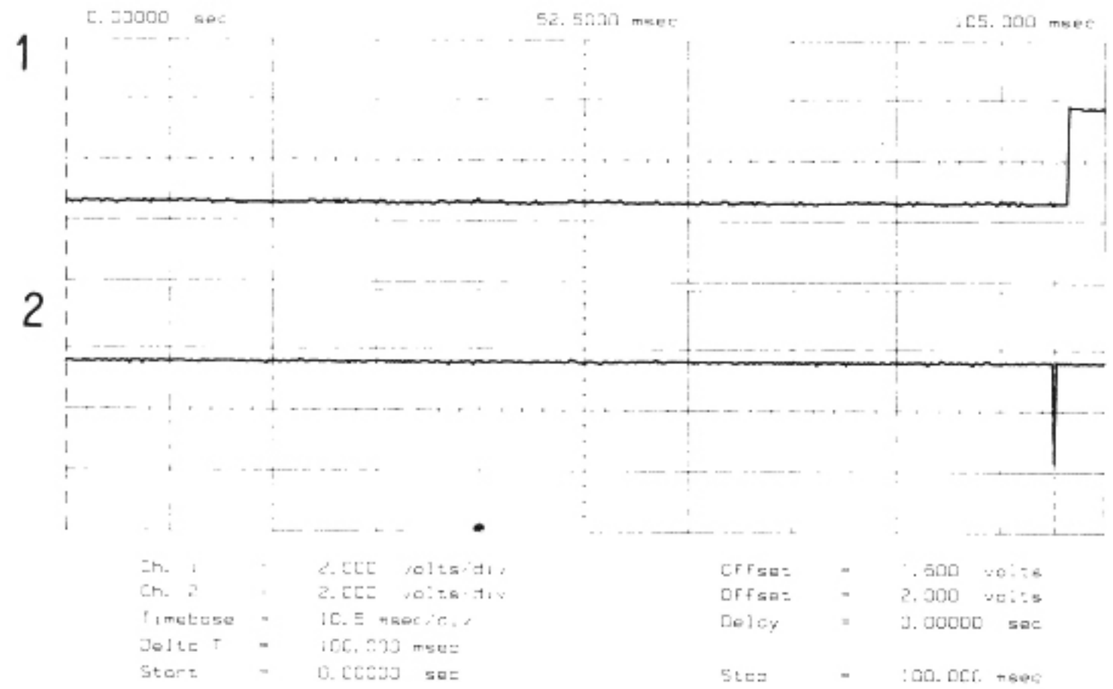


AD2 : Log. amp. interface

1
2

BOARD : AD3

TEST POINT : TP3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC32 pin 7 (Fig. 36) for Ch. 2

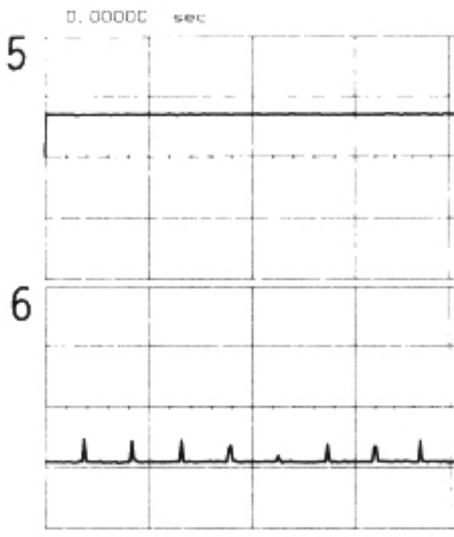
PROCEDURE :

1. Press PRESET.

5
6

BOARD : AD3

TEST POINT : IC28 pin 9 for Ch.
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : IC31b pin 9 for Ch.

PROCEDURE :

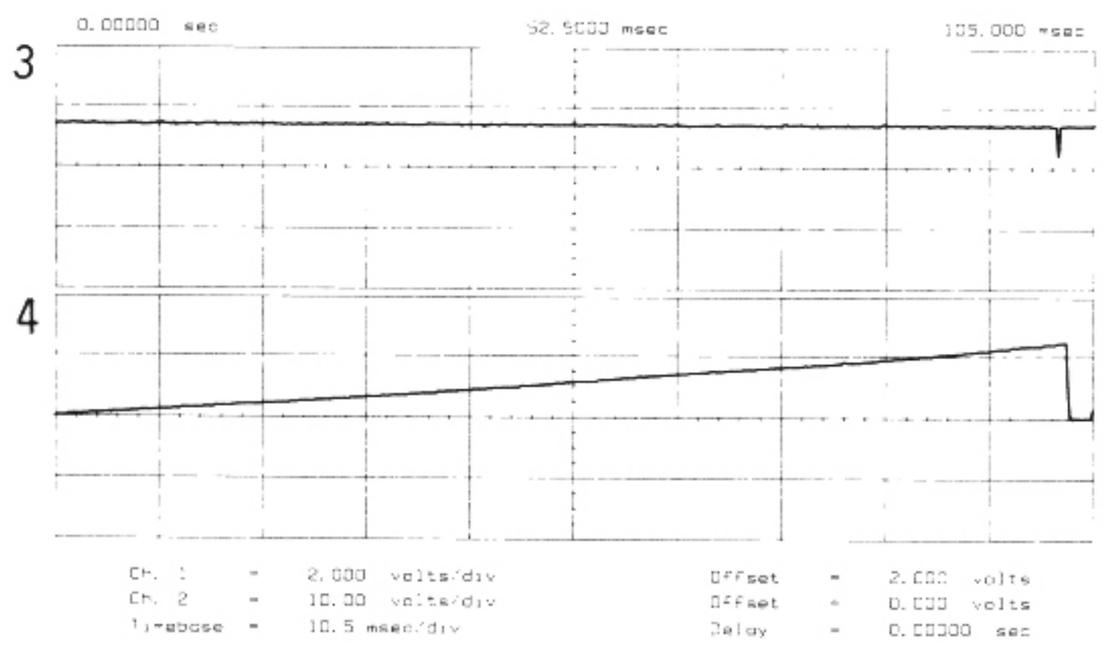
1. Press PRESET then select th

Span 10 MHz/DIV

3
4

BOARD : AD3

TEST POINT : IC12 pin 24 (Fig. 36) for Ch. 1
SCOPE SETTING :
TRIGGER PT : TP3



TEST POINT : AB1 TP5 (Fig. 14) for Ch. 2

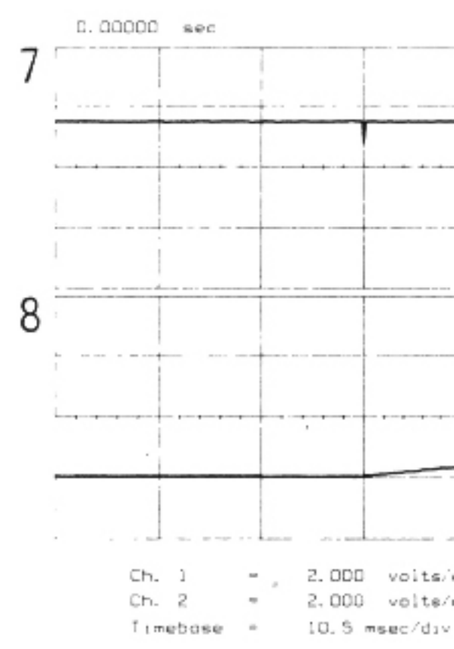
PROCEDURE :

1. Press PRESET.

7
8

BOARD : AD3

TEST POINT : IC32 pin 7 (Fig. 36
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : AB1 TP5 (Fig. 14) f

PROCEDURE :

1. Press PRESET then select th

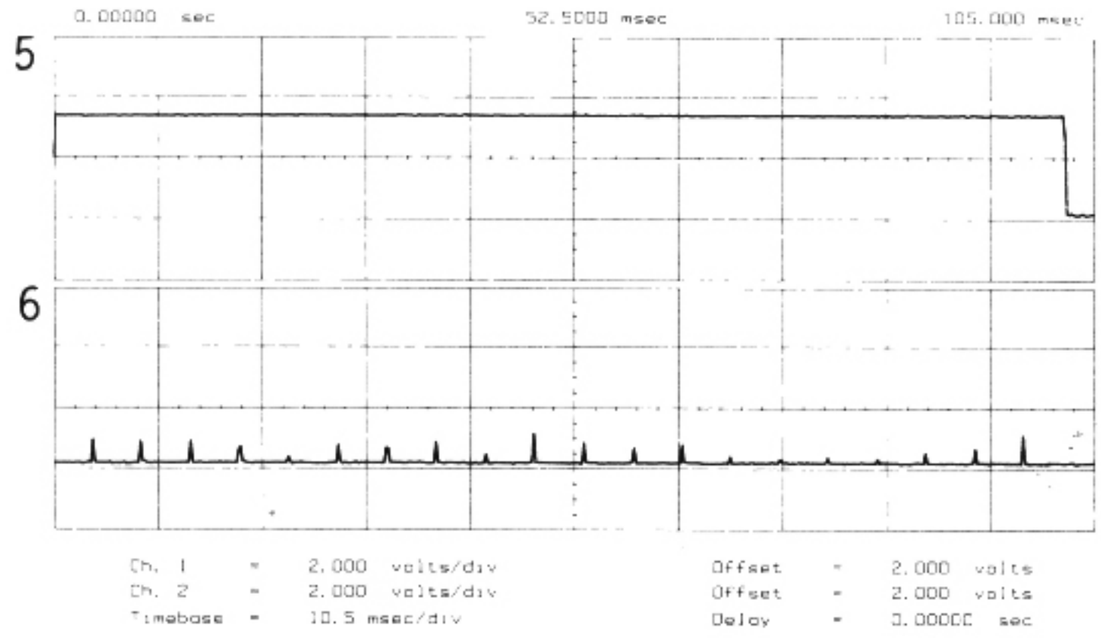
Ref. freq. 14
Span 10

Fig. 35a
Chap. 7
Page 78

5
6

BOARD : AD3

TEST POINT : IC28 pin 9 for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : IC31b pin 9 for Ch. 2

PROCEDURE :

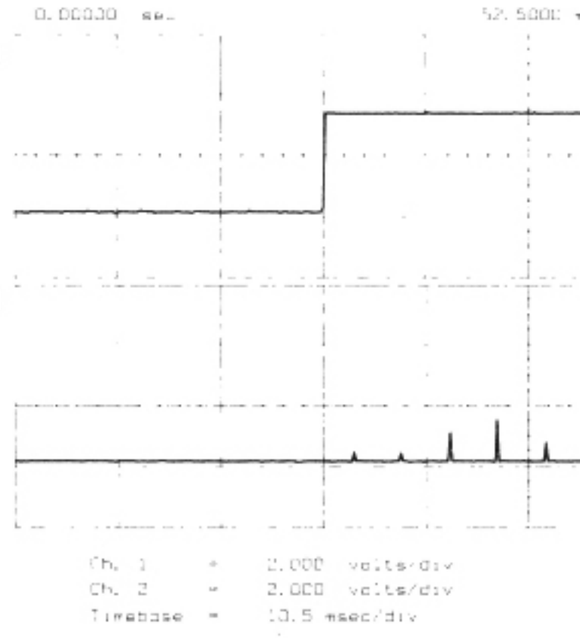
1. Press PRESET then select the following 2382 setting:

Span	10 MHz/DIV

9
10

BOARD : AD3

TEST POINT : IC28 pin 9 for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : IC31b pin 9 for Ch. 2

PROCEDURE :

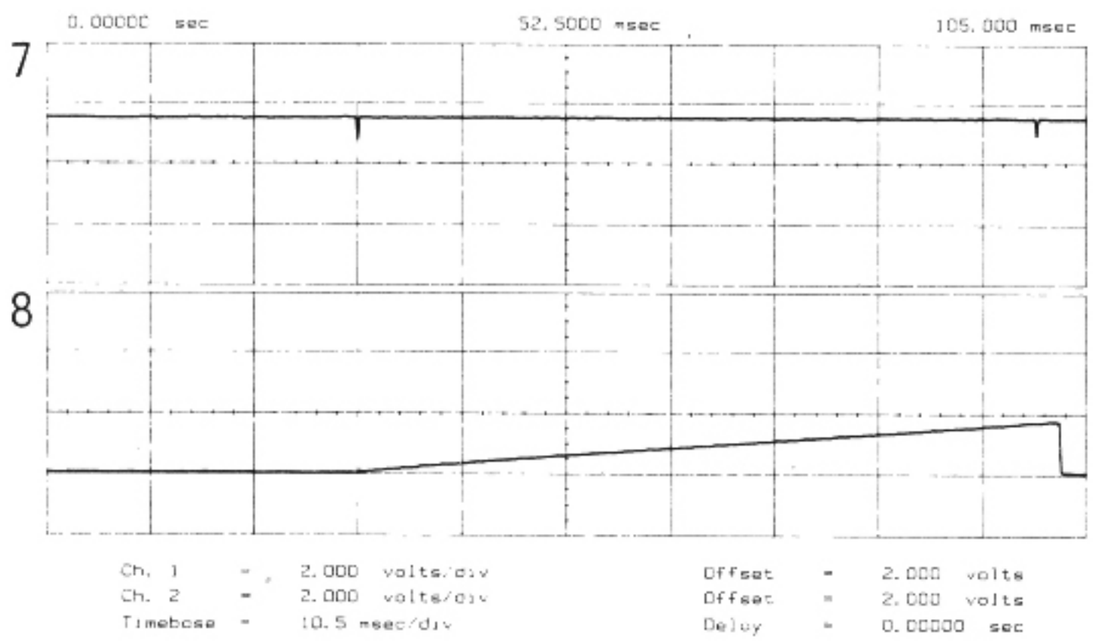
1. Press PRESET then select the followi

Ref. freq.	14.6 MHz
Span	10 MHz/DIV

7
8

BOARD : AD3

TEST POINT : IC32 pin 7 (Fig. 36) for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : AB1 TP5 (Fig. 14) for Ch. 2

PROCEDURE :

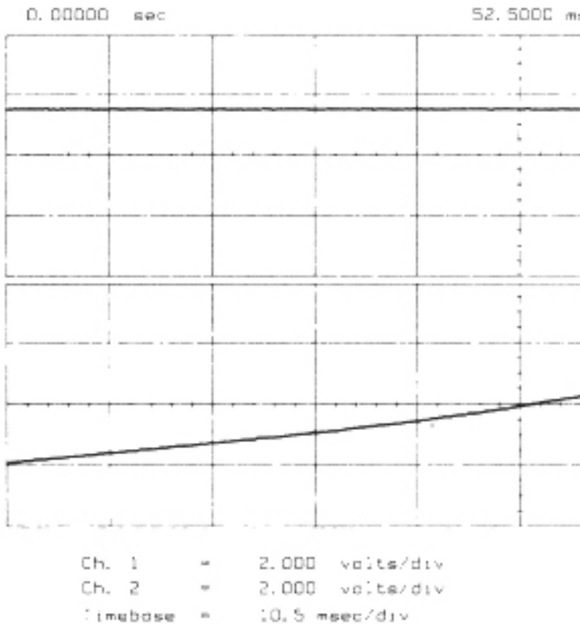
1. Press PRESET then select the following 2382 setting:

Ref. freq.	14.6 MHz
Span	10 MHz/DIV

11
12

BOARD : AD3

TEST POINT : IC32 pin 7 (Fig. 36) for Ch.
SCOPE SETTING
TRIGGER PT : TP3



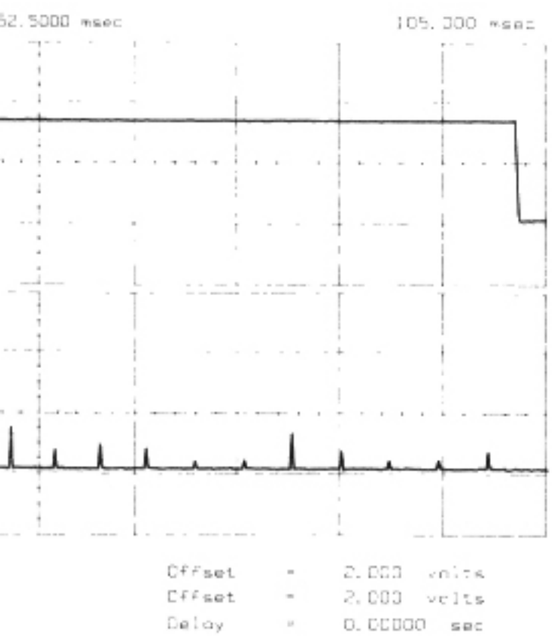
TEST POINT : AB1 TP5 (Fig. 14) for Ch. 2

PROCEDURE :

1. Press PRESET then select the followir

Ref. freq.	381 MHz
Span	10 MHz/DIV

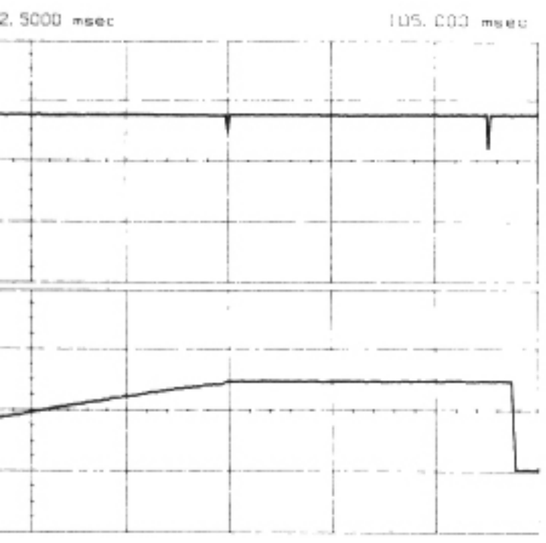
Waveforms sequence for AD3



llowing 2382 settings:

Hz
/DIV

r Ch. 1



h. 2

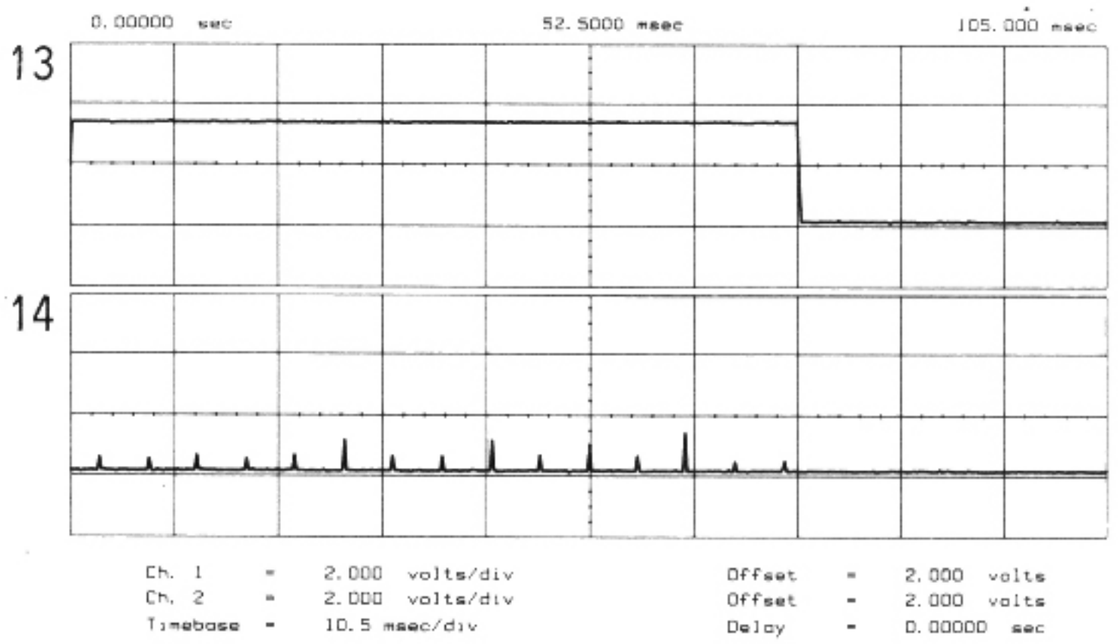
llowing 2382 settings:

z
/DIV

13 BOARD : AD3

14

TEST POINT : IC28 pin 9 or 15 (Fig. 35) for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : IC31b pin 9 (Fig. 35) for Ch. 2

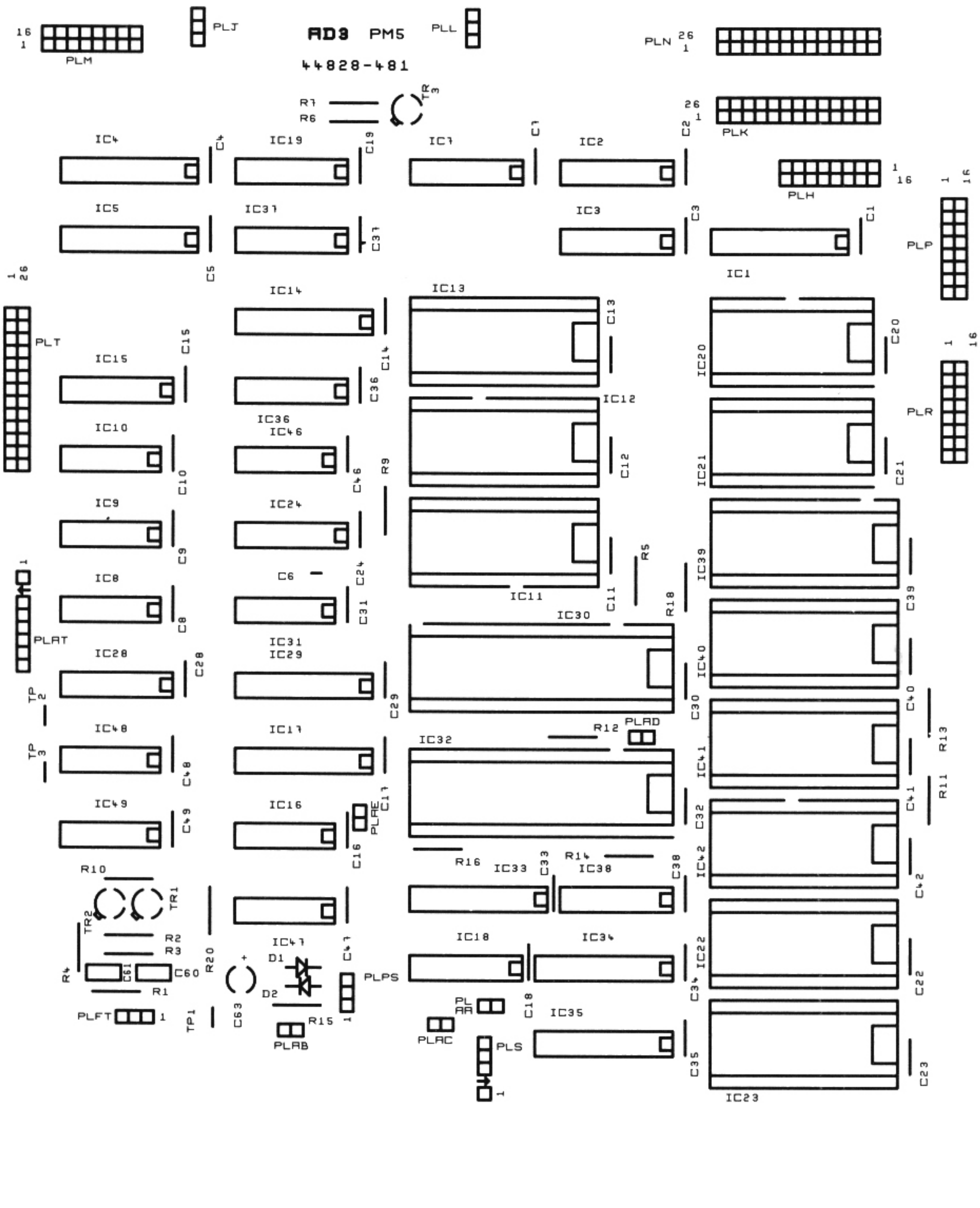
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

Ref. freq.	381 MHz
Span	10 MHz/DIV

Fig. 35a

May 86



Component layout for AD3

Fig. 35

May 86

PART OF
AD 3
44828-481U

TO AD2 PLD 11

PLT 11

20 BIT FREQUENCY COUNTER

AUTOTEST INVERTER

+5V
R20 1k0
IC47(c) LS04
PLAT 8

PLJ
TP1
PLFT
FROM AB7 PL4B

TTL DRIVER
+5V
R2 1k5
C60 4n7
TR1 MPSL08
R3 5k1
C61 4n7
TR2 2N2369
R4 1k0
R1 200R
2 SELECTED OSC. FREQ.

IC49(a) LS08
+5V
CLK1
COUNT/LOAD
CLR
IC16 74197
PART OF IC30
EXTERNAL 4 BIT COUNTER/LATCH
BUFFER
CS20
FROM IC37 PIN 15 SHEET 4

CS 21
FROM IC37 PIN 14 SHEET 4

GATE PERIOD GENERATOR
PART OF IC30
+5V
R5 15k
IC31(a) 74S74
TP2
17 21 22

÷ 5
IC8(a) LS90
PLT 8 10 MHz
FROM AD2 PLD 8
2MHz

IC9(b) LS74

÷ 20,000
PART OF IC30
10mS CLK TIK INTERRUPT
2MHz
TO IC46(c) PINS 9, 10 SHEET 2

GATE TRIGGER CS22
FROM IC37 PIN 13 SHEET 4

÷ 2
IC8(b) LS90

µP DATA BUS

PART OF IC30
INT. 7·5
TO IC32 (µP) PIN 7 SHEET 2

PLT 9
10X ORDINATE RATE
FROM AD 2 PLD 9

SWEEP ARM LATCH
SWEEP ENABLE LATCH

CS23
FROM IC37 PIN 12 SHEET 4
IC29 LS273
IC28 LS75
D0
D7
5 9 13

PLH 4
RESET IN
PLPS 1

TO IC24 PIN 2 SHEET 3

IC48(a) LS00
INT. 5·5
TO IC32 (µP) PIN 9 SHEET 2

TP3
1
PLT 17
SWEEP TRIG.
FROM AD2 PLD 17

LOW POWER STANDBY
SERIAL DATA ENABLE
DISPLAY INHIBIT

PLS 5
PLH 7
PLT 19

TO AD4 PLAA 3
TO AR1 PLA 7
PLA 11
TO AD2 PLD 19

✱ SEE CIRCUIT AD0 FOR CONNECTION DETAILS
† REPEATED ON THIS DIAGRAM FOR CIRCUIT CLAR

Drg. No. Z44828-481U
Sh. 1 Iss. 2

AD3 : Microproc

EQUENCY COUNTER

IC17
LS244

BUFFER

D7
D0

CS20

FROM IC37
PIN 15 SHEET 4

PART OF IC30

IC30
9513

DETAILS OF IC30
(INDIVIDUAL SECTIONS
SHOWN WHERE USED)

GATE 1
GATE 2
GATE 3
GATE 4
GATE 5

SOURCE 1
SOURCE 2
SOURCE 3
SOURCE 4
SOURCE 5

GATE 5A
GATE 4A
GATE 3A
GATE 2A
GATE 1A

DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0

+5V

F OUT
OUT 1
OUT 2
OUT 3
OUT 4
OUT 5

RD
CS
WR
A0

A0 FROM IC34 PIN 19 SHEET 2
WR(L) FROM IC47 PIN 18 SHEET 2
CS10 FROM IC19 PIN 9 SHEET 4
RD (L) FROM IC47 PIN 4 SHEET 2

μP DATA BUS
FROM SHEET 2

5MHz TO
IC32 PIN 1
SHEET 2

÷ 20,000

PART OF IC30

X2 F OUT

7 10mS CLK TTR INTERRUPT → TO IC12 PIN 25 SHEET 2

TO IC46 (c)
PINS 9, 10
SHEET 2

÷ 32

+5V

IC9(a)
LS74

IC10(a)
LS93

IC10(b)
LS93

BAUD RATE
CLOCK

TO IC11 PINS 9, 25 SHEET 2
& PLP PIN 15 SHEET 2

NON-LINEAR SWEEP GENERATOR

PART OF IC30

GRADIENT DIV RATIO

2X(SWEEP SPEED DIV RATIO)

BREAK POINT TRIGGER GENERATOR

IC31(b)
LS74

INT. 6·5 → TO IC32 (μP) PIN 8 SHEET 2

CS10

7·5 → TO IC32 (μP) PIN 7 SHEET 2

R7
2k4

R6
33k

TR3
2N2369

SWEEP CLOCK

PLL 1
2
3

TO AB1 PLF 2

TO SHEET TWO

PLH 3 5MHz → TO AR1 PLA 3

PLT 18 → TO AD2 PLD 18

T AD0 FOR CONNECTION DETAILS
THIS DIAGRAM FOR CIRCUIT CLARITY

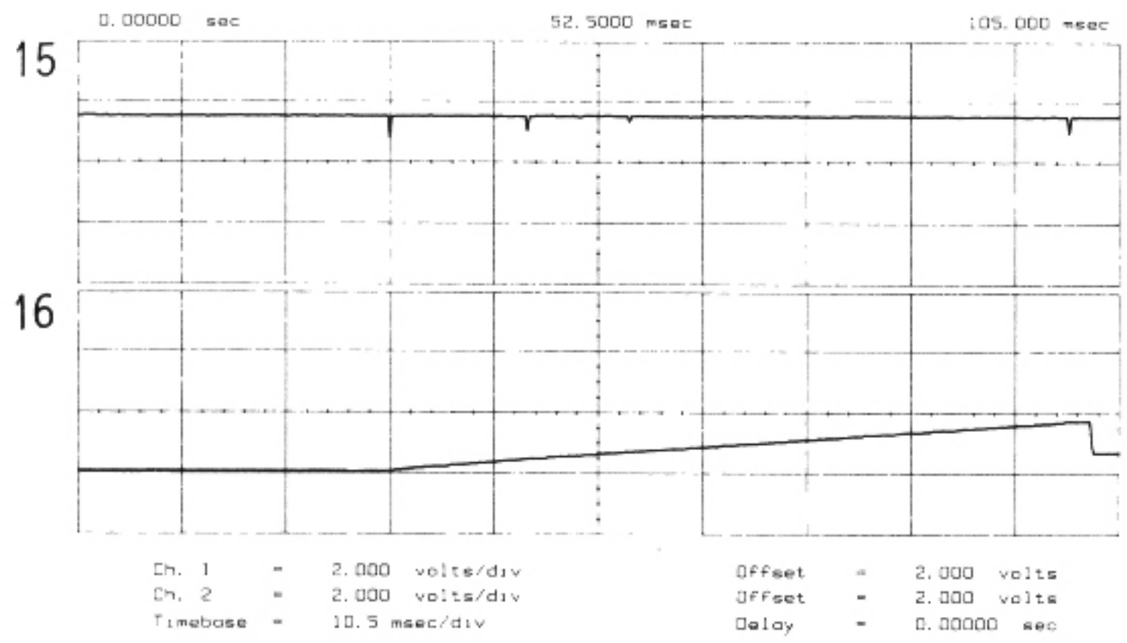
AD3

AD3 : Microprocessor

15
16

BOARD : AD3

TEST POINT : IC32 pin 7 for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : AB1 TP5 (Fig. 14) for Ch. 2

PROCEDURE :

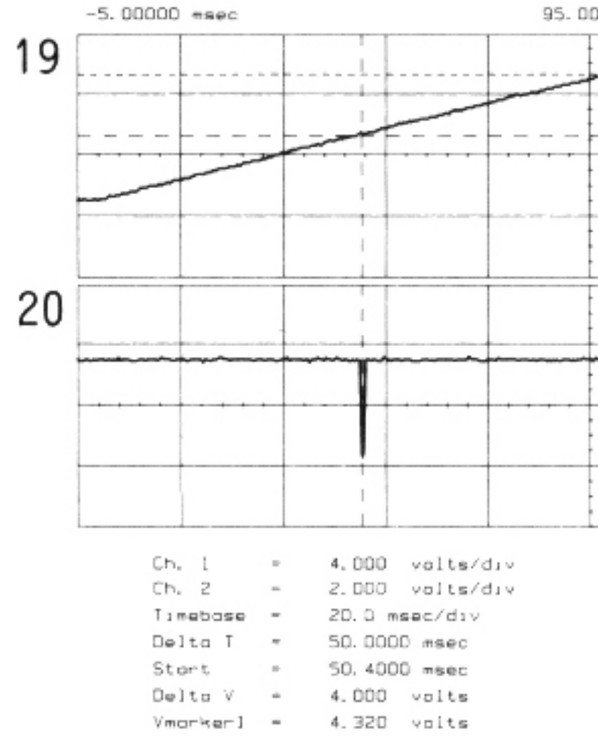
1. Press PRESET then select the following 2382 settings:

Ref. freq.	14.6 MHz
Span	10 MHz/DIV
[MKR 1 and 2] ON	10 and 20 MHz teeth
[FREQ COUNT]	On

19
20

BOARD : AD3

TEST POINT : AB1 TP4 (Fig. 14) for Ch.
SCOPE SETTING
TRIGGER PT : TP3 falling edge



TEST POINT : IC32 pin 7 for Ch. 2

PROCEDURE :

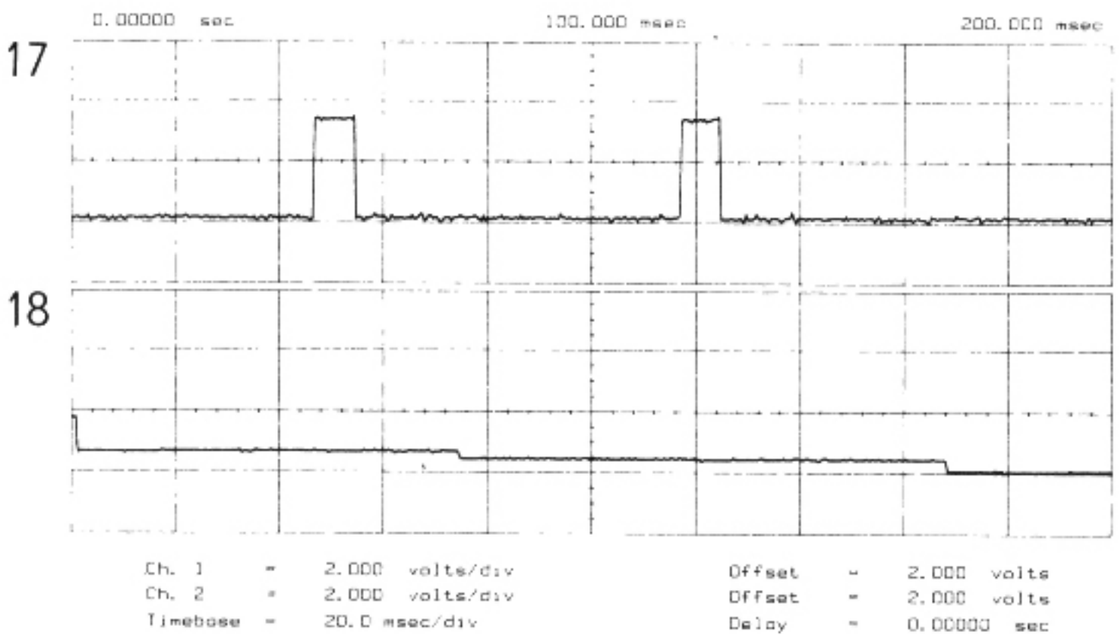
1. Press PRESET then select the follo

Span	100 k
[FREQ COUNT]	On

17
18

BOARD : AD3

TEST POINT : TP2 for Ch. 1
SCOPE SETTING
TRIGGER PT : TP3 rising edge



TEST POINT : AB1 TP5 (Fig. 14) for Ch. 2

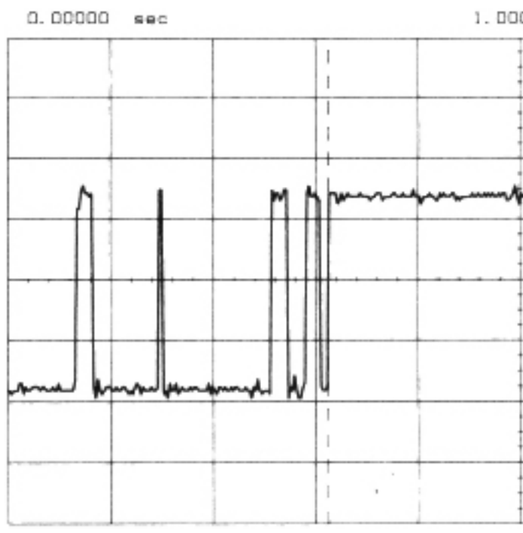
PROCEDURE :

1. Press PRESET.

21

BOARD : AD3

SCOPE SETTING
TRIGGER PT : TP3



TEST POINT : TP2 (Fig. 35) for Ch. 2

PROCEDURE :

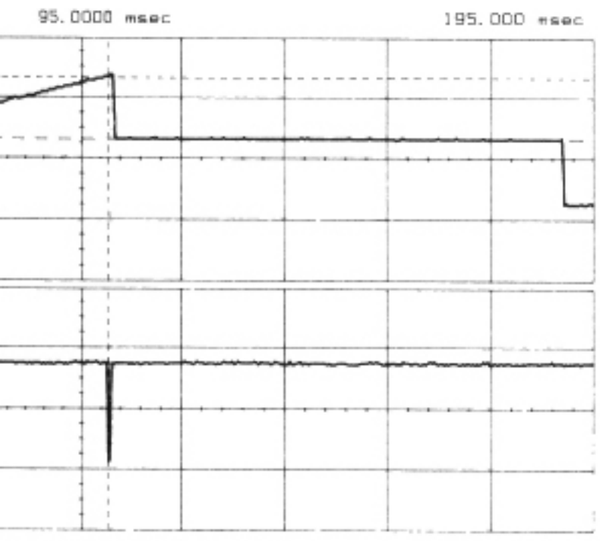
1. Press PRESET then select :

[2ND FUNCT]
[RES 1 Hz] on the markers sec

A typical waveform should appear

Waveforms sequence for AD3

r Ch. 1



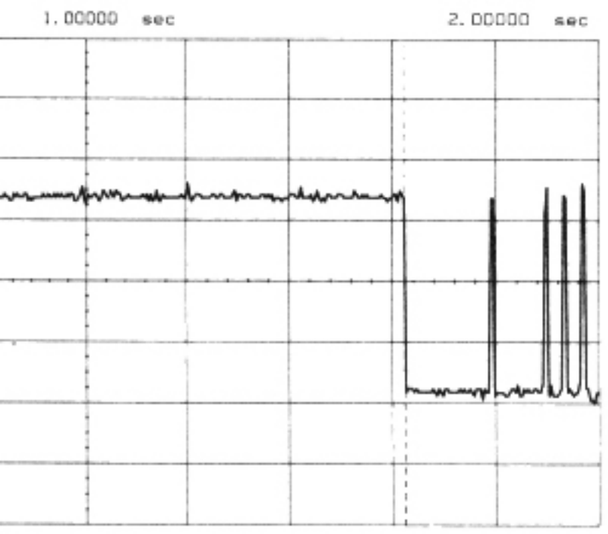
v Offset = 3.000 volts
v Offset = 2.000 volts
Delay = -5.00000 msec

Stop = 100.400 msec

Vmarker2 = 8.320 volts

following 2382 settings:

100 kHz/DIV
On



:v Offset = 2.000 volts
Delay = 0.00000 sec

Stop = 1.62500 sec

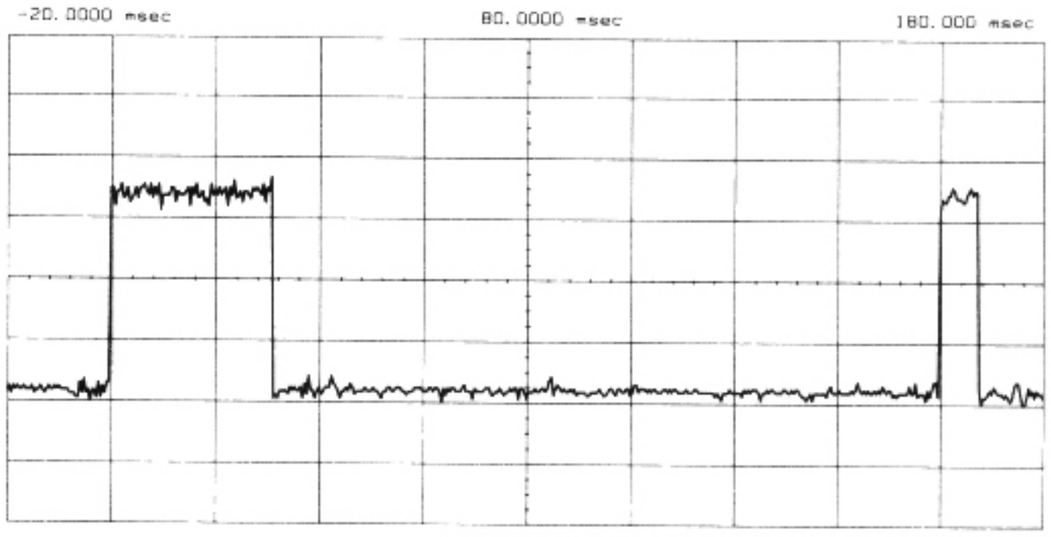
. 2

rs section

pear with pulse widths of 1 s, 30 ms and 7.8 ms.

22 BOARD : AD3

SCOPE SETTING
TRIGGER PT : TP3



Ch. 2 = 1.000 volts/div
Timebase = 20.0 msec/div

Offset = 2.000 volts
Delay = -20.0000 msec

TEST POINT : TP2 (Fig. 35) for Ch. 2

PROCEDURE :

1. Press PRESET then select

[2ND FUNCT]
[RES 1 Hz] on the markers section

Fig. 36a

May 86

PART OF
AD3
44828-481U

FROM AD0 *
PLS
3 → +5V
2
1

PLK
FROM AB1 PLE 13 — 13 INPUT ATTEN. OVERLOAD

PLN
FROM AF2 PLA
20 REF. UP
8 REF. DOWN
19 MARKER UP
9 MARKER DOWN
18 HZ/DIV
10 SELECT
17 KEY ON
11 KEY OFF

PLT
FROM AD2 PLD 13 — 13 END OF SWEEP

FROM IC23 PIN 1 SHEET 3
FROM IC30 PIN 7 SHEET 1
3

SLAVE INTERRUPT CONTROLLER

IC12 8259A
IR0 18, IR1 19, IR2 20, IR3 21, IR4 22, IR5 23, IR6 24, IR7 25
INTA 26, INT 17
A0 27, CAS0 12, CAS1 13, CAS2 15
RD 3, WR 2, CS 1
D0 11, D1 10, D2 9, D3 8, D4 7, D5 6, D6 5, D7 4
D0, D7, 8
CS02 — FROM IC19 (a) PIN 6 SHEET 4

PLAT
1, 2, 3, 7

TO SHEET 1
8

PLAT
4, 5, 6

µP DATA BUS

MASTER INTERRUPT CONTROLLER

IC13 8259A
IR0 18, IR1 19, IR2 20, IR3 21, IR4 22, IR5 23, IR6 24, IR7 25
INTA 26, INT 17
+5V 16
A0 27, CAS0 12, CAS1 13, CAS2 15
RD 3, WR 2, CS 1
D0 11, D1 10, D2 9, D3 8, D4 7, D5 6, D6 5, D7 4
D0, D7, 8
CS00 — FROM IC19 (a) PIN 7 SHEET 4

WR(L) — FROM IC47 PIN 10
RD (L) — FROM IC47 PIN 4
A0 — FROM IC34 PIN 2

FROM IC30 PIN 37 SHEET 1 — INT — 2
FROM IC31(b) PIN 9 SHEET 1 — INT
FROM IC48(a) PIN 11 SHEET 1 — INT

FROM IC28 PIN 12 SHEET 1 — 5MH

IC11 8251A
TXRDY 15, RXRDY 14, BD 16
CLK 20, RXC 25, TXC 9
RESET 21, C/D 12
RXD 3, CTS 17, TXD 19
RD 13, WR 10, CS 11
D0 27, 28, 1, 2, 5, 6, 7, 8 D7
D0, D7, 8
CS04 — FROM IC19 (a) PIN 5 SHEET 4

FROM IC10 PIN 11 SHEET 1 — BAUD RATE CLOCK

+5V
R10 4k7
IC46(b) LS32
IC47(d) LS04

TX
RX

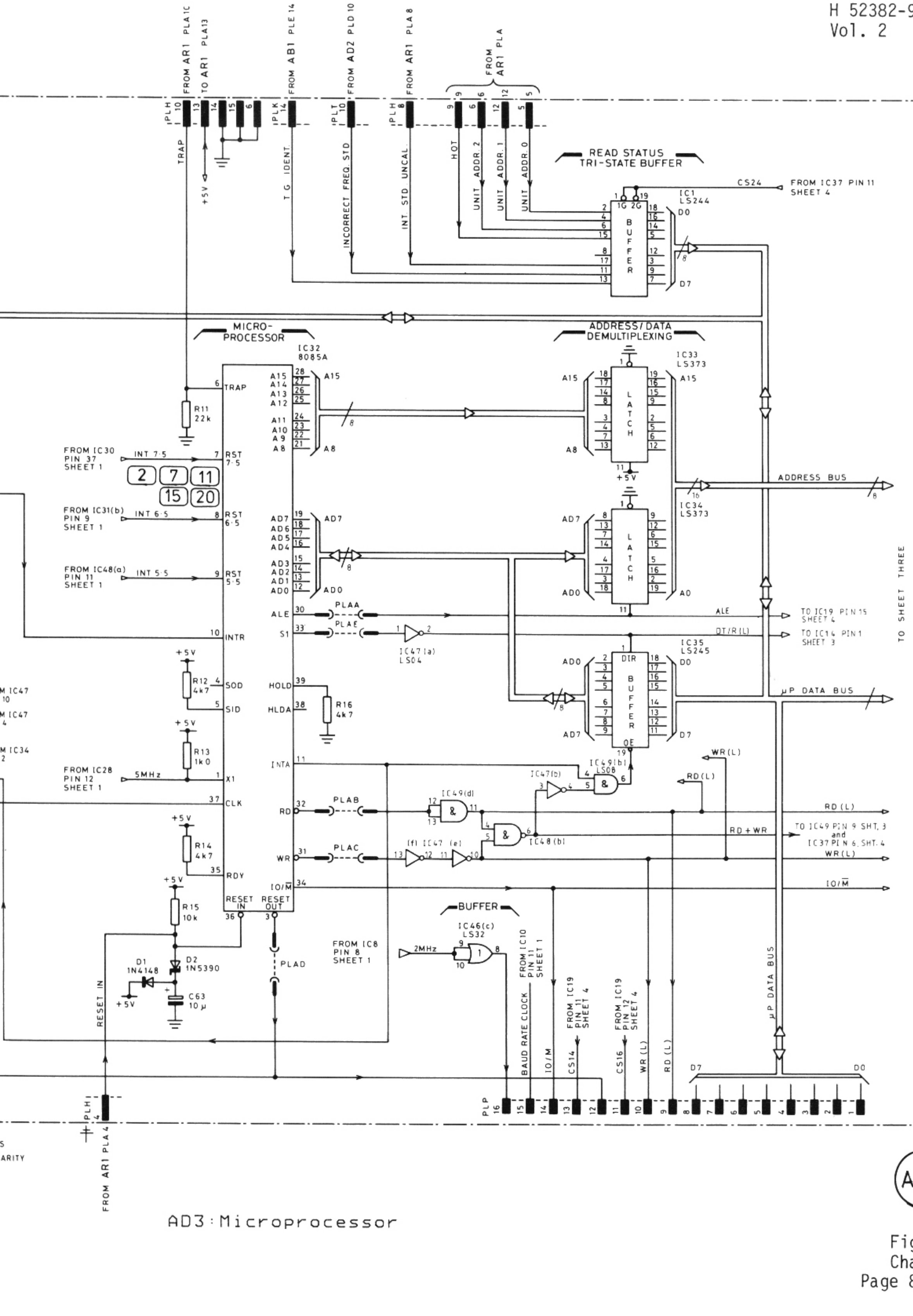
RESET IN
D1 1N4148
+5V

PLH
1 — TO AR1 PLA 1
2 — FROM AR1 PLA 2
4 — FROM AR1 PLA 4

FROM SHEET ONE

* SEE CIRCUIT AD0 FOR CONNECTION DETAILS
‡ REPEATED ON THIS DIAGRAM FOR CIRCUIT CLARITY

Drg. No. Z44828-481U
Sh. 2 Iss. 4



AD3 : Microprocessor

Fig. 36
Chap. 7
Page 81/82

PART OF
AD3
44828-481U

MEMORY CHIP SELECT DECODING

SEMI-CONDUCTOR MEMORY

ADDRESS BUS

WR(L)

RD(L)

A15 A14 A13 A12 A11

IC20 6116 — IC21 6116

OE WE

A10 A0 D7 D0 CS

RAM

IC18 LS138

G1 G2A G2B A B C Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

11 E000-E7FFH

E800H-EFFH

IC48(c) LS00

ADDRESS BUS 16

IO/M

µP DATA BUS 8

F000H-F7FFH

NON VOLATILE WRITE PROTECT

+5V

R9 4k7

C6 10n

IC24(a) LS221

FROM IC37 PIN 10 SHEET 4 — CS25

FROM IC29 PIN 16 SHEET 1 — LOW POWER STANDBY

CX RX A B Q R

IC46(d) LS32

FROM SHEET TWO

ADDRESS BUS

RD(L)

A15 A14 A5

IC39 A 27128

IC40 B 27128

IC41 C 27128

IC42 D 2764

EPROM

A13

IC38 LS138

0000H-3FFFH

4000H-7FFFH

8000H-BFFFH

C000H-FFFFH

IC46(a) LS32

C000H-DFFFH

µP DATA BUS

FROM SHEET 1 IC35 PIN 1

IC49(c)

FROM SHEET 2 IC48 PIN 6 — RD+WR

WR(L)

RD(L)

IO/M

µP DATA BUS

PLT 15 12

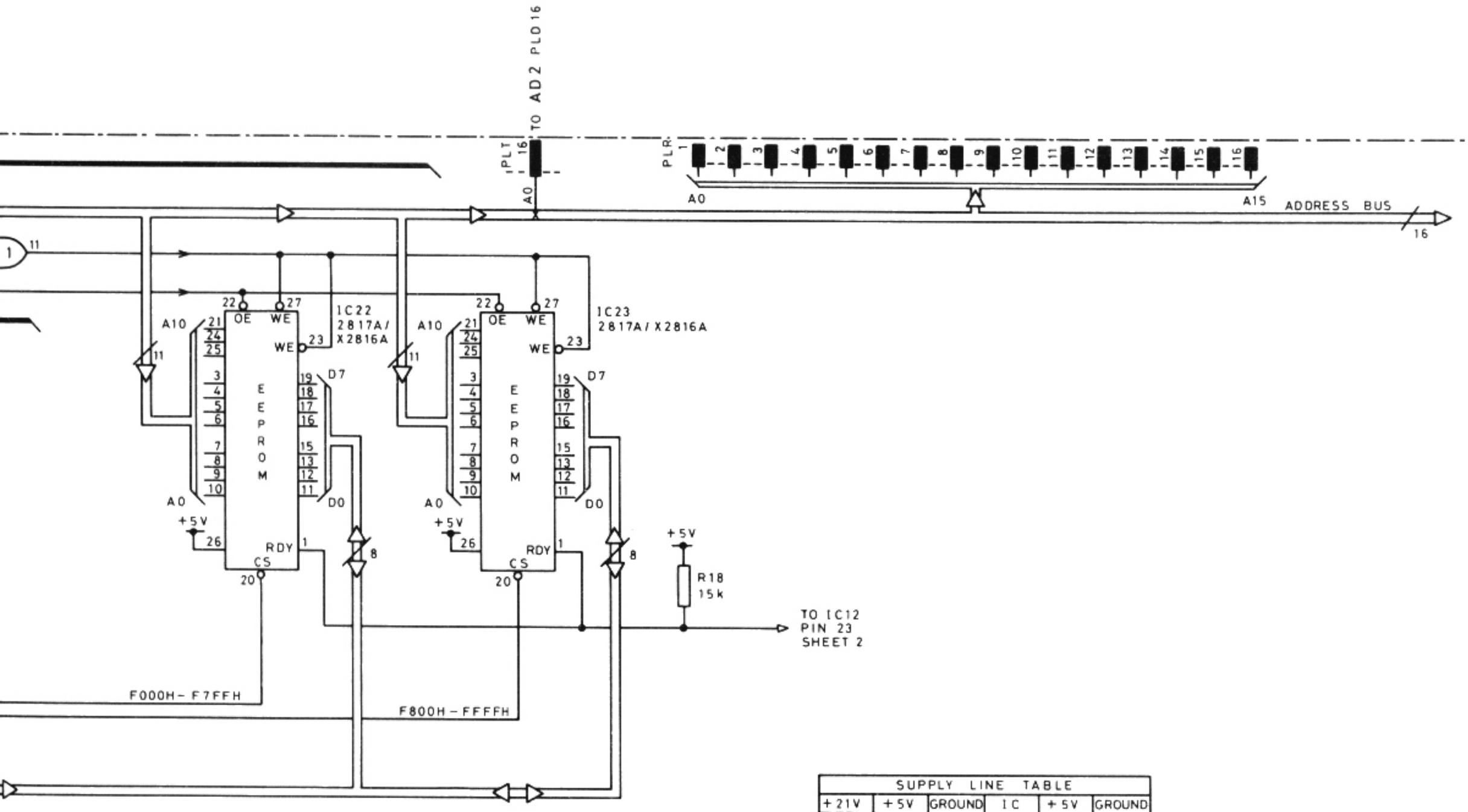
TO AD2 PLD 15

TO AD2 PLD 12

‡ SEE CIRCUIT AD0 FOR CONNECTION DETAILS

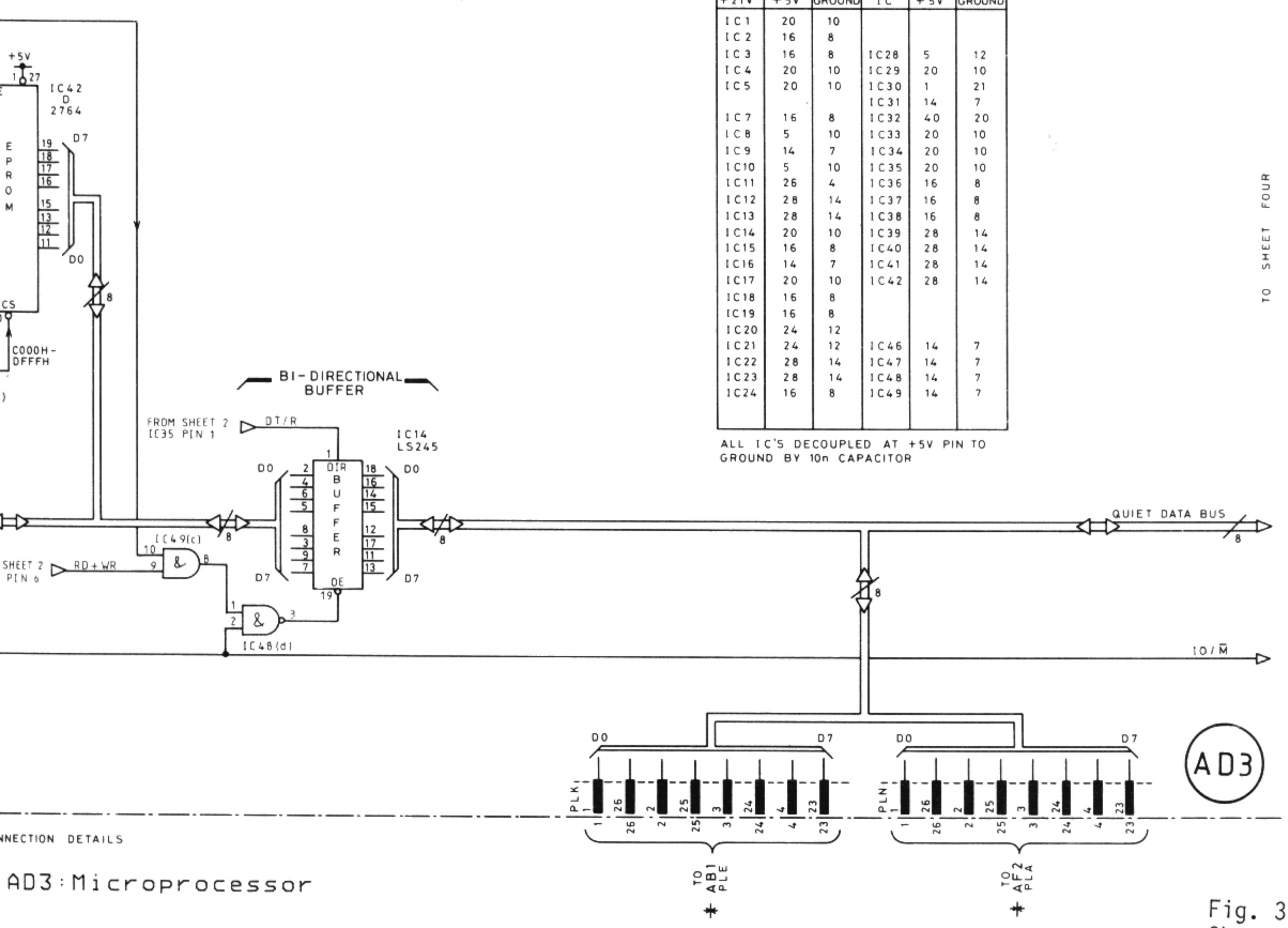
Drg.No. Z44828-481U
Sh.3 Iss.3

AD3: Microproc



SUPPLY LINE TABLE					
+21V	+5V	GROUND	IC	+5V	GROUND
IC1	20	10			
IC2	16	8			
IC3	16	8	IC28	5	12
IC4	20	10	IC29	20	10
IC5	20	10	IC30	1	21
			IC31	14	7
IC7	16	8	IC32	40	20
IC8	5	10	IC33	20	10
IC9	14	7	IC34	20	10
IC10	5	10	IC35	20	10
IC11	26	4	IC36	16	8
IC12	28	14	IC37	16	8
IC13	28	14	IC38	16	8
IC14	20	10	IC39	28	14
IC15	16	8	IC40	28	14
IC16	14	7	IC41	28	14
IC17	20	10	IC42	28	14
IC18	16	8			
IC19	16	8			
IC20	24	12			
IC21	24	12	IC46	14	7
IC22	28	14	IC47	14	7
IC23	28	14	IC48	14	7
IC24	16	8	IC49	14	7

ALL IC'S DECOUPLED AT +5V PIN TO GROUND BY 10n CAPACITOR



CONNECTION DETAILS

AD3 : Microprocessor

ADDRESS BUS

PART OF
AD 3
44828-481U

A3 A4 A5 A6 A7 A0

IO/M

IC36
LS138

CS4 *
CS0 *
CS1 *
CS5 *
CS2 *
CS6 *
CS7 *

I.F. CONTROL LATCHES

FROM IC34 PIN11
SHEET 2
ALE

RD + WR
FROM
SHEET 2

FROM SHEET THREE

FROM IC7
PIN 15
CS40
IC4
LS273

FROM IC7
PIN 14
CS41
IC5
LS273

QUIET DATA BUS

IO/M

D0 D7

PLT 1 26 2 25 3 24 4 23

TO AD2 PLD *

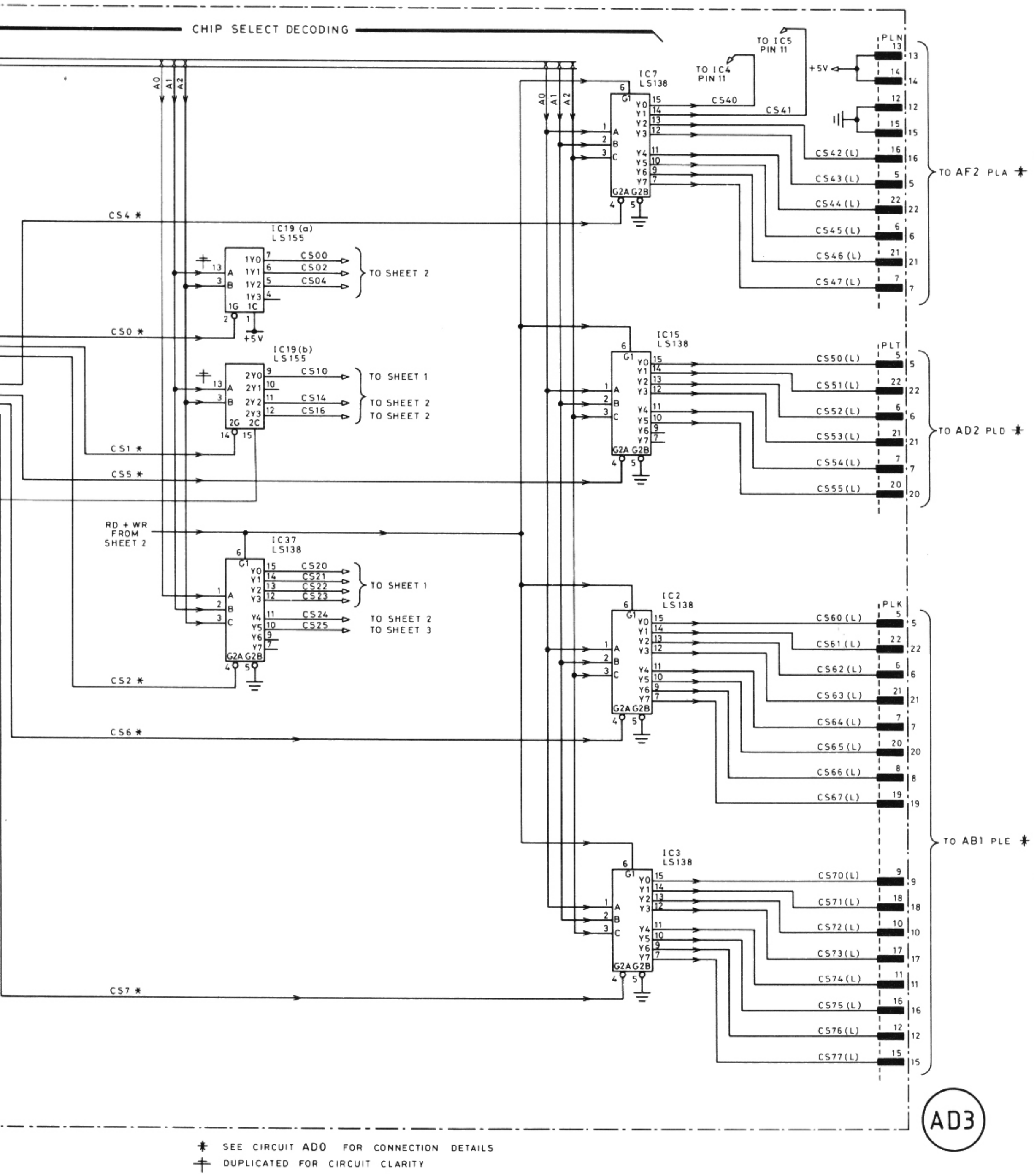
PLM 9 SPARE
8 SELECT 100Hz FILTER
10 SELECT 300Hz FILTER (L)
7 SELECT 1KHz FILTER (L)
11 BANDWIDTH 1
6 BANDWIDTH 2
12 100KHz XTAL BYPASS (L) CF ADJUST ENABLE (L)
PLS 5 XTAL FILTERS BYPASS (L)
4

PLM 13 SELECT 30KHz FILTER (L)
4 SELECT 100KHz FILTER (L)
14 SELECT 300KHz FILTER (L)
3 SELECT 1MHz FILTER (L)
15 30dB I.F. ATTEN. (L) A4
2 20dB I.F. ATTEN. (L) A3
16 20dB I.F. ATTEN. (L) A2
1 10dB I.F. ATTEN. (L) A1

TO AC5 PLL 2
TO AC5 PLL 9
TO AC5 PLL 3
TO AC4 PLX 7
TO AC4 PLX 8
TO AC4 PLX 9
TO AC5 PLL 6
TO AC3 PLH 5
TO AD1 PLW 7
TO AC3 PLH 3
TO AC3 PLH12
TO AC3 PLH 4
TO AC3 PLH11
TO AC3 PLH 10
TO AC2 PLD 5
TO AC2 PLD 6
TO AC2 PLD 7

AD3 : Microp

Drg. No. Z44828-481U
Sh. 4 Iss. 2



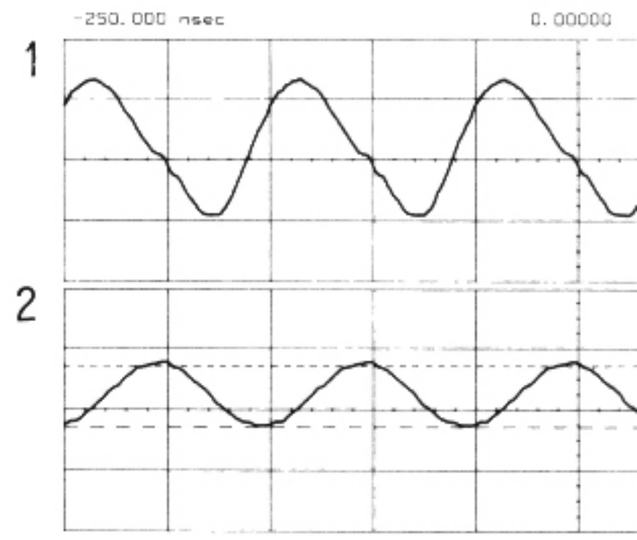
* SEE CIRCUIT AD0 FOR CONNECTION DETAILS
╪ DUPLICATED FOR CIRCUIT CLARITY

AD3 : Microprocessor

1 BOARD : AD4

2

TEST POINT : R15 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP8 for Ch. 2

PROCEDURE :

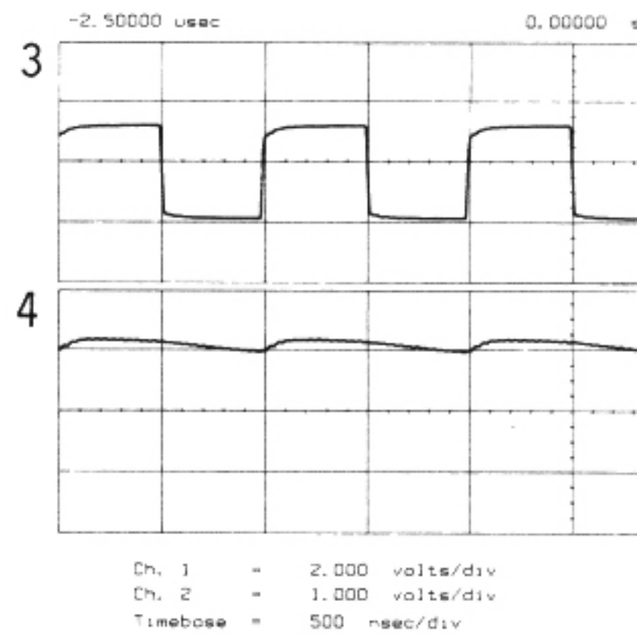
1. Ground TP5 and terminate PLAC into 50

2. Press PRESET.

3 BOARD : AD4

4

TEST POINT : TP10 for Ch. 1
SCOPE SETTING [DEFAULT]



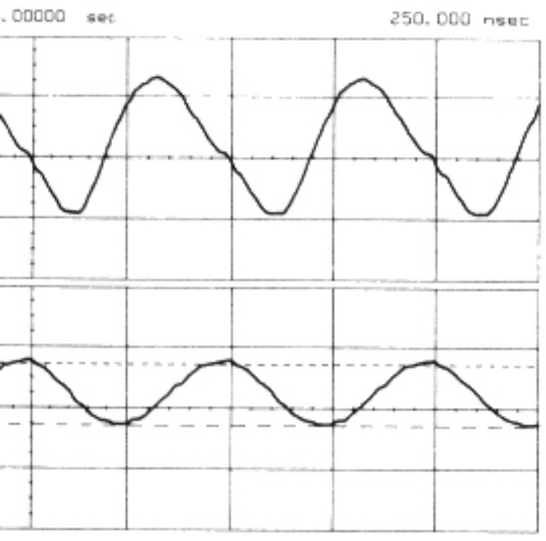
TEST POINT : TP11 for Ch. 2

PROCEDURE :

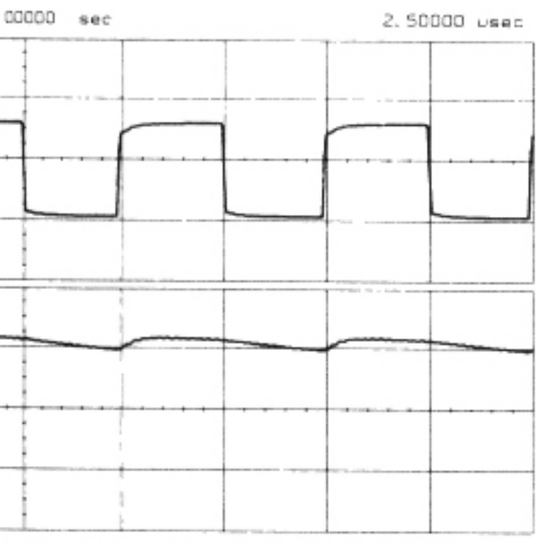
1. Press PRESET.

2. Connect signal generator to EXT STD s
   at 0 dBm.

Waveforms for AD4



to 50 Ω.

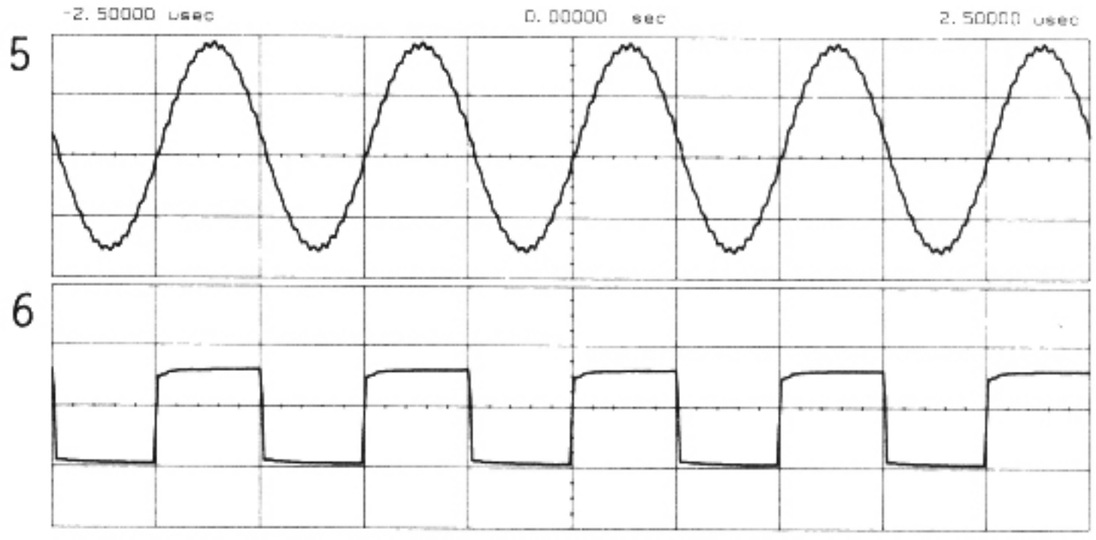


STD socket to provide 1 MHz signal

5
6

BOARD : AD4

TEST POINT : PLAA6 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP10 for Ch. 2

PROCEDURE :

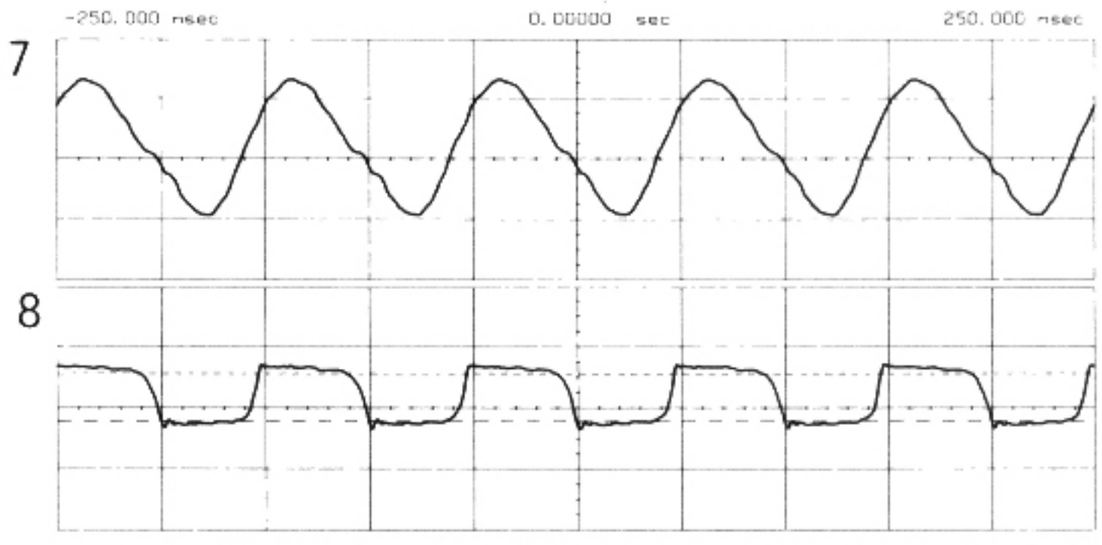
1. Press PRESET.

2. Connect signal generator to EXT STD socket to provide 1 MHz signal at 0 dBm.

7
8

BOARD : AD4

TEST POINT : R15 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP8 for Ch. 2

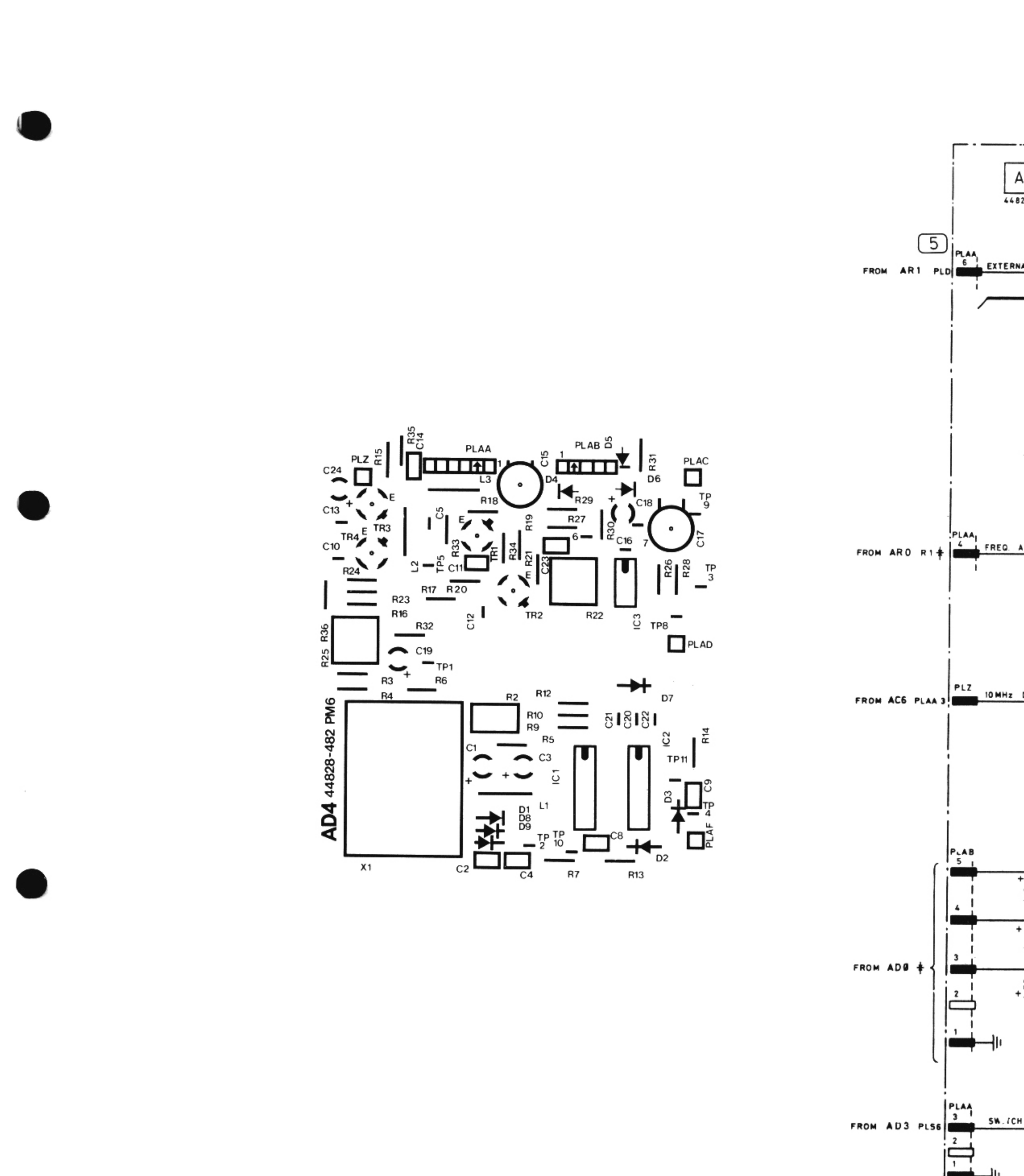
PROCEDURE :

1. Press PRESET.

2. Connect a 50 Ω load to the STD 10 MHz OUTPUT.

Fig. 39a

May 86



Component layout for AD4

Fig. 39

May 86

AD4

44828-482Y

5

FROM AR1 PLD — PLAA 6 — EXTERNAL STANDARD (1,2,5 OR 10MHz @ −15dBm TO +15dBm)

C5 10n

EXTERNAL STAN

10MHz STANDARD

+5V

R10 51R

R12 10k

R13 2k7

TP10

6 8

12 11 9

R9 51R

IC1 75107

+15V

R5 330R

C3 33µ

R6 470R

1

+15V

STD. ADJUST

R2 500k

R3 47k

R4 47k

TP1

L1 100µ

C1 1µ0

D1 D8 D9

C2 1n5

3

TCX0

2

X1 TCX03F

5

C4 1n5

TP2

R7 10k

1 2 4 5

D1, D8, D9 = BB405B

FROM AR0 R1 — PLAA 4 — FREQ. ADJUST

SQUAREWAV

+5V

C10 10n

R16 100R

C11 1n5

FROM AC6 PLAA 3 — PLZ — 10MHz DRIVE (800mV p-p SINE)

TR1 BFY90

R33 47R

R18 4R7

R19 4R7

R21 2k0

SQUARE LEVEL

−15V

PLAB 5 — +15V — C18 3·3µ

4 — +5V — C24 1µ0

FROM AD0 — 3 — R32 750R — −5V — C19 33µ — D7 BZY88C5V1

2

1 — −15V

SINEWAVE

+5V

C13 10n

1 7

R35 47R

TR3 BFY90

R15 51R

R24 1k5

SINE LEVEL

−15V

SUPPLY LINE TABLE				
IC	+5V	GROUND	−5V	DECOUPLING
IC1	14	7	13	C20, C21 (10n)
IC2	14	7	–	C22 (10n)

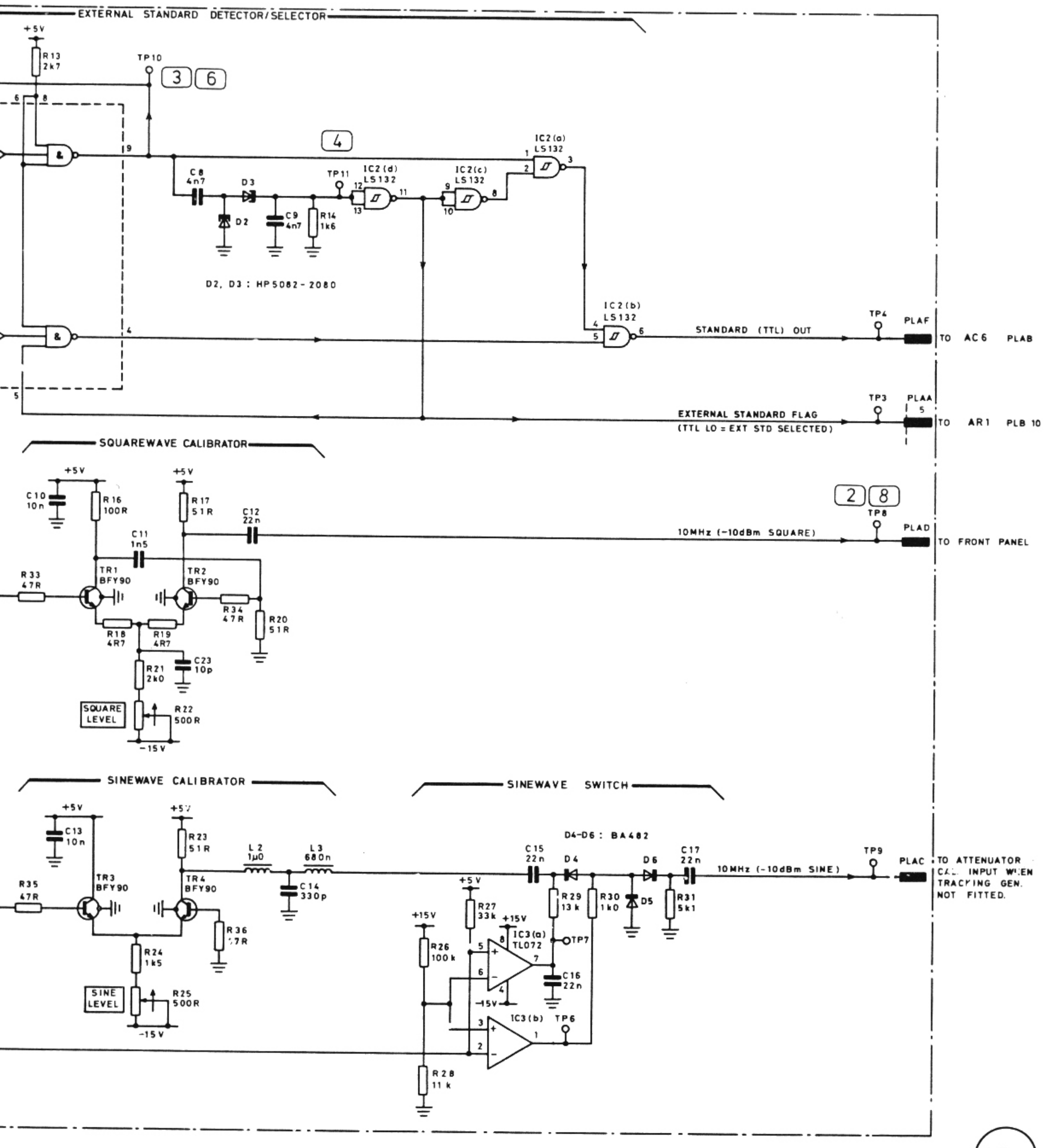
FROM AD3 PLS6 — PLAA 3 — SWITCH CONTROL (TTL, HI OFF) — TP5

2

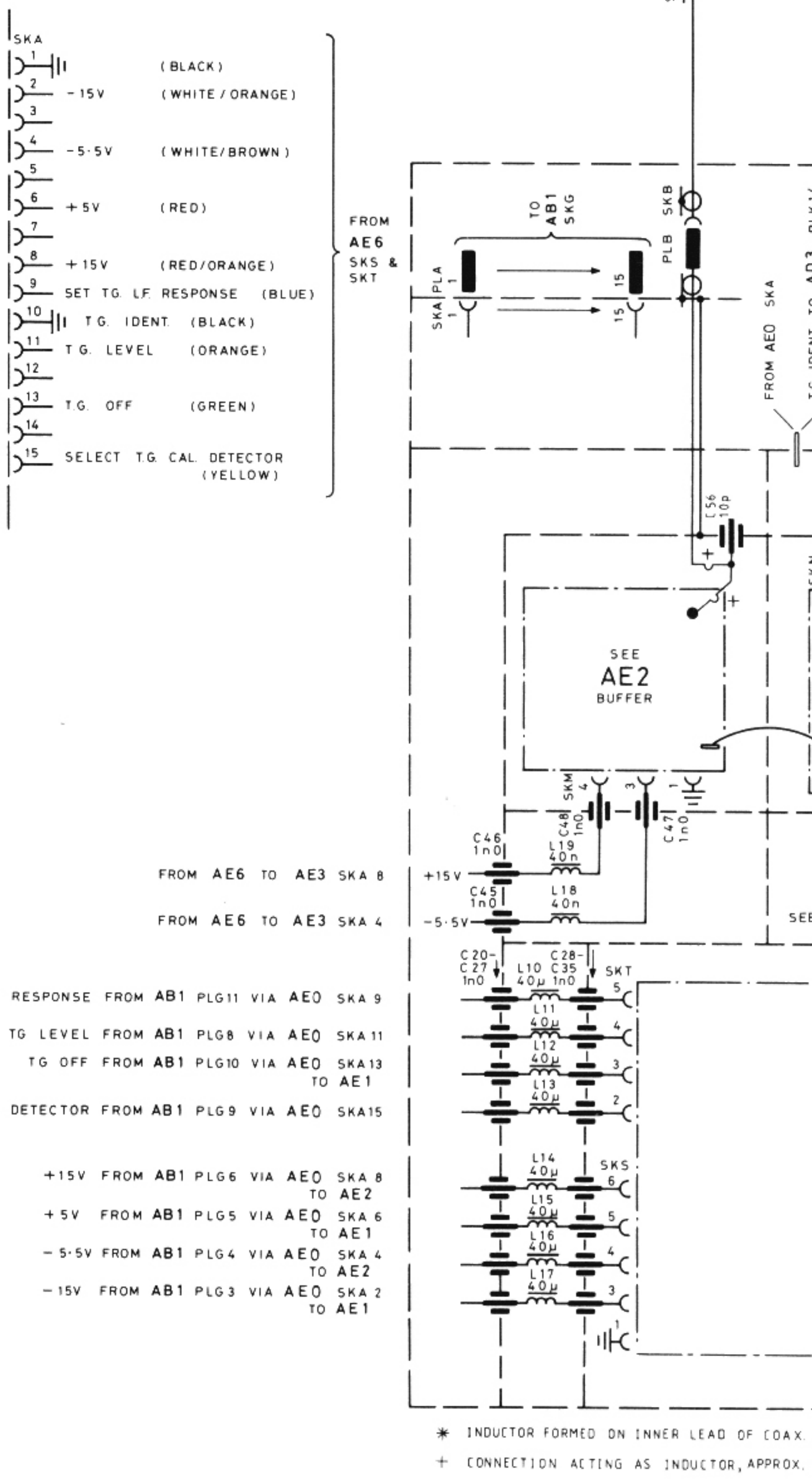
1

Drg.No. Z44828-482Y
Sh.1 Iss.1

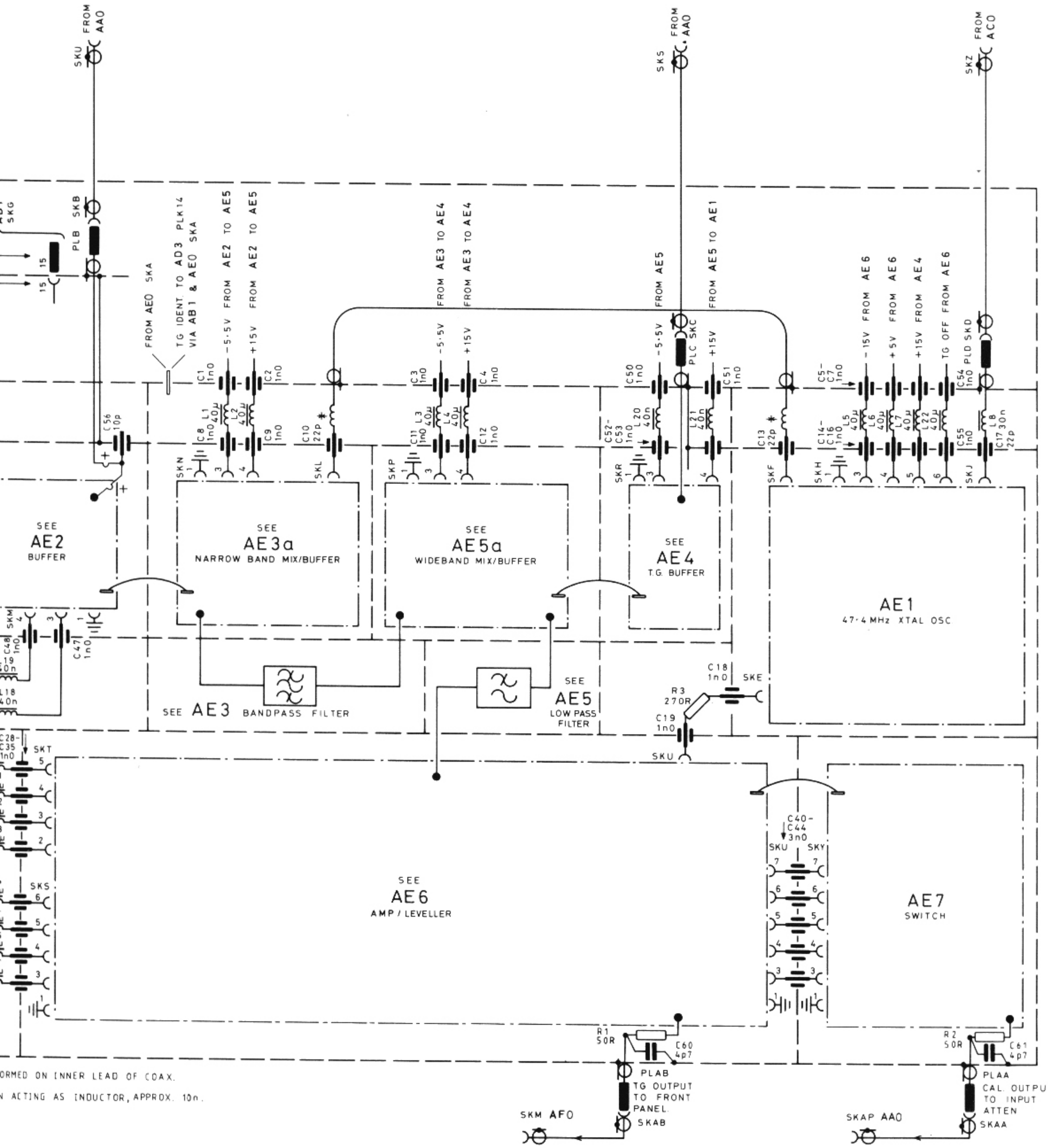
AD4: 10MHz ca



AD4 : 10MHz calibrator



Drg. No. Z44990-452
Sh. 1 Iss. 3



AE0 : AE tray interconnection

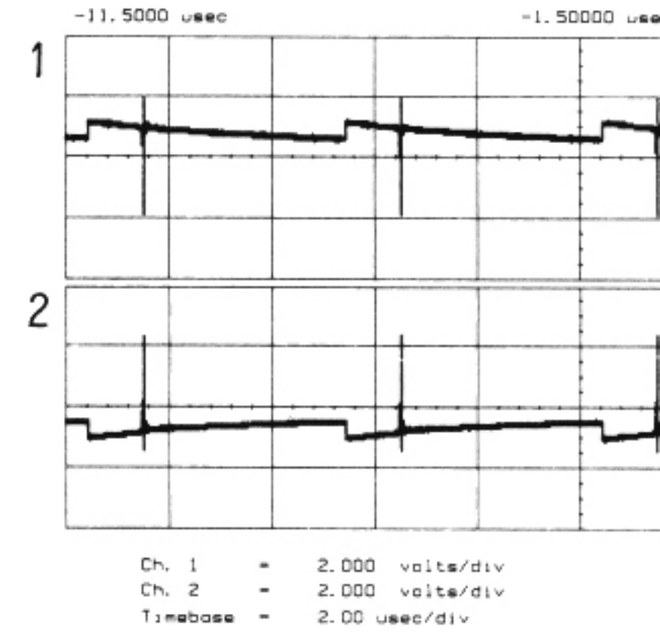
Fig. 40
Chap. 7
Page 89

Fig. 41a
Chap. 7
Page 90

1
2

BOARD : AE1

TEST POINT : R20 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : R21 for Ch. 2

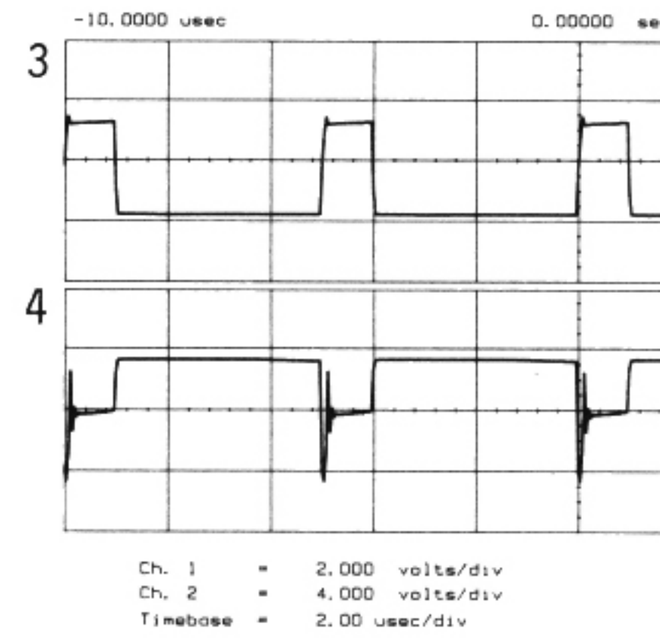
PROCEDURE :

1. Press PRESET.

3
4

BOARD : AE1

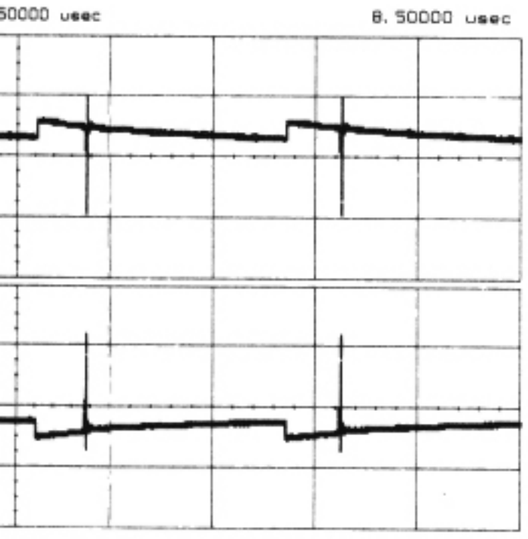
TEST POINT : TP3 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP2 for Ch. 2

PROCEDURE :

1. Press PRESET.

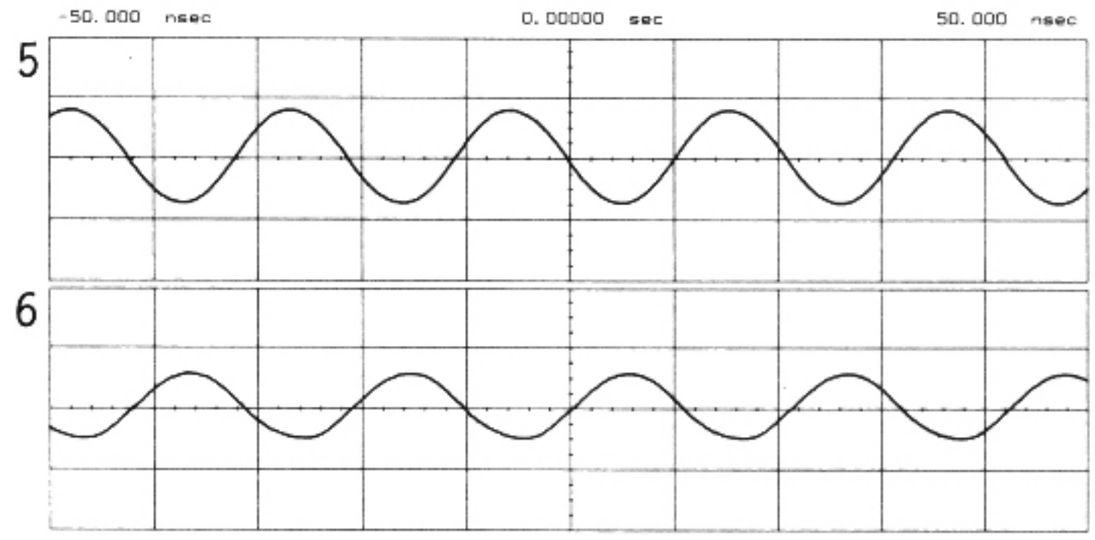


Offset = 0.000 volts
Offset = 0.000 volts
Delay = -1.50000 usec

5
6

BOARD : AE1

TEST POINT : TP1 for Ch. 1
SCOPE SETTING [DEFAULT]



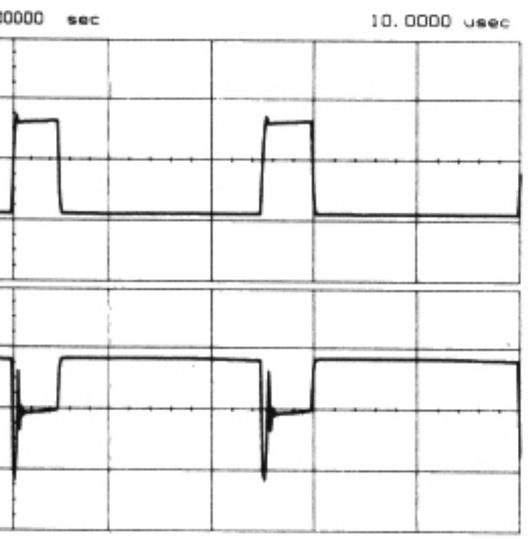
Ch. 1 = 1.000 volts/div
Ch. 2 = 200.0 mvolts/div
Timebase = 10.0 nsec/div

Offset = 0.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

TEST POINT : TP9 for Ch. 2

PROCEDURE :

1. Press PRESET then switch [TRACK GEN] on.

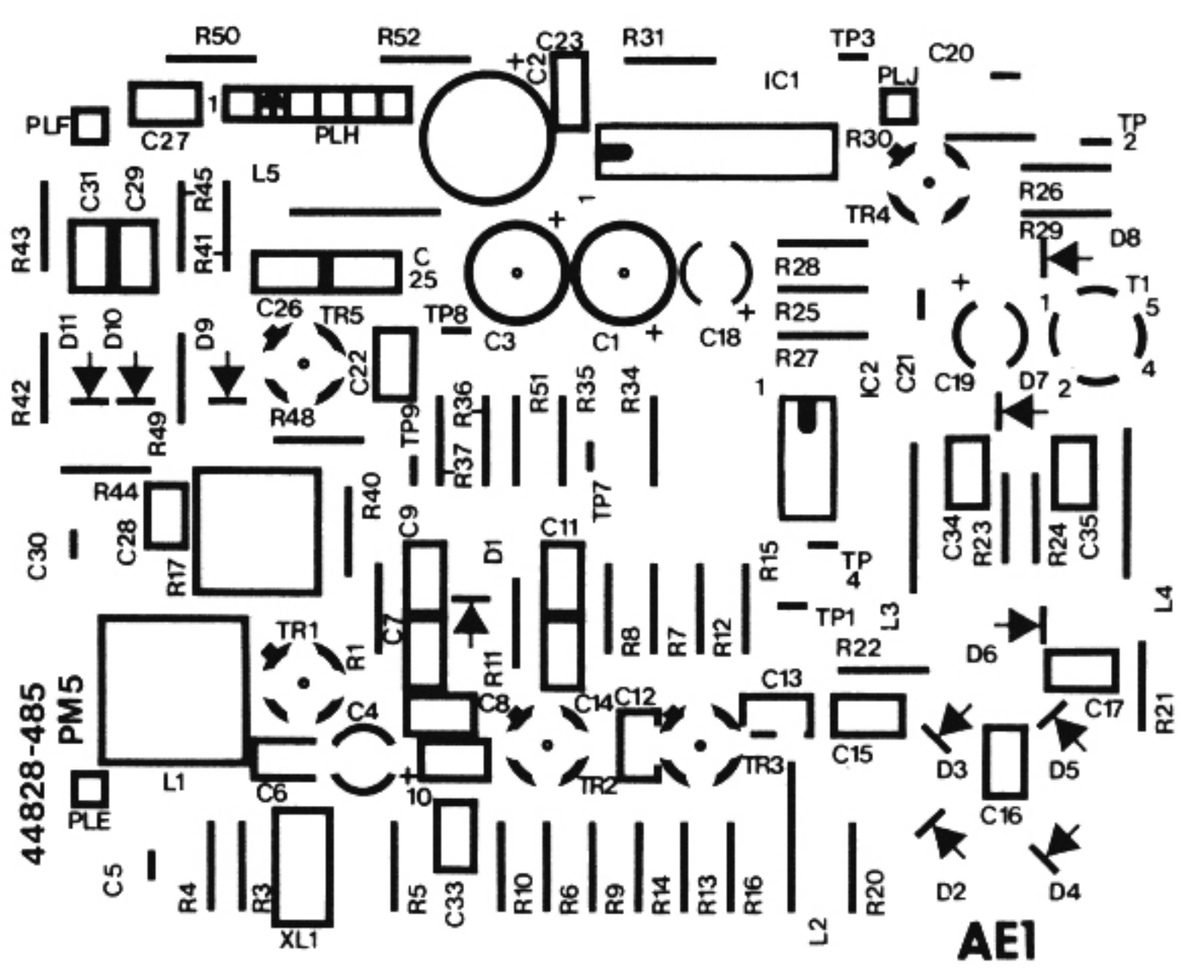


Offset = 2.000 volts
Offset = 12.00 volts
Delay = 0.00000 sec

Waveforms for AE1

Fig. 41a

May 86



Component layout for AE1

Fig. 41

May 86

AE1
44828-485J

GAIN CONTROLLED AMP.

FROM AE0 ✦

PLH
5 — +15V
4 — R52 4R7 — +5Vd
3 — −15V
2
1

C1 33µ
C2 470µ
C3 33µ

+5Vd
L5 100n
C25 470p
C26 100p
R17 5k0
6 TP9
TR5 BFY90
R48 51R
SET WKG. LEVEL
R40 120R
R41 1k0
−15V
C29 4n7
R45 24k
−15V
C31 4n7
R43 10k
−15V

47·4MHz VOLTAGE CONTROLLED XTAL OSC.

ISOLATING AMP. — SAMPL

FROM AE0 ✦

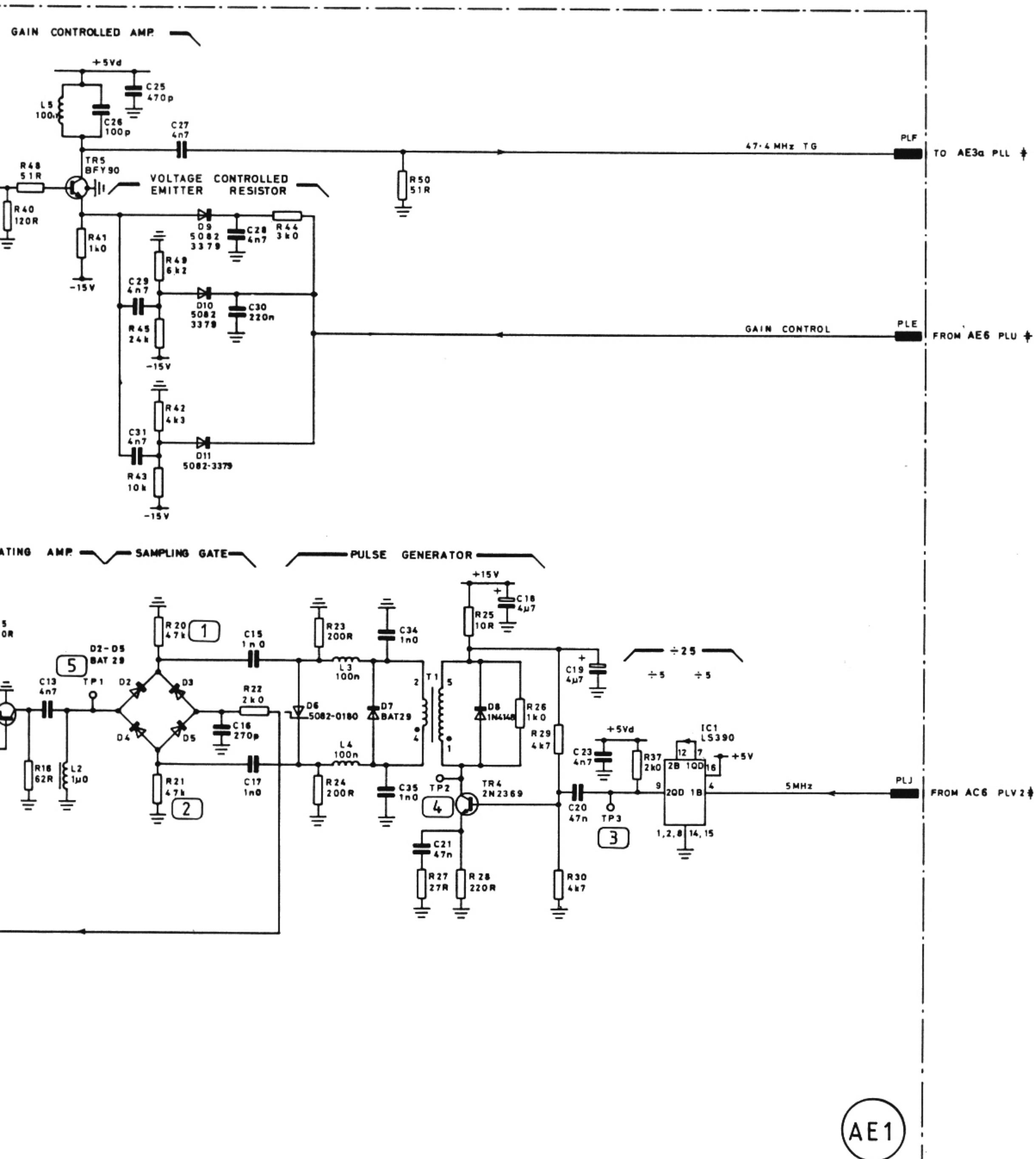
PLH 6 — TG OFF (L) — R1 1k0

+15V
C5 47n
L1
FINE TUNE
TR1 BFY90
47·4MHz
XL1
R5 82R
C4 33µ
R3 1k2
C6 4n7
R4 100R
C7 47p
C8 68p
C9 100p
D1 BB405
C10 15p
R37 10k
R51 10k
C33 4n7
−15V
TP8
R7 2k0
R9 3k9
R8 100R
C14 4n7
R6 100R
TR2 BFY90
R10 470R
R11 56R
C11 4n7
C12 4n7
R13 4k7
R12 4k7
R15 330R
R14 39R
TR3 BFR99
C13 4n7
R16 62R
L2 1µ0
5 TP1
D2-D5 BAT 29
D2
D4
TP4
IC2 741
TP7
R36 10k
C22 4n7
R35 68k
R34 2k2

✦ SEE CIRCUIT AE0 FOR CONNEC

Drg.No. Z44828-485J
Sh.1 Iss.1

AE1 : 47.4MHz cry

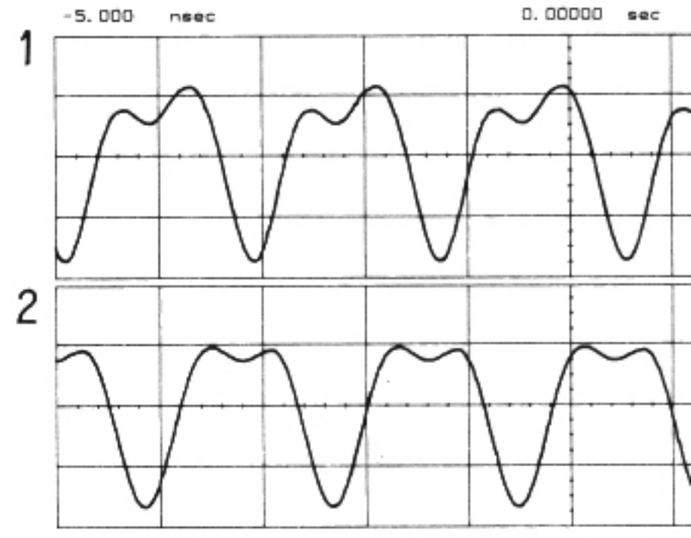


1 : 47.4MHz crystal oscillator

1
2

BOARD : AE2

TEST POINT : R13 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : R10 for Ch. 2

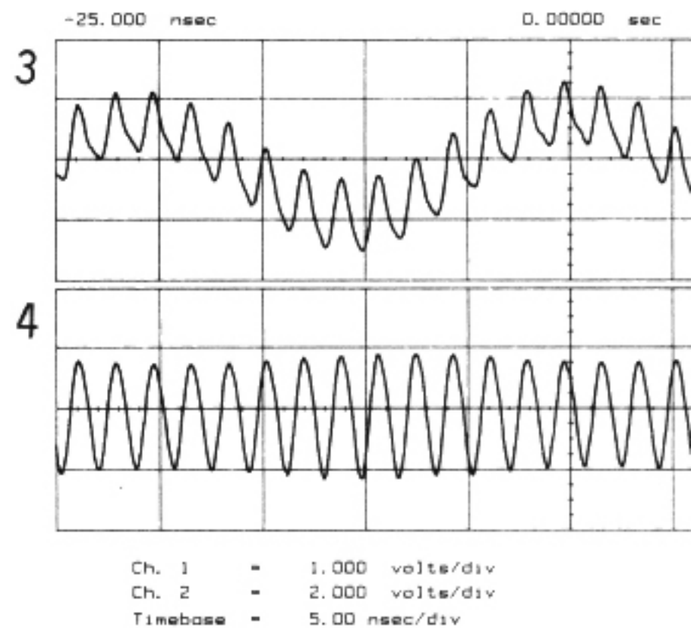
PROCEDURE :

1. Press PRESET.

3
4

BOARD : AE3a

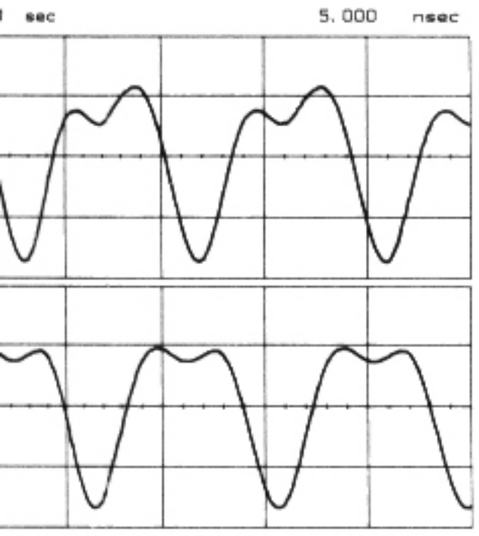
TEST POINT : TR3 G1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TR3 G2

PROCEDURE :

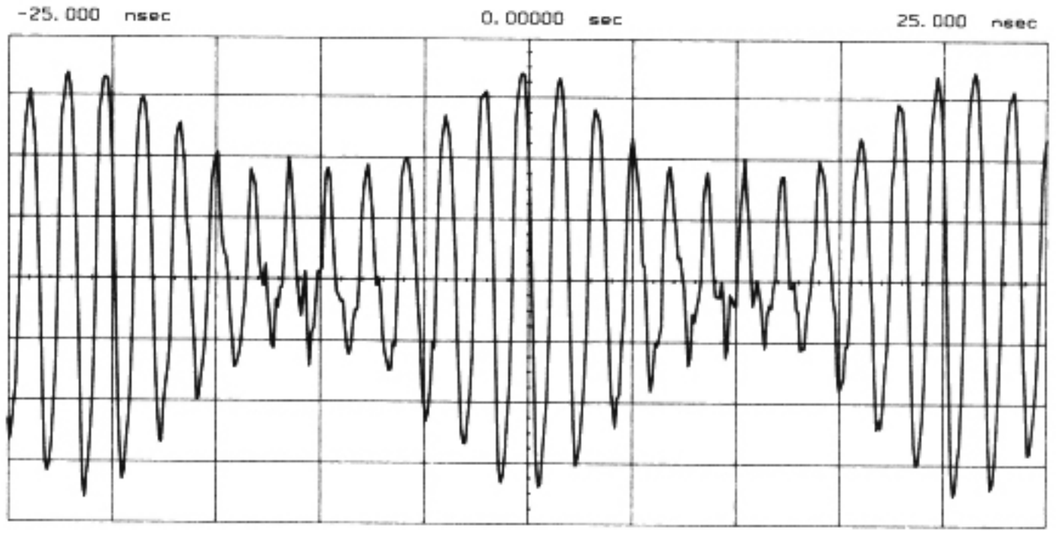
1. Press PRESET.



Offset = 0.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

5 BOARD : AE3

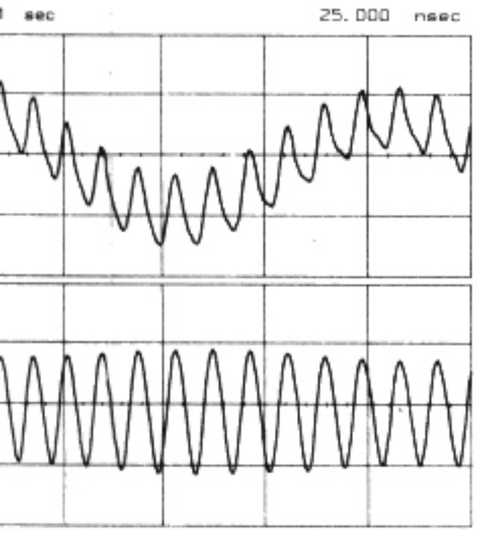
TEST POINT : TP1 for Ch. 2
SCOPE SETTING [DEFAULT]



Ch. 1 = 100.0 mvolts/div
Timebase = 5.00 nsec/div
Offset = 0.000 volts
Delay = 0.00000 sec

PROCEDURE :

1. Press PRESET then turn [TRACK GEN] on.



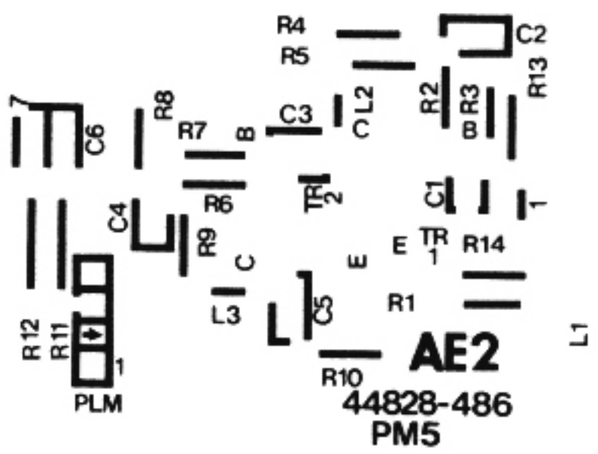
Offset = 1.500 volts
Offset = 1.500 volts
Delay = 0.00000 sec

Waveforms for AE2, AE3 & AE3a

Fig. 42a

May 86

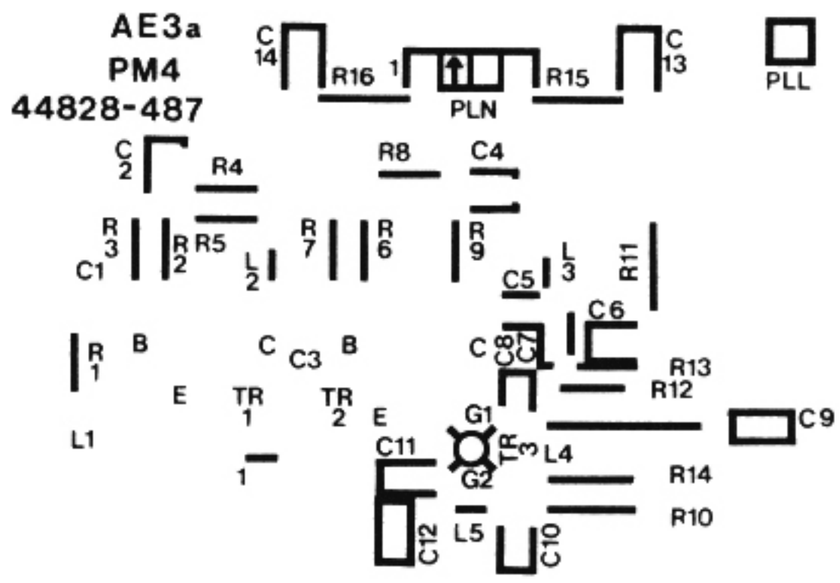
FROM AE0



FROM AE1

Component layout for AE2

FROM AE0



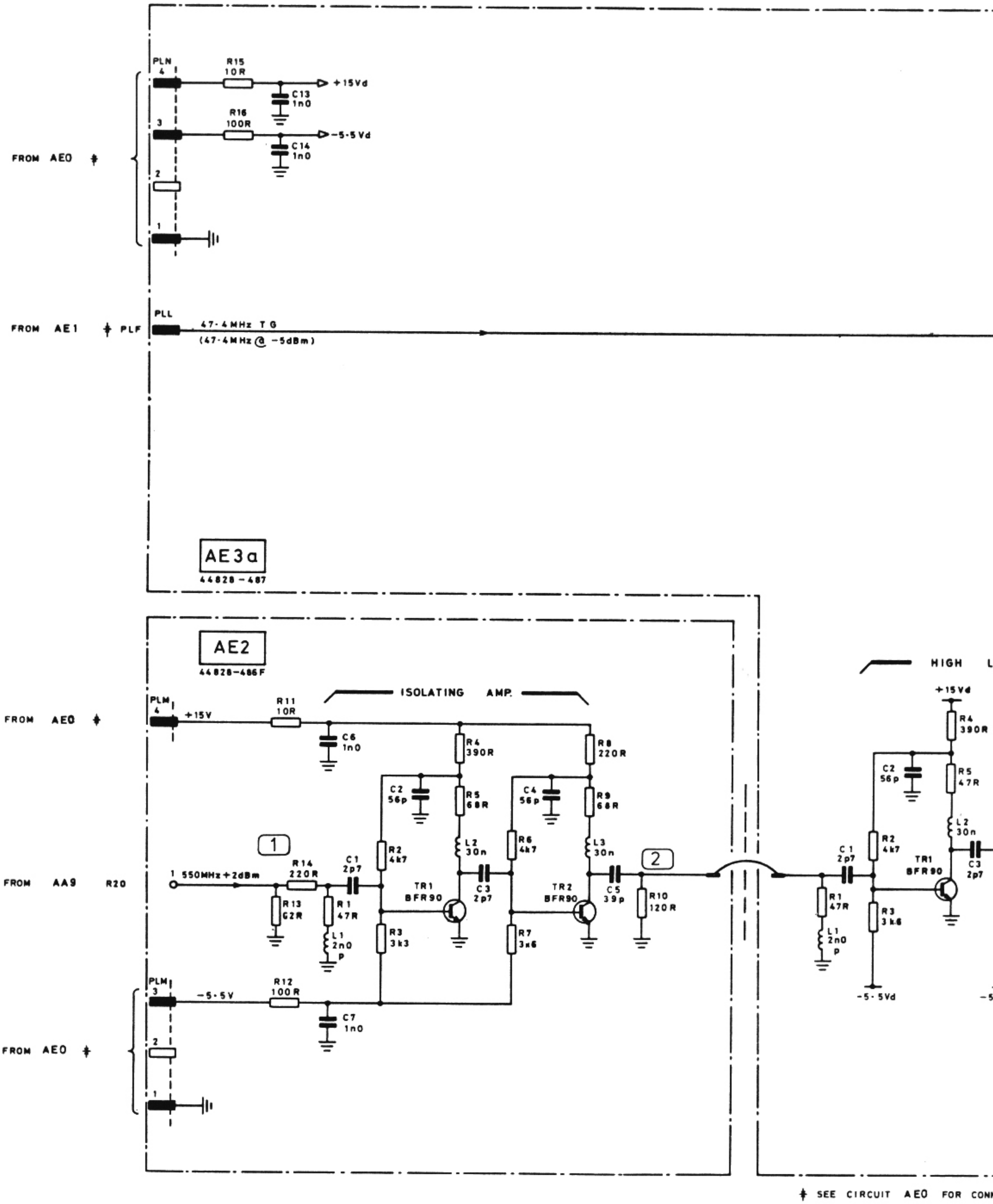
FROM AA9

FROM AE0

Component layout for AE3a

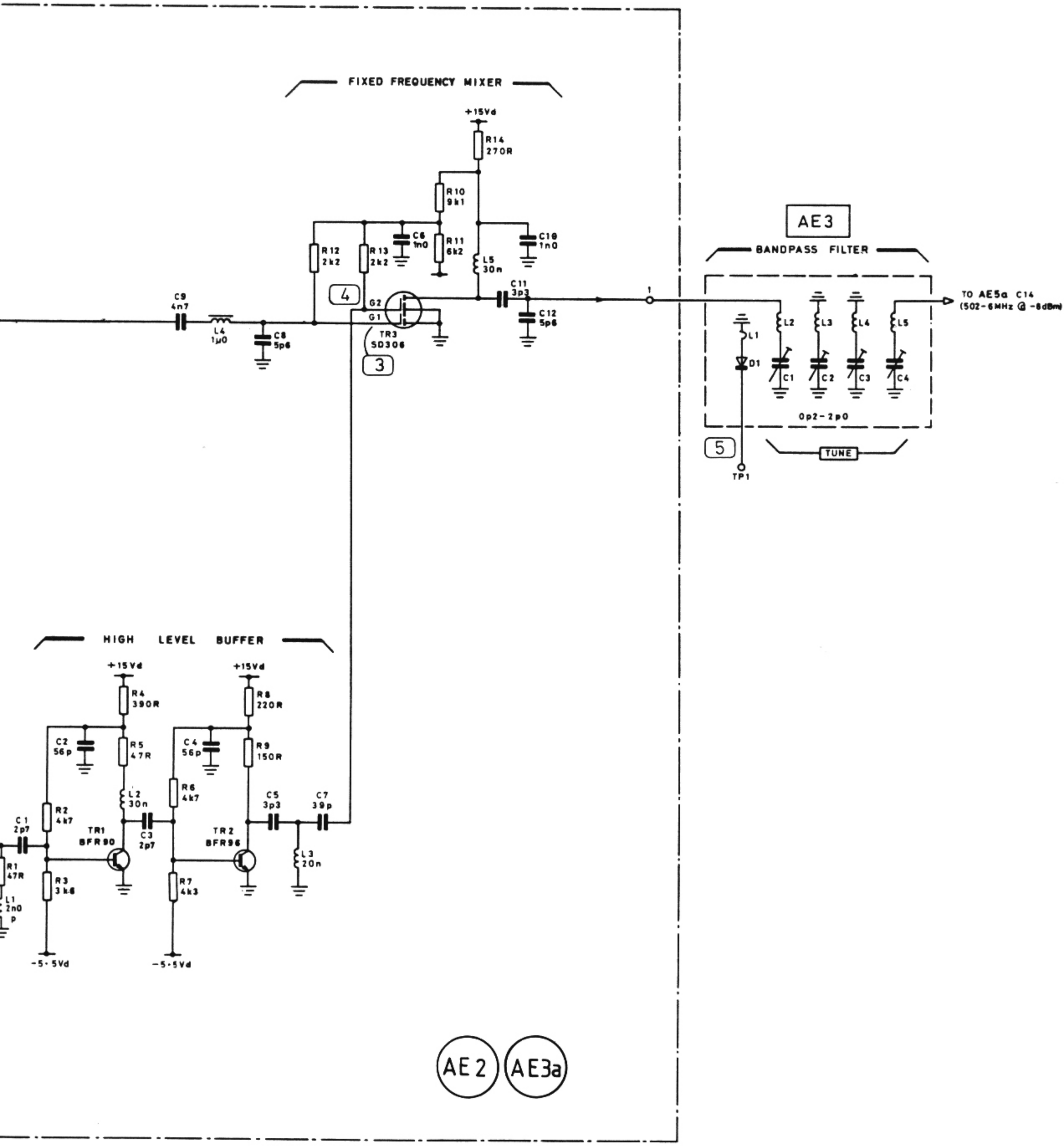
Fig. 42

May 86



Drg.No. Z44990-452
Sh.2 Iss.1

AE2: Buffer
AE3a: Narrow band



SEE CIRCUIT AE0 FOR CONNECTION DETAILS.

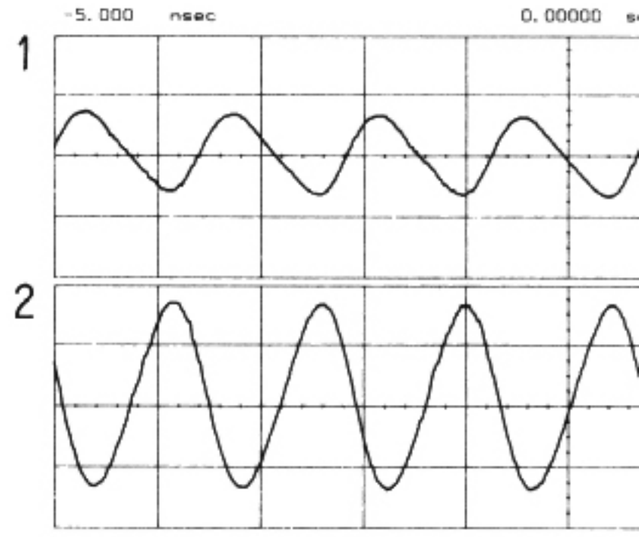
Buffer
:Narrow band mixer/buffer

Fig. 42
Chap. 7
Page 93

1 BOARD : AE4

2

TEST POINT : R1
SCOPE SETTING [DEFAULT]



TEST POINT : R10

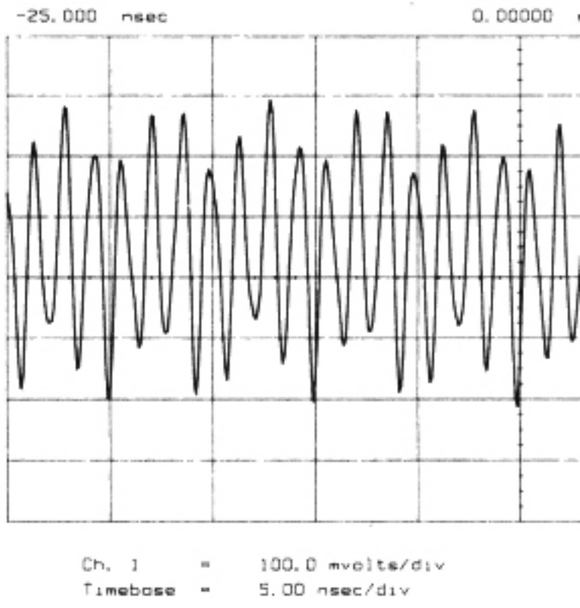
PROCEDURE :

1. Press PRESET then select the followin

Zero span

3 BOARD : AE5a

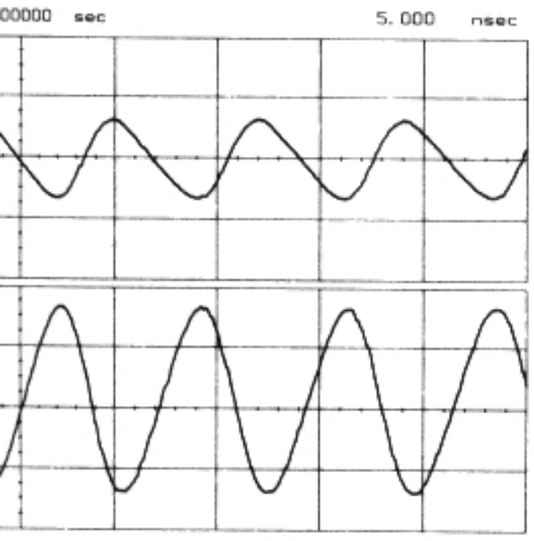
TEST POINT : tag 2 (XM1 pin 3)
SCOPE SETTING [DEFAULT]



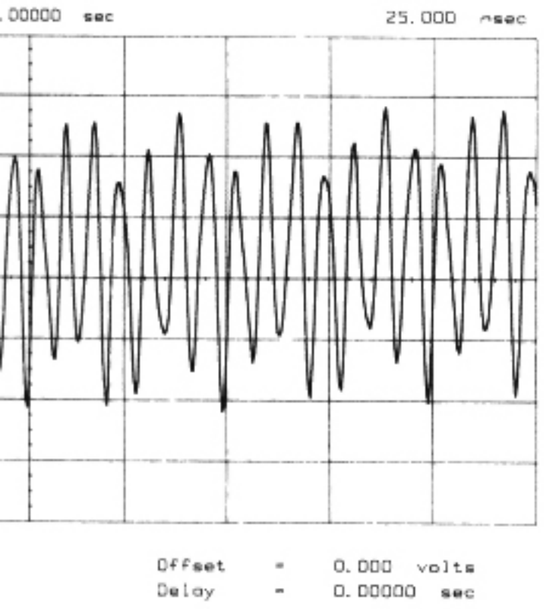
PROCEDURE :

1. Press PRESET then select the followin

Zero span
Track gen. on



lowing 2382 setting:

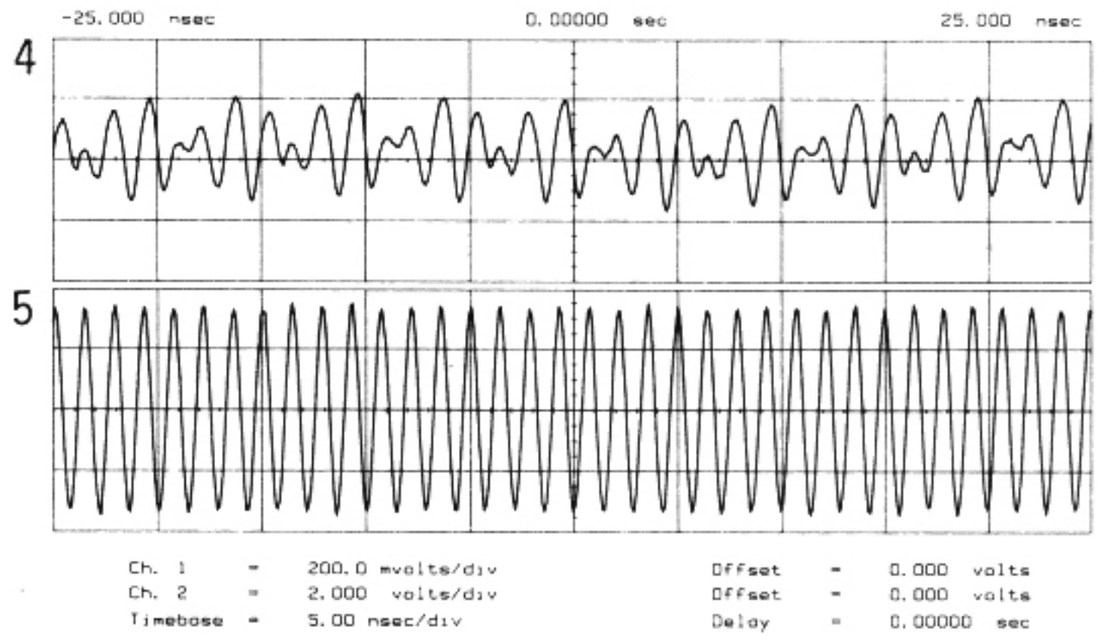


lowing 2382 settings:

4
5

BOARD : AE5a

TEST POINT : XM1 pin 1 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : XM1 pin 8 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Zero span
   Track gen. on

Waveforms for AE4 & AE5a

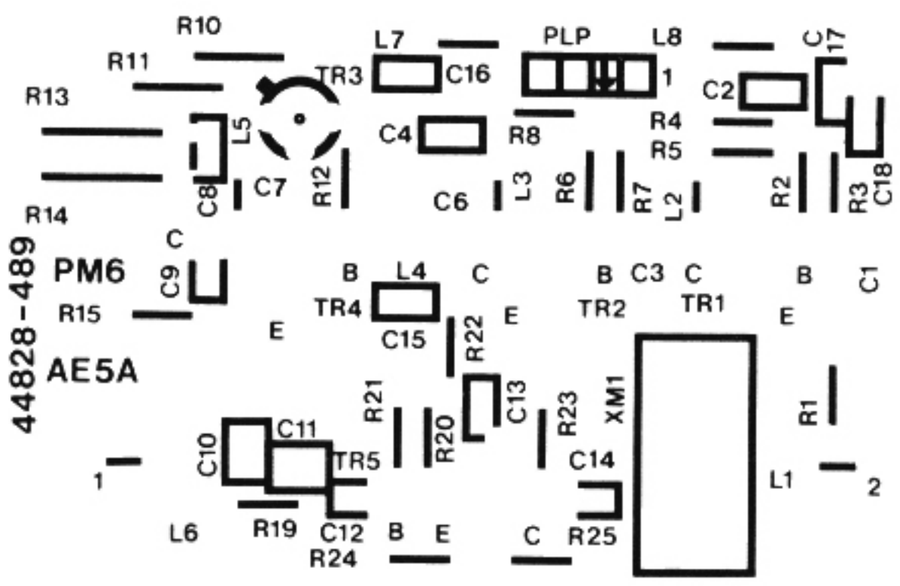
Fig. 43a

May 86

FROM AE0

FROM AE3 L6

Component layout for AE4



FROM AE0

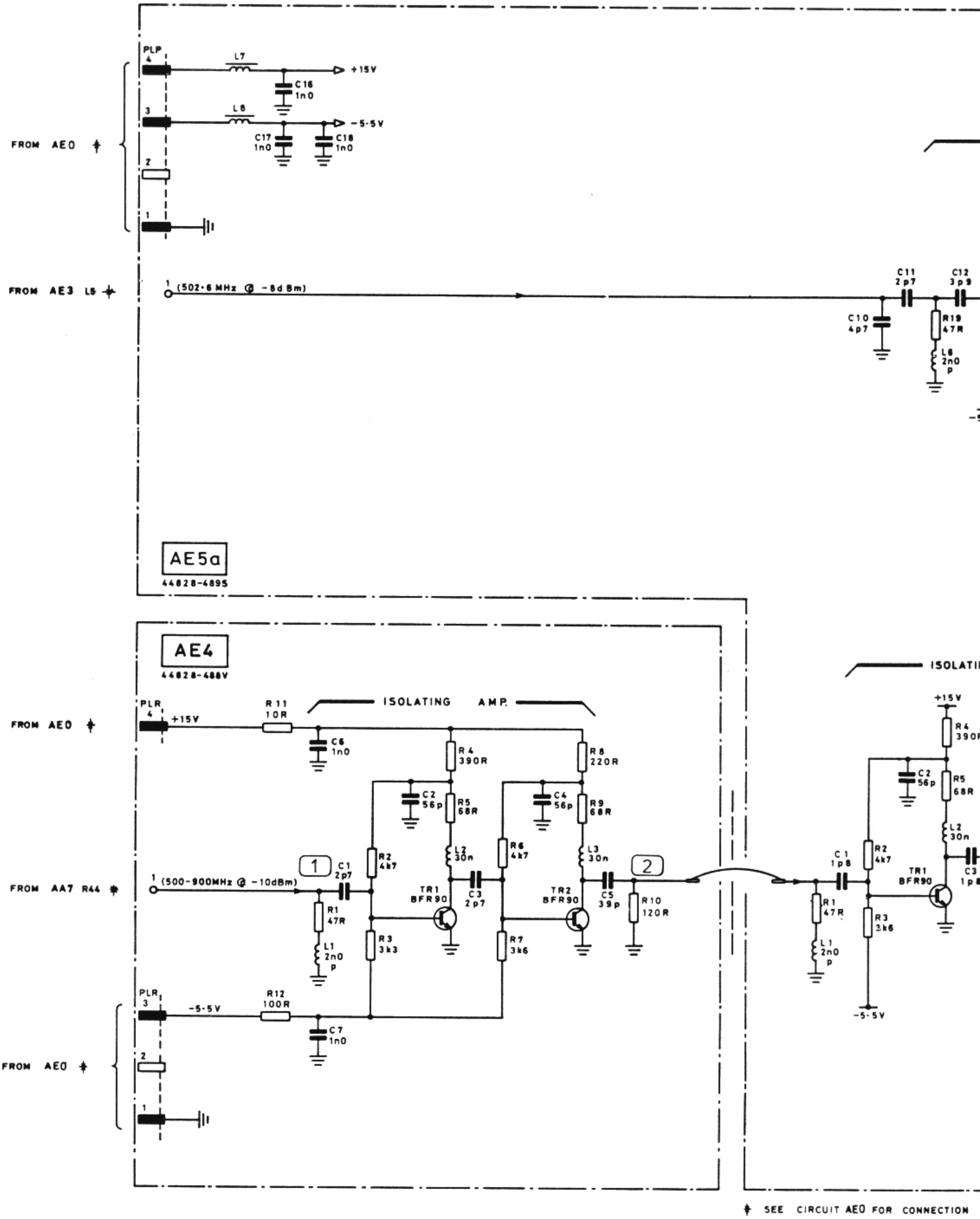
FROM AA7 R44

Component layout for AE5a

FROM AE0

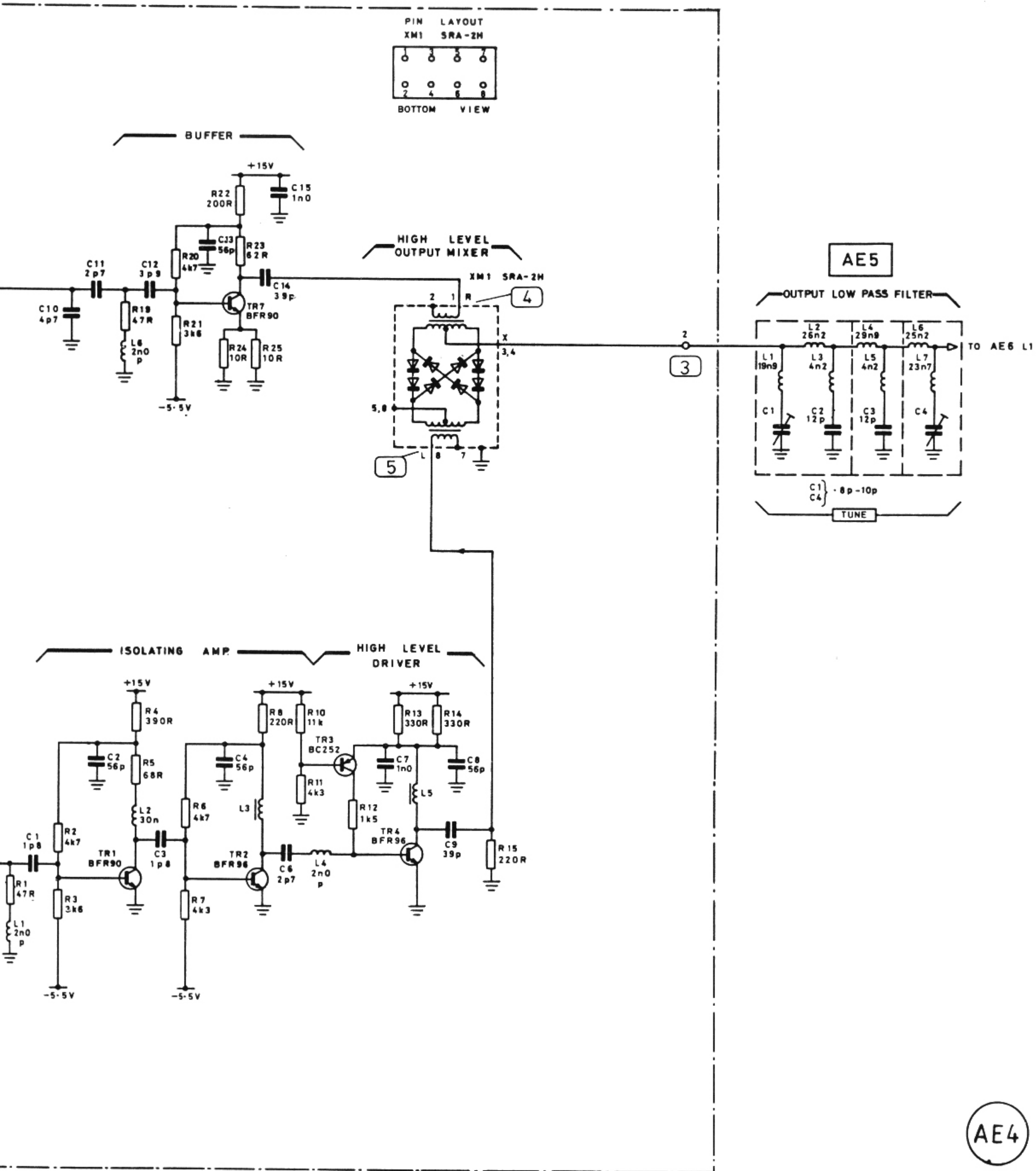
Fig. 43

May 86



Drg.No. Z44990-452
Sh.3 Iss.1

AE4 : TG buffer
AE5a : Wide band



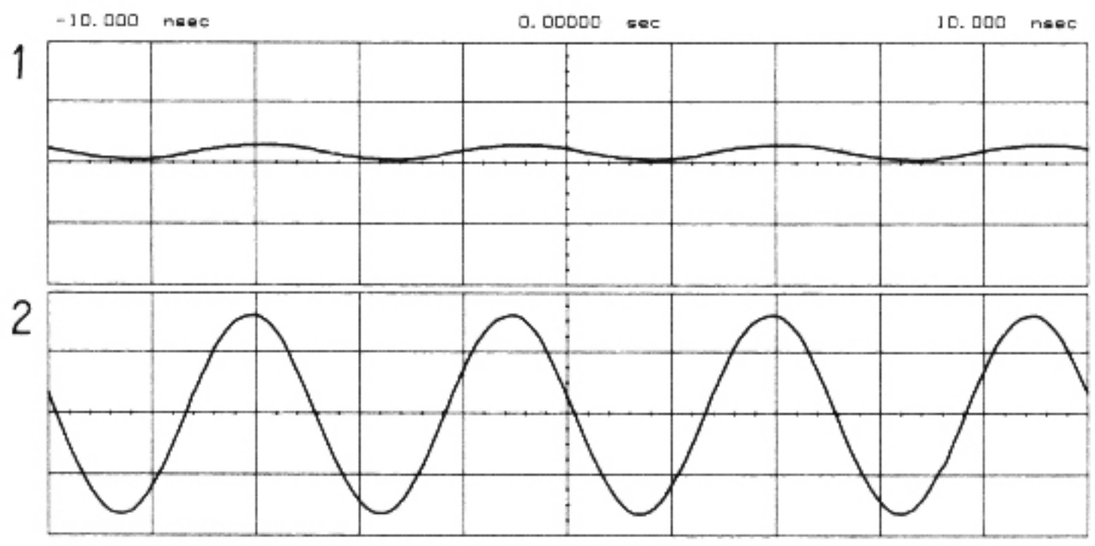
...RCUIT AE0 FOR CONNECTION DETAILS.

4 : TG buffer
5a : Wide band mixer/buffer

AE4
AE5a

1
2 BOARD : AE6 *(Fig. 44 refers)*

TEST POINT : tag 1 for Ch. 1
SCOPE SETTING [DEFAULT]



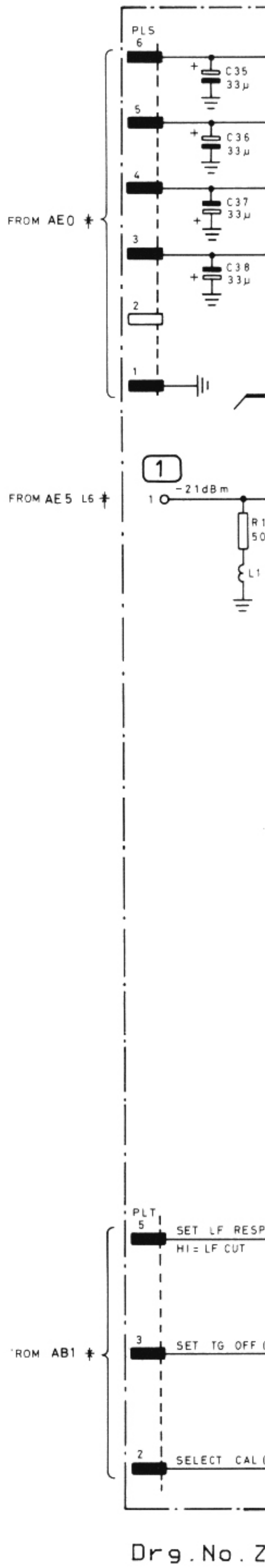
Ch. 1	-	200.0 mvolts/div	Offset	-	0.000 volts
Ch. 2	-	200.0 mvolts/div	Offset	-	0.000 volts
Timebase	-	2.00 nsec/div	Delay	-	0.00000 sec

TEST POINT : junction D17/D19 for Ch. 2

PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Zero span
   Track gen. on



Waveforms for AE6

Fig. 44

May 86

Drg. No. Z
Sh. 4 I

PART OF
AE6
44828-490G

FROM AE0 ✱

PLS
6 → +15V
C35 33µ
5 → +5V
C36 33µ
R86 27k
4 → −5·5V
C37 33µ
Vb
R87 12k
3 → −15V
C38 33µ
2
1

21dB AMPLIFIER

LF ROLL-OFF SELECT

FROM AE5 L6 ✱

1 → −21dBm
C1 22n
C2 100µ
R1 50R
L1
TR4 VN10KM
R2 1k0
+5V
R120 9k1
R32 10k
R119 91k
−5·5V

R11 10R
D33 BZX79C 6V2
+15V
C15 220µ
R16 68R
C16 22n
R23 160R
C17 1µ0
R8 68R
D31 BZX79C 5V6
D32 BZX79C 4V7
C11 220µ
R6 56R
R13 22R
R19 22R
TR1 BFR90
TR2 BFR90
TR3 BFR96
R24 43k
C44 1µ0
R9 12R
C5 10p
R10 24R
R12 2k2
R14 4R7
R17 20R
R20 2k0
R21 39R
R22 20R
R25 75k
R90 2k2
R89 4k7
C4 12p
C8 3p5 13p
R122 5k0
C10 18p
−15V
C18 1µ0

D.C. STABILISATION

C13 22n
+15V
R5 1k0
IC1 TL071
R31 1M0
R4 62R
R30 1M0
R7 39R
C19 470µ
−5·5V

Vb
IC5(a) LM348
−15V
+15V

FROM AB1 ✱

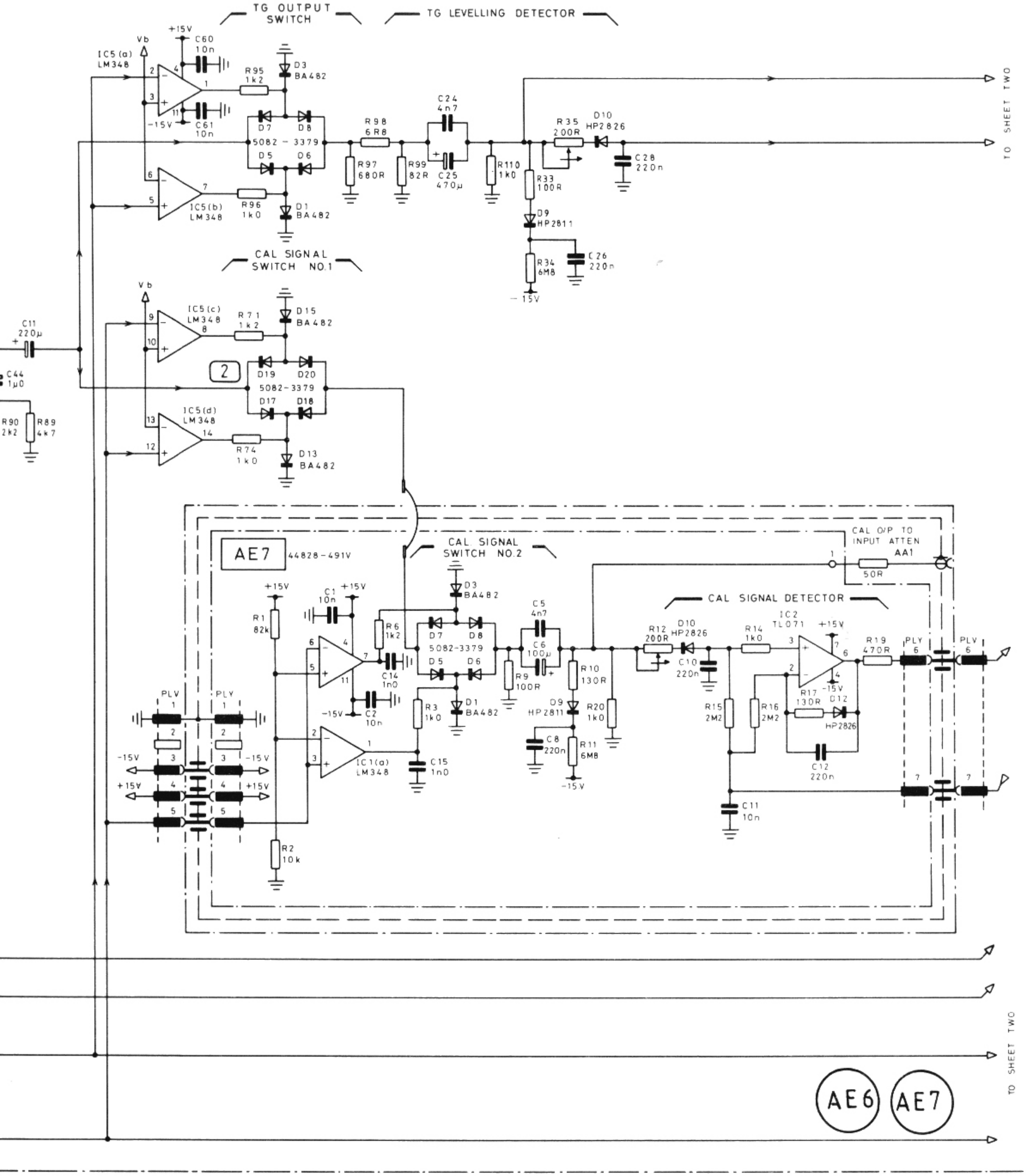
PLT
5 SET LF RESPONSE HI = LF CUT
3 SET TG OFF (L)
2 SELECT CAL (L)

+5V
R76(c) 6k8
R76(b) 6k8
R76(a) 6k8
IC12(a) LS132
IC12(c) LS132

✱ SEE CIRCUIT AE0 FOR CONNECTION DETAILS

AE6 :
AE7 :

Drg.No. Z44990-452
Sh.4 Iss.4 & 2



ECTION DETAILS

AE6 : Amp. leveller

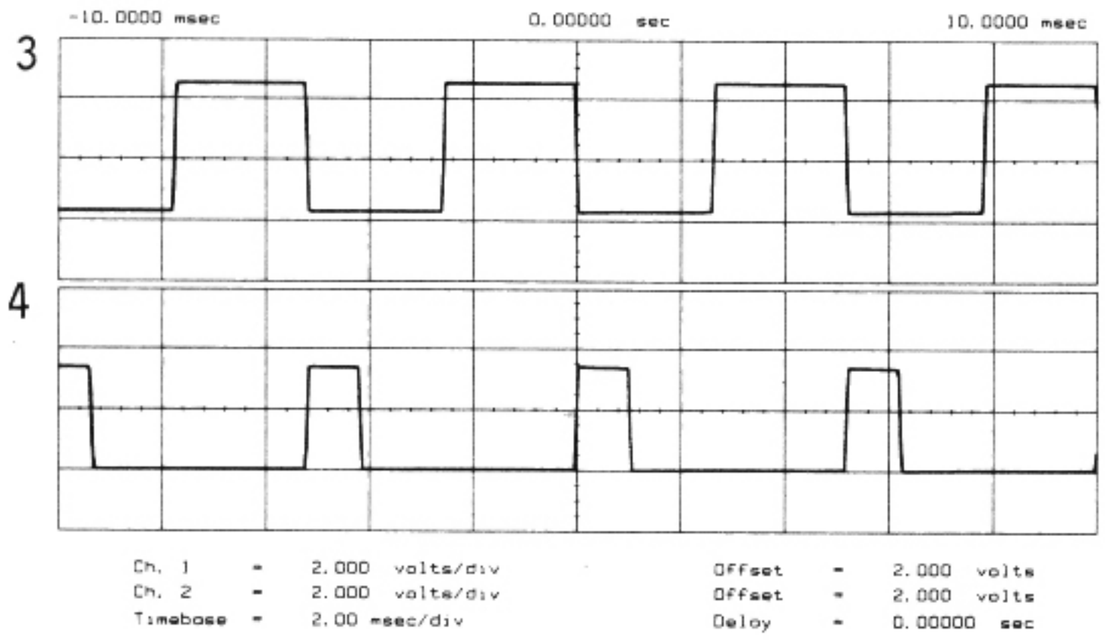
AE7 : Switch

Fig. 44
Chap. 7
Page 97

3
4

BOARD : AE6 *(Fig. 45 refers)*

TEST POINT : TP16 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP17 for Ch. 2

PROCEDURE :

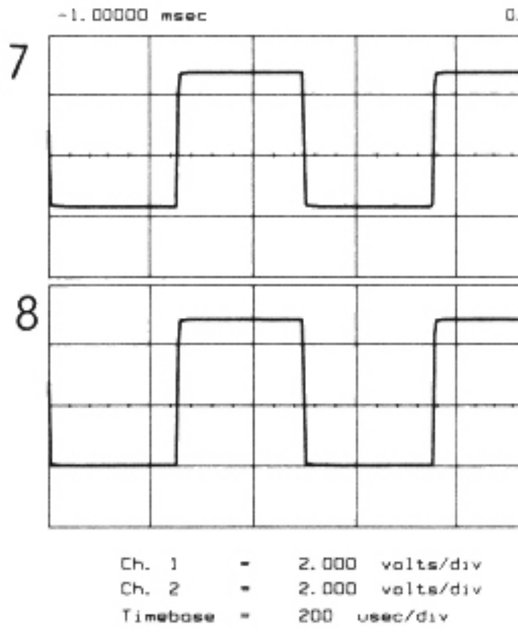
1. Press PRESET then select the following 2382 settings:

Track gen. on
Zero span
Ref. freq. 200 Hz

7
8

BOARD : AE6

TEST POINT : TP16 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC11b pin 4 for Ch. 2

PROCEDURE :

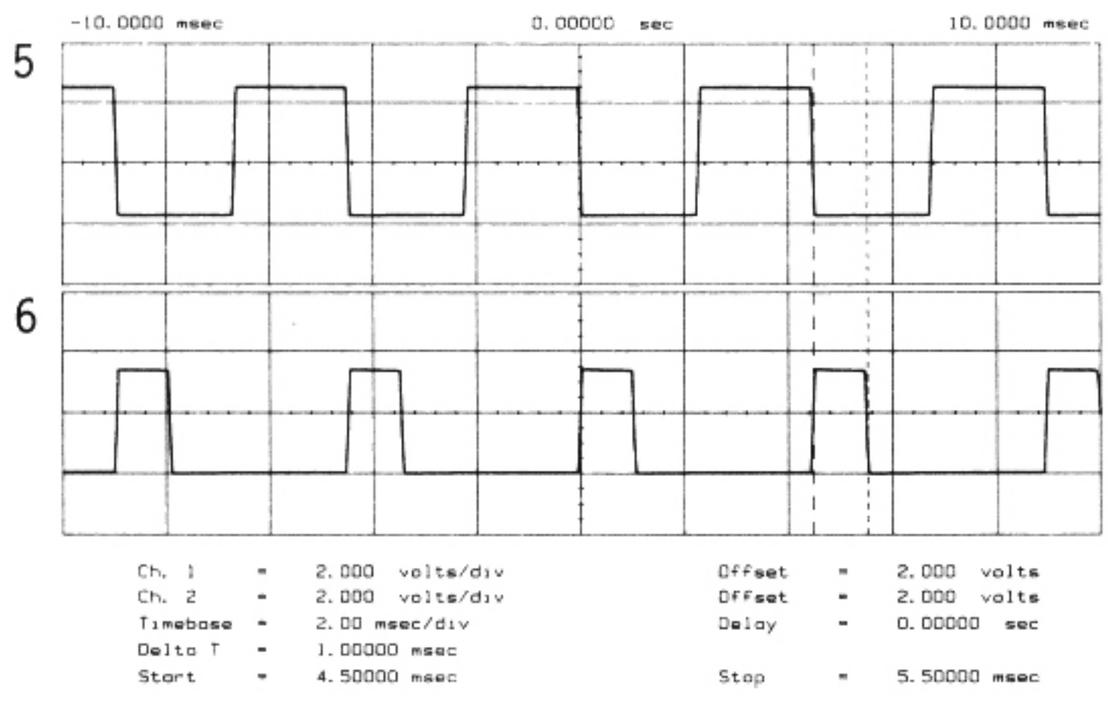
1. Press PRESET then select the

Track gen. on
Zero span
Ref. freq. 2 kHz

5
6

BOARD : AE6

TEST POINT : TP16 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : TP17 for Ch. 2

PROCEDURE :

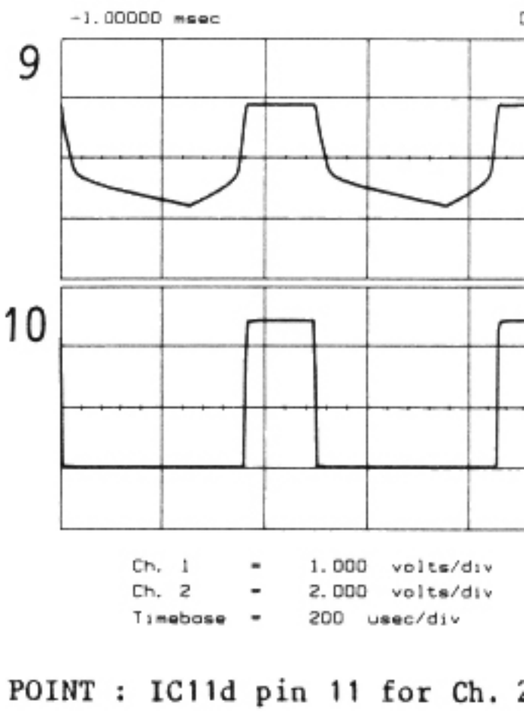
1. Press PRESET then select the following 2382 settings:

Track gen. on
Zero span
Ref. freq. 222 Hz

9
10

BOARD : AE6

TEST POINT : IC9c pin 8 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC11d pin 11 for Ch. 2

PROCEDURE :

1. Press PRESET then select the

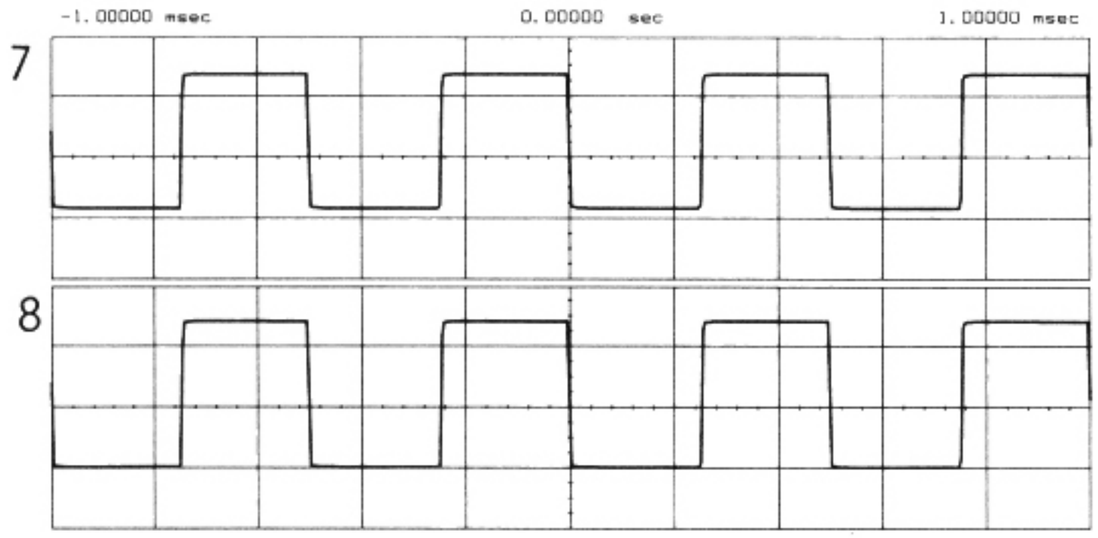
Track gen. on
Zero span
Ref. freq. 2 kHz

Fig. 45a
Chap. 7
Page 98

7
8

BOARD : AE6

TEST POINT : TP16 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC11b pin 4 for Ch. 2

PROCEDURE :

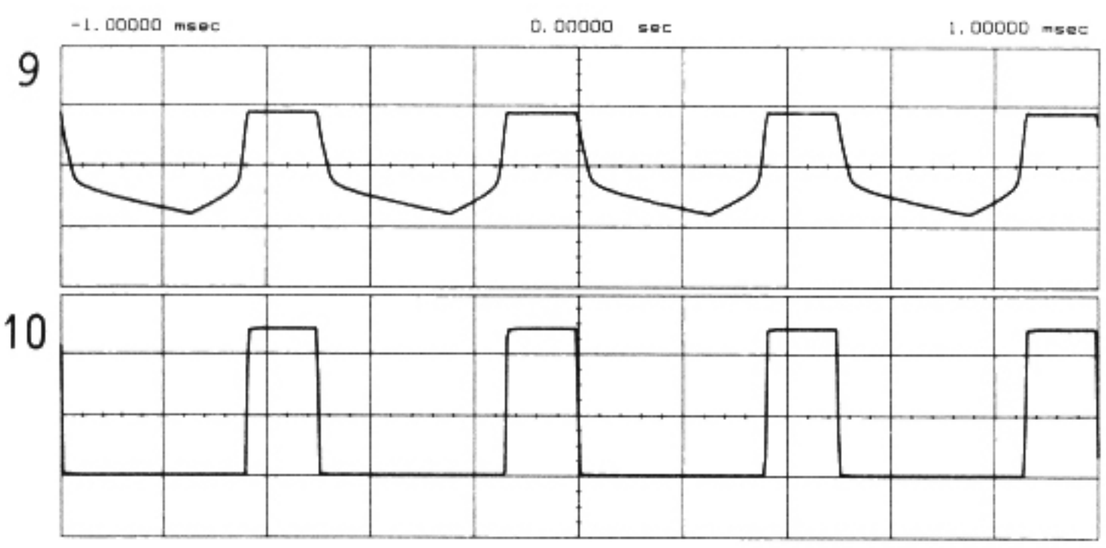
1. Press PRESET then select the following 2382 settings:

   Track gen. on
   Zero span
   Ref. freq. 2 kHz

9
10

BOARD : AE6

TEST POINT : IC9c pin 8 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : IC11d pin 11 for Ch. 2

PROCEDURE :

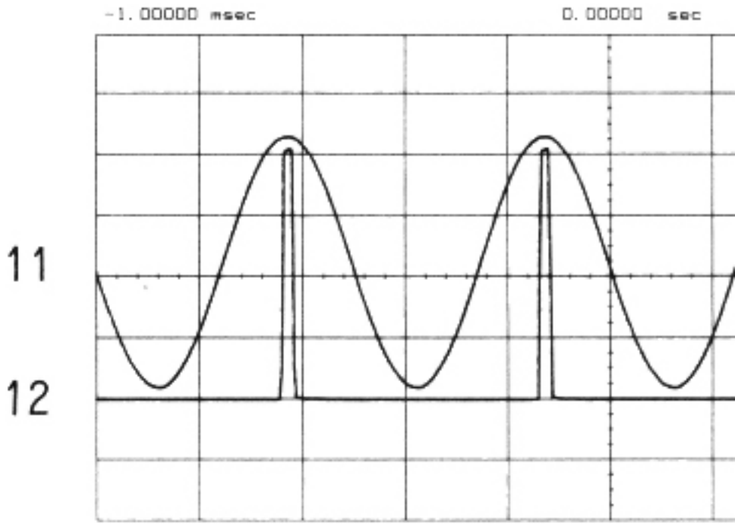
1. Press PRESET then select the following 2382 settings:

   Track gen. on
   Zero span
   Ref. freq. 2 kHz

11
12

BOARD : AE6

TEST POINT : IC7c pin 14 for Ch. 1
SCOPE SETTING [DEFAULT]



TEST POINT : tag 8

PROCEDURE :

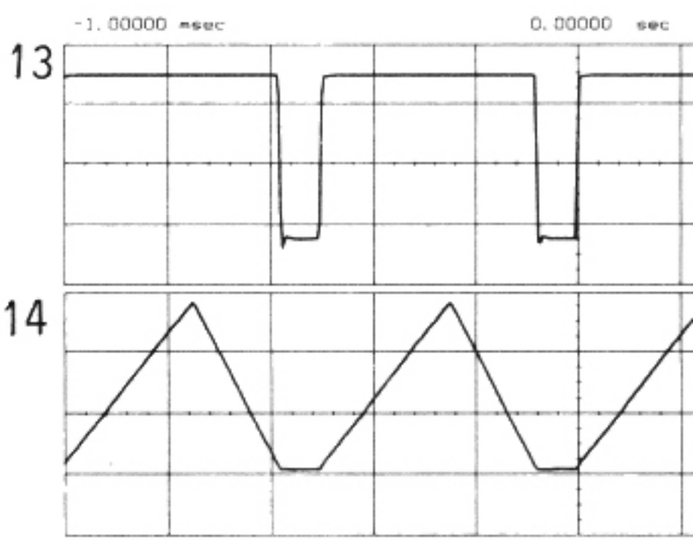
1. Press PRESET then select the following

   Track gen. on
   Zero span
   Ref. freq. 2 kHz

13
14

BOARD : AE6

TEST POINT : TR9 collector for Ch. 1
SCOPE SETTING [DEFAULT]

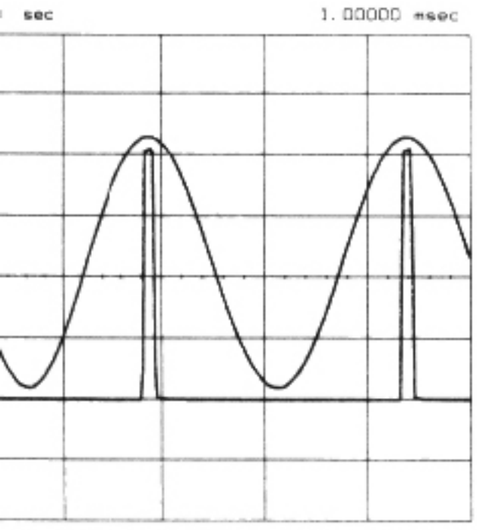


TEST POINT : TP7 (IC9d pin 14) for Ch. 2

PROCEDURE :

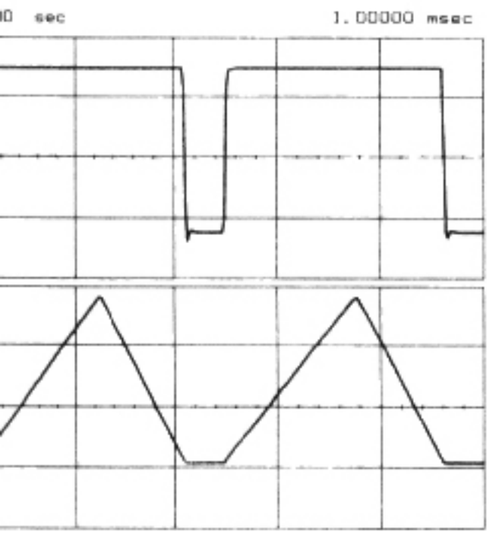
1. Press PRESET then select the following

   Track gen. on
   Zero span
   Ref. freq. 2 kHz



Offset - -1.200 volts
Offset - 0.000 volts
Delay - 0.00000 sec

owing 2382 settings:



Offset - 3.000 volts
Offset - 200.0 mvolts
Delay - 0.00000 sec

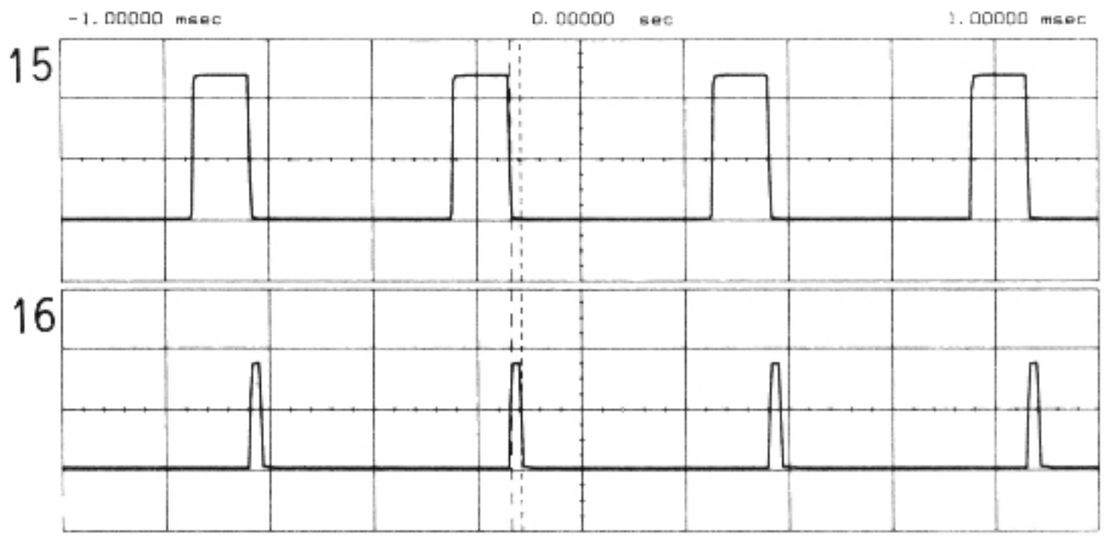
2

owing 2382 settings:

15
16

BOARD : AE6

TEST POINT : IC11c pin 10 for Ch. 1
SCOPE SETTING [DEFAULT]



Ch. 1 - 2.000 volts/div
Ch. 2 - 2.000 volts/div
Timebase - 200 usec/div
Delta T - 20.0000 usec
Start - -135.000 usec

Offset - 2.000 volts
Offset - 2.000 volts
Delay - 0.00000 sec
Stop - -115.000 usec

TEST POINT : IC10b pin 5 for Ch. 2

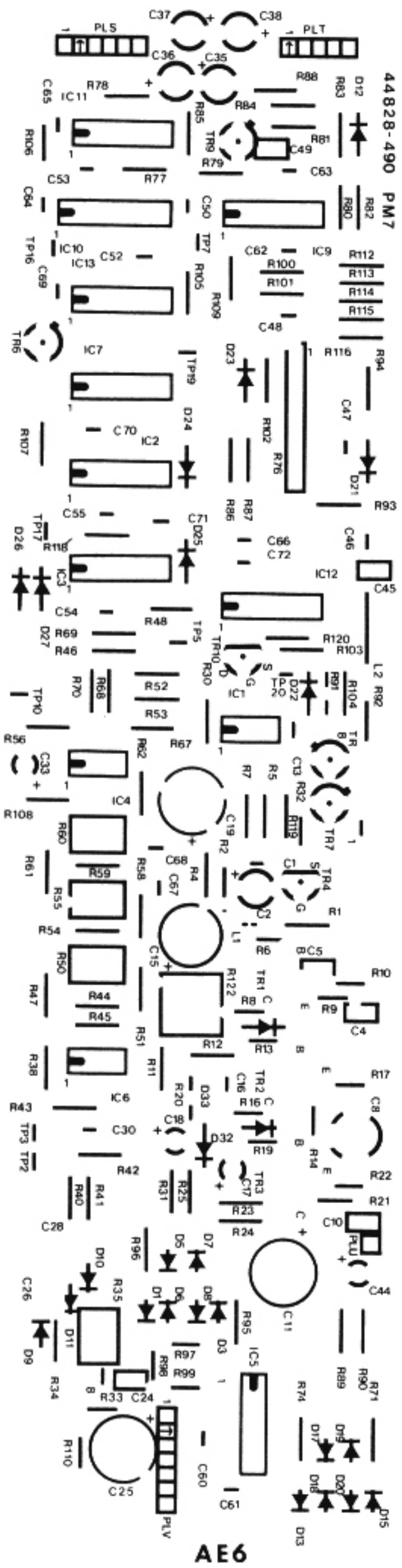
PROCEDURE :

1. Press PRESET then select the following 2382 settings:

   Track gen. on
   Zero span
   Ref. freq. 2 kHz

Fig. 45a

May 86



Component layouts for AE6 & AE7

Fig. 45

May 86

PART OF
AE6
44828-490G

FROM SHEET ONE

FREQUENCY CONSCIOUS SWITCH

SQUARER

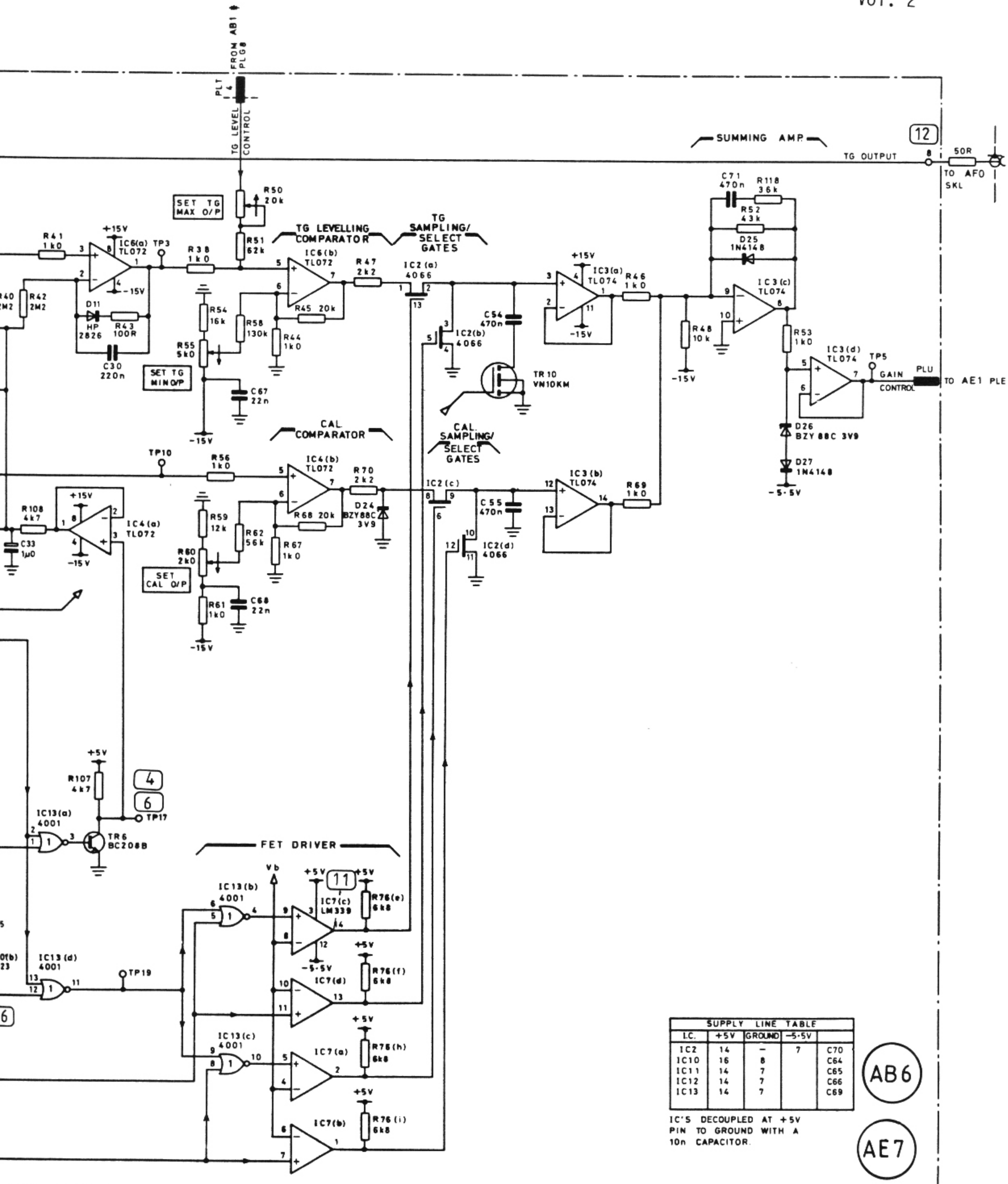
90° PHASE SHIFTER

FROM SHEET ONE

♦ SEE CIRCUIT AE0 FOR CONNECTION DETAILS.

Drg.No. Z44990-452
Sh.5 Iss.4

AE6 : Amp. leveller
AE7 : Switch



SUPPLY LINE TABLE				
I.C.	+5V	GROUND	−5·5V	
IC2	14	–	7	C70
IC10	16	8		C64
IC11	14	7		C65
IC12	14	7		C66
IC13	14	7		C69

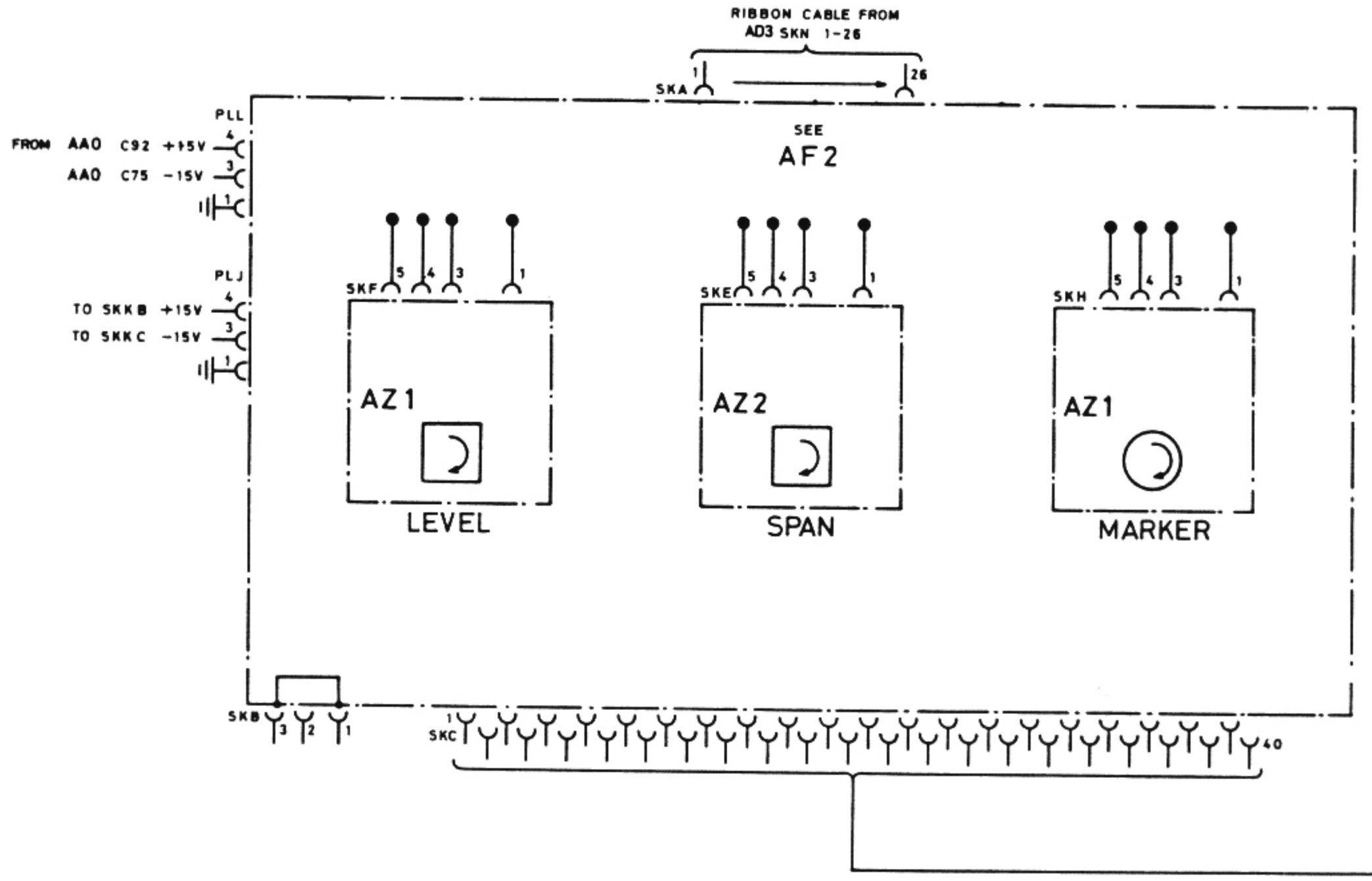
IC'S DECOUPLED AT +5V PIN TO GROUND WITH A 10n CAPACITOR.

AB6

AE7

FOR CONNECTION DETAILS.

Amp. leveller
Switch



BOARDS VIEWED FROM FRONT OF INSTRUMENT.

Drg.No. Z44990-468
Sh.1 Iss.1

AF0:AF front pane

AF0

PLP
3
2
1
FROM AAO C2 +5V

SEE
AF1

SA-SW
KEYBOARD
SWITCHES

40 CONNECTIONS BY RIBBON CABLE TO/FROM AF2 SKC

HENT.

FROM AEO PLAB
SKM

TRACKING
GEN.

FROM ADO SKAD
SKN

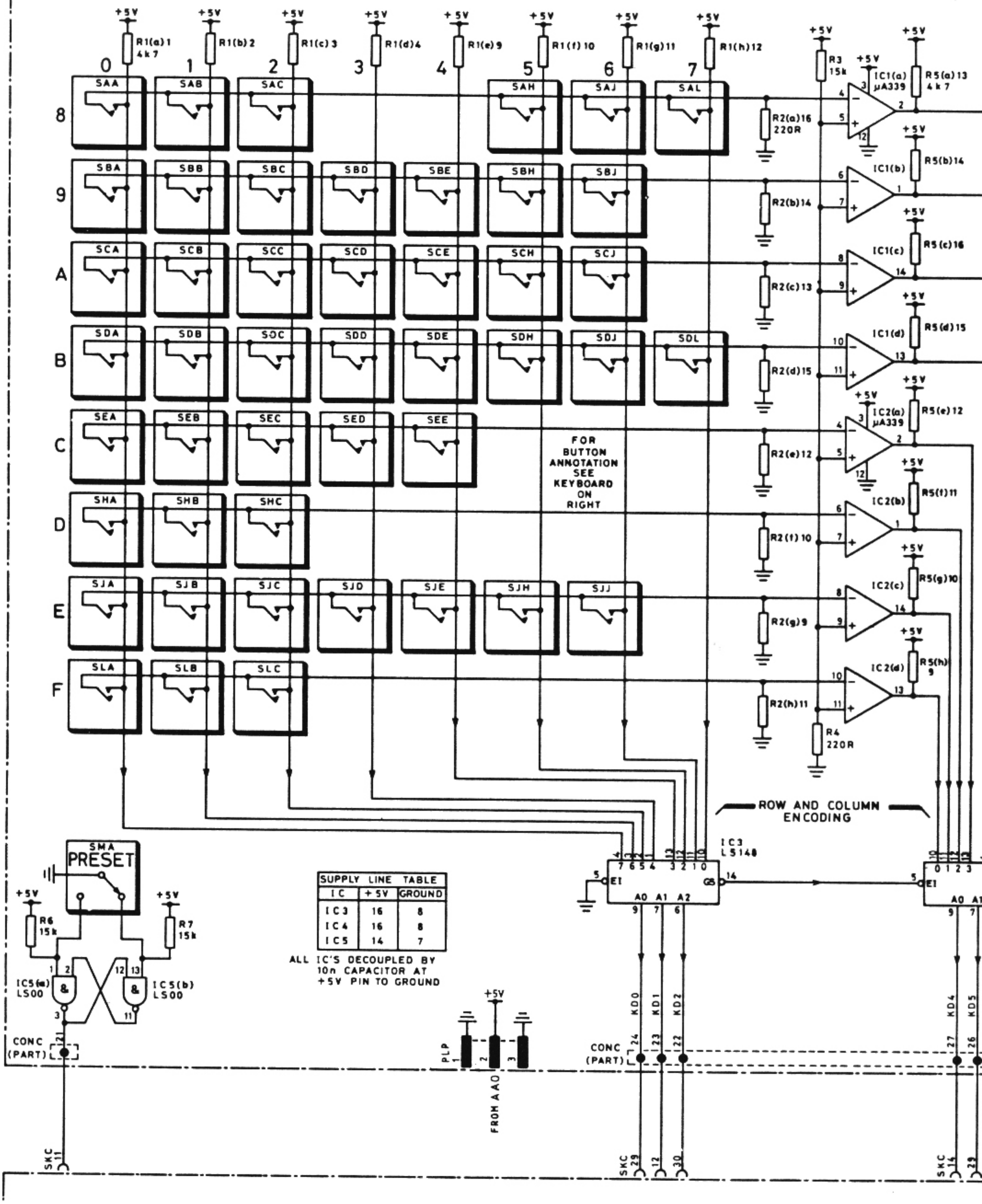
10 MHz
STD

AF0

AF front panel interconnection

SB7
SB6
SB5
SB4
SB3
SB2
SB1
SB0
SC9
SC8
SCC
SCD
SCE
SCF
SC1
SC2
SC3
SC4
SC5
SC6
SC7
SD9
SD8
SDC
SDD
SDE
SDF
SDH
SE7
SE8
SEC
SED
SEE
SEF
SEH
SF7
SF8
SFC
SFD
SFE
SFF
SFH
SG7
SG8
SGC
SGD
SGE
SGF
SGH
SH7
SH8
SHC
SHD
SHE
SHF
SHH
SI7
SI8
SIC
SID
SIE
SIF
SIH
SJ7
SJ8
SJC
SJD
SJE
SJF
SJH
SK7
SK8
SKC
SKD
SKE
SKF
SKH
SL7
SL8
SLC
SLD
SLE
SLF
SLH
SM7
SM8
SMC
SMD
SME
SMF
SMH
SN7
SN8
SNC
SND
SNE
SNF
SNH
SP7
SP8
SPC
SPD
SPE
SPF
SPH
SQ7
SQ8
SQC
SQD
SQE
SQF
SQH
SR7
SR8
SRC
SRD
SRE
SRF
SRH
SS7
SS8
SSC
SSD
SSE
SSF
SSH
ST7
ST8
STC
STD
STE
STF
STH
SU7
SU8
SUC
SUD
SUE
SUF
SUH
SV7
SV8
SVC
SVD
SVE
SVF
SVH
SW7
SW8
SWC
SWD
SWE
SWF
SWH
SX7
SX8
SXC
SXD
SXE
SXF
SXH
SY7
SY8
SYC
SYD
SYE
SYF
SYH
SZ7
SZ8
SZC
SZD
SZE
SZF
SZH
S17
S18
S1C
S1D
S1E
S1F
S1H
S27
S28
S2C
S2D
S2E
S2F
S2H
S37
S38
S3C
S3D
S3E
S3F
S3H
S47
S48
S4C
S4D
S4E
S4F
S4H
S57
S58
S5C
S5D
S5E
S5F
S5H
S67
S68
S6C
S6D
S6E
S6F
S6H
S77
S78
S7C
S7D
S7E
S7F
S7H
S87
S88
S8C
S8D
S8E
S8F
S8H
S97
S98
S9C
S9D
S9E
S9F
S9H
SA7
SA8
SAC
SAD
SAE
SAF
SAH
SB7
SB8
SBC
SBD
SBE
SBF
SBH
SC7
SC8
SCC
SCD
SCE
SCF
SCH
SD7

SWITCH MATRIX DETAILS

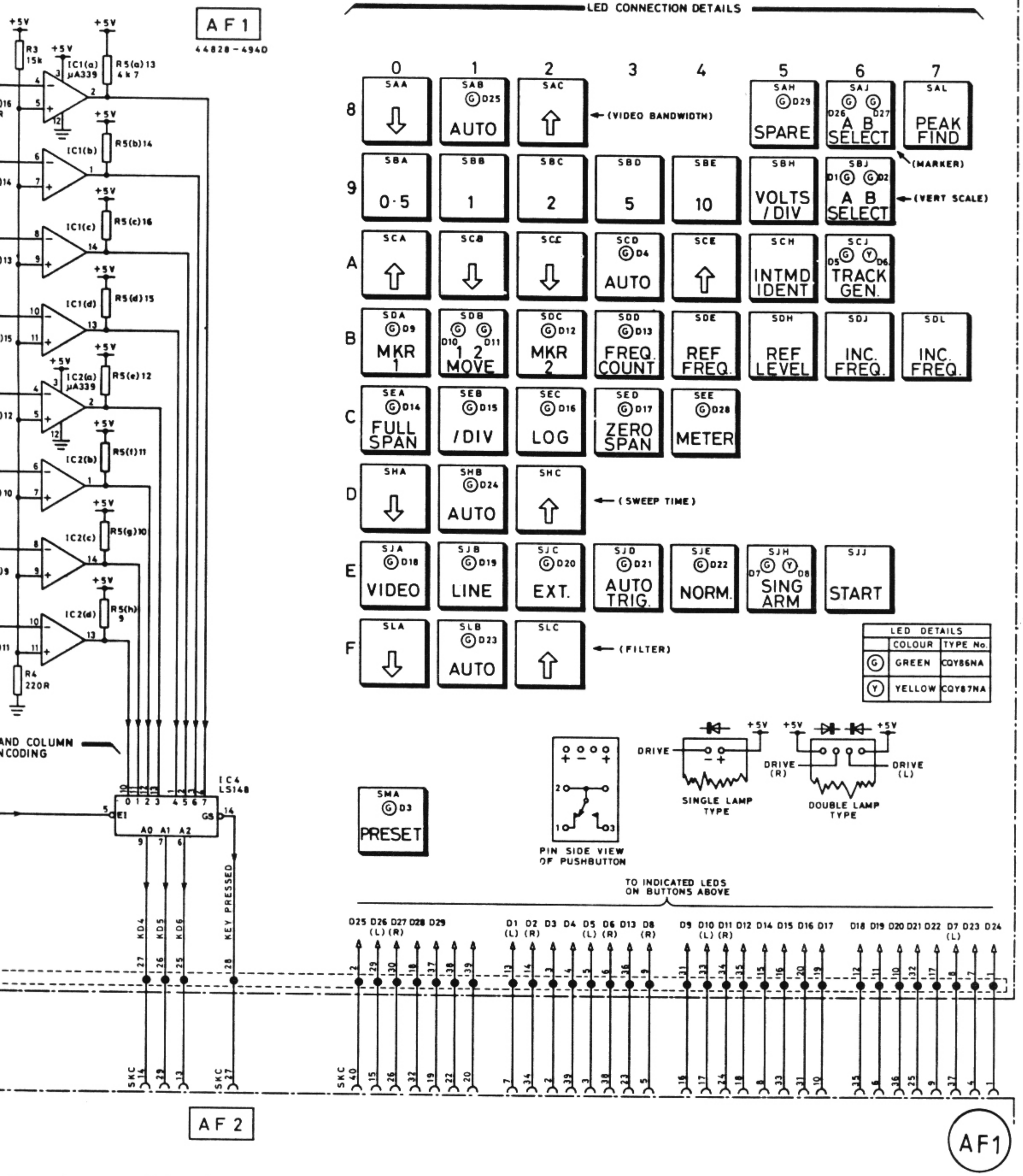


SUPPLY LINE TABLE		
IC	+5V	GROUND
IC3	16	8
IC4	16	8
IC5	14	7

ALL IC'S DECOUPLED BY 10n CAPACITOR AT +5V PIN TO GROUND

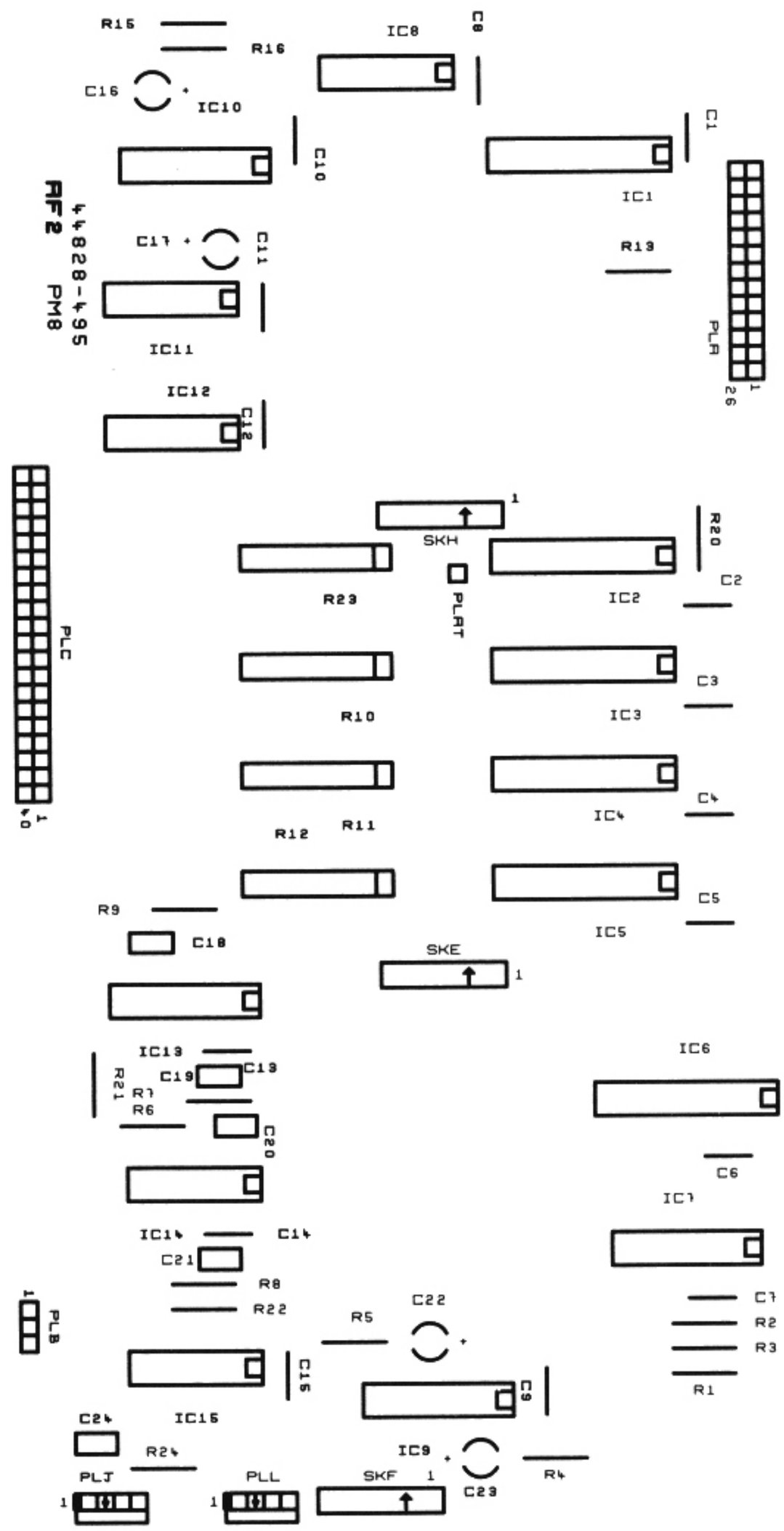
Drg.No. Z44828-494D
Sh.1 Iss.2

AF1:Front panel



Front panel keyboard

Fig. 47
Chap. 7
Page 103/104



Component layout for AF2

Fig. 48

May 86

AZ 2

SKE

FROM AA3a +15V

FROM AA10 -15V

PLL

PLA

FROM AD3 PLN

+5V

R1 15k

R2 15k

R3 15k

R13 15K

CS42(L)

SUPPLY LINE TABLE		
IC	+5V	GROUND
IC1	20	10
IC2	20	10
IC3	20	10
IC4	20	10
IC5	20	10
IC6	20	10
IC7	16	8
IC8	14	7
IC9	16	8
IC10	16	8
IC11	14	7
IC12	14	7
IC13	16	8
IC14	14	7
IC15	14	7

ALL IC'S DECOUPLED AT +5V PIN TO GROUND BY 10n CAPACITOR

AZ 1

SKH

IC14(b) LS86

R21 560R

EDGE DOUBLER

AZ 1

SKF

IC14(a) LS86

R6 360R

C20 2n2

IC14(c) LS86

R22 560R

EDGE DOUBLER

IC14(d) LS86

R8 360R

C21 2n2

R20 2k2

PLAT

Drg.No. Z44828-495T
Sh.1 Iss.1

AF2:Front pa

FROM AD3 PLN 7

PLA 7

CS42(L)

PART OF
AF 2
44828-495T

R3
15k

+5V

IC7
LS348

IC6
LS244

QUIET DATA BUS

D0

D7

HZ/DIV DEBOUNCE CIRCUITRY

MAKE DEBOUNCE MONO

MAKE DEBOUNCE MONO

R4
6k8

C23
100n

IC9 (a)
LS221

R5
33k

C22
100n

IC9 (b)
LS221

IC15(a)
LS74

IC15(b)
LS74

HZ / DIV

INITIALIZE DEBOUNCE CIRCUITRY (L)

CS42 (L)

DIRECTION DETECTION

IC14 (b)
LS86

IC11 (c)
LS00

IC12 (c)
LS00

IC11 (b)
LS00

MARKER DOWN

MARKER UP

R21
560R

R7
10k

EDGE DOUBLER

C19
220p

IC13(a)
LS123

IC14(a)
LS86

R6
360R

C20
2n2

IC14(c)
LS86

IC11(d)
LS00

REF DOWN

REF UP

R22
560R

R9
10k

IC12(d)
LS00

IC11(a)
LS00

EDGE DOUBLER

C18
220p

IC13(b)
LS123

IC14(d)
LS86

R8
360R

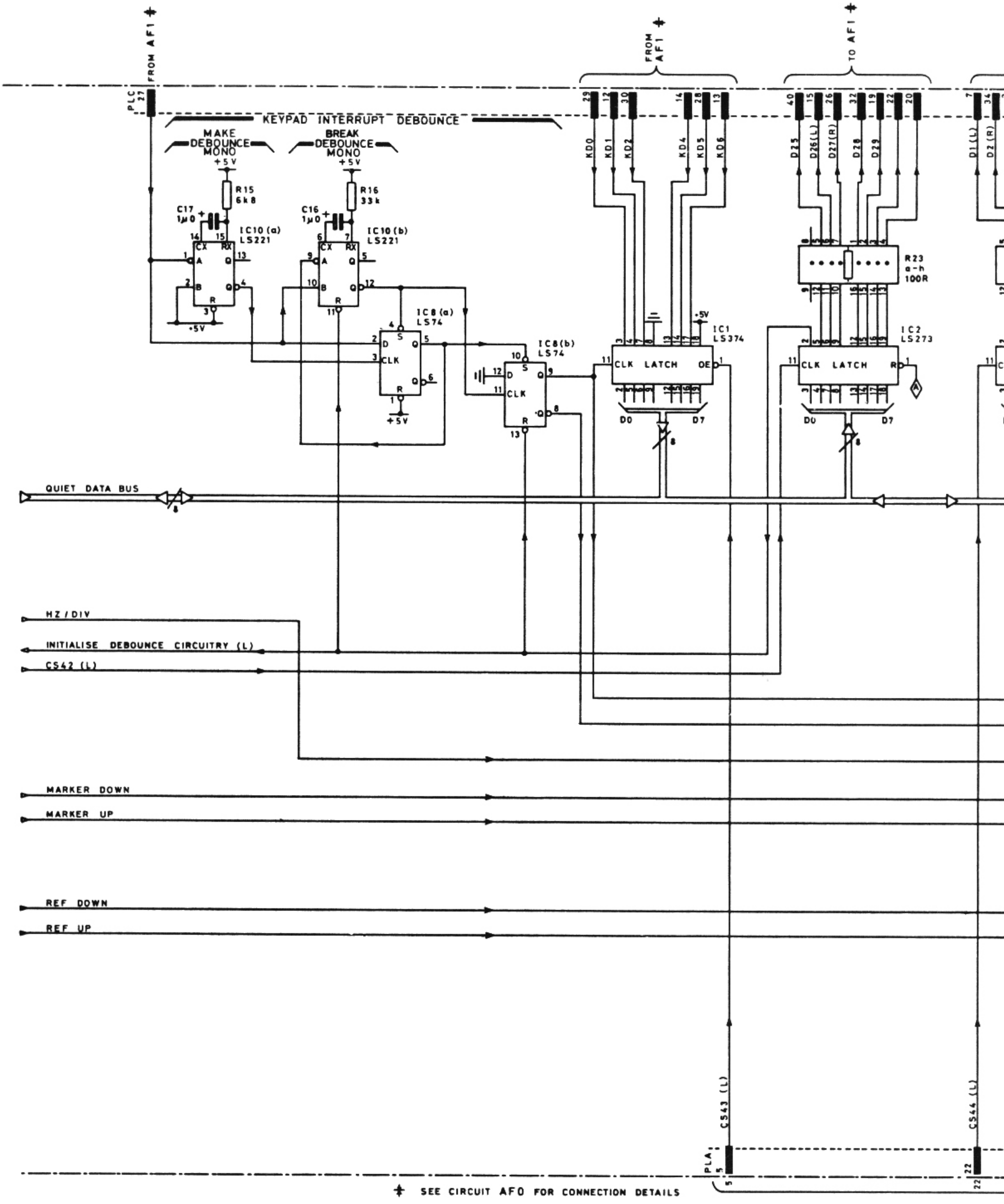
C21
2n2

LINE TABLE	
+5V	GROUND
20	10
20	10
20	10
20	10
20	10
20	10
16	8
14	7
16	8
16	8
14	7
14	7
16	8
14	7
14	7

DECOUPLED
IN TO GROUND
APACITOR

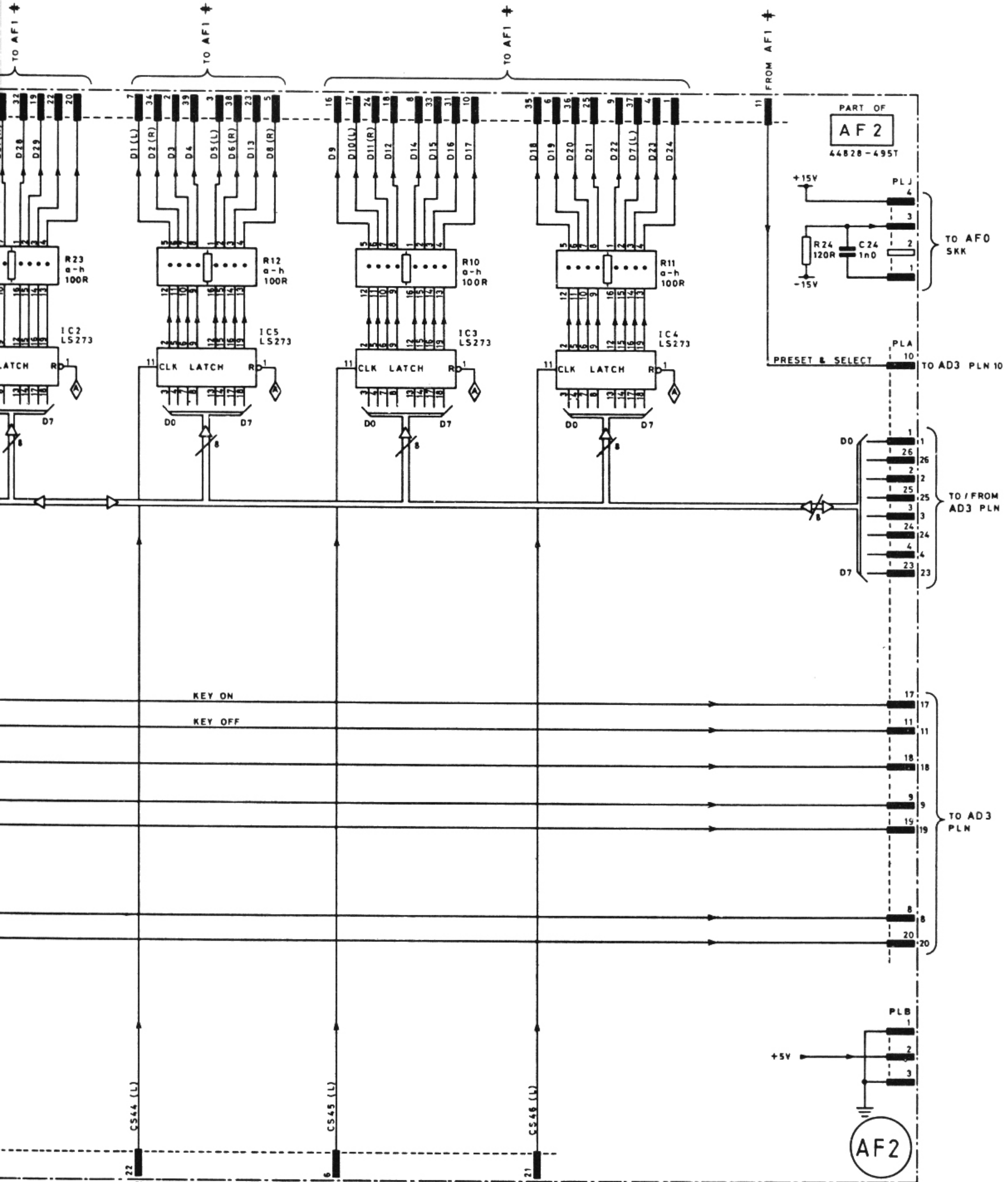
AF2

AF2: Front panel logic

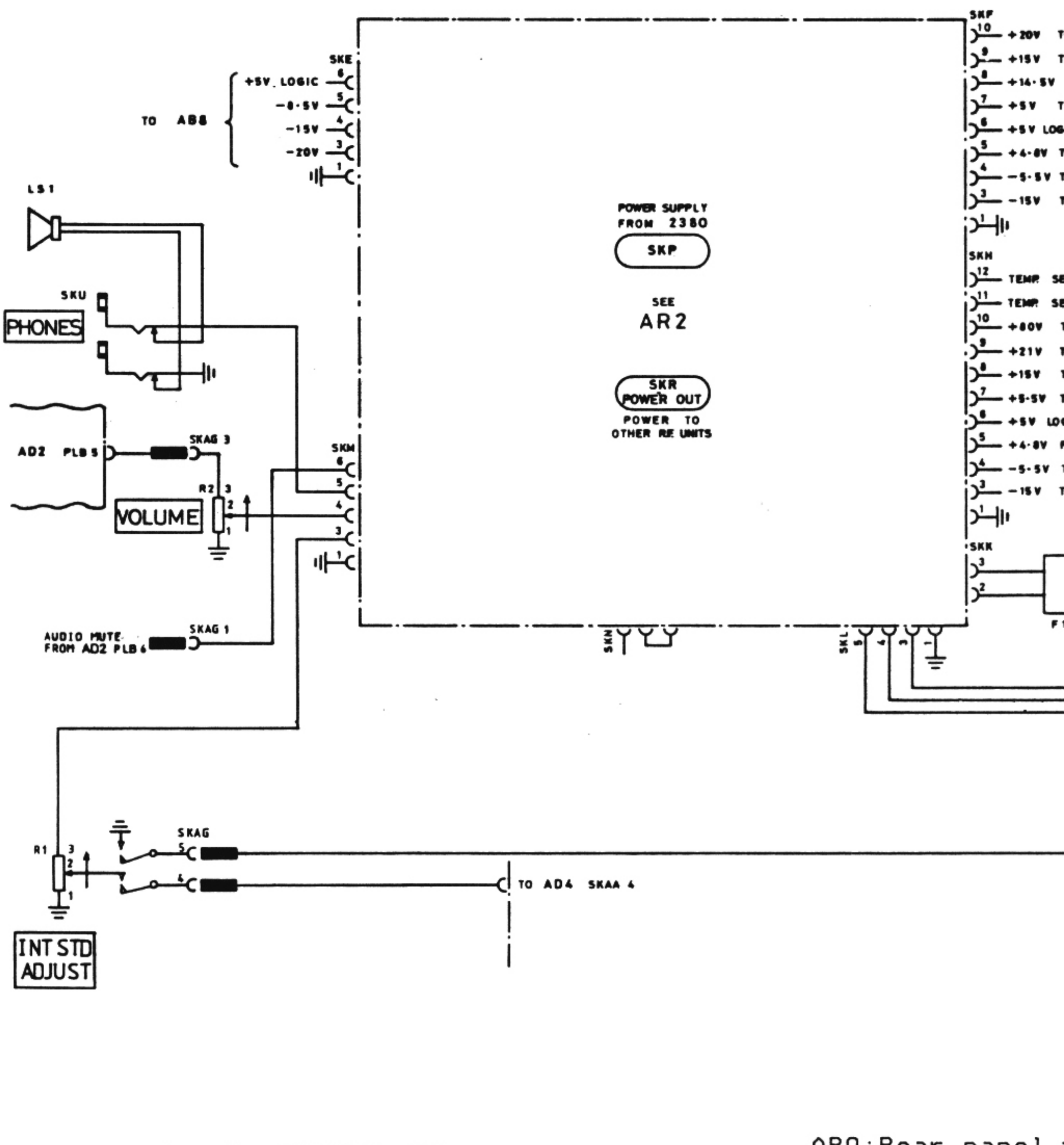


Drg.No. Z44828-495T
Sh.2 Iss.2

AF2:Front panel logic



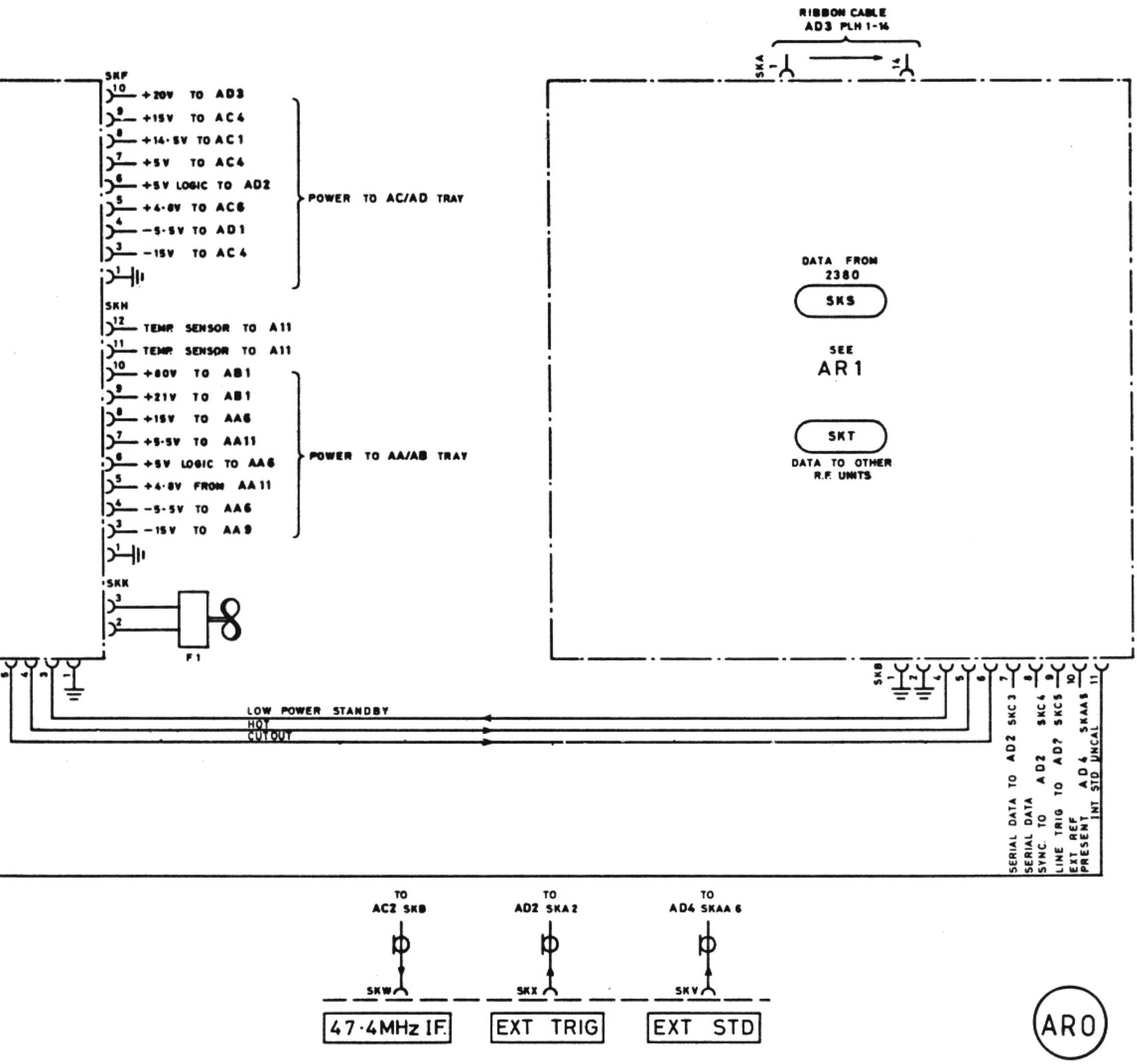
t panel logic



Drg.No. Z44990-469
Sh.1 Iss.1

AR0:Rear panel

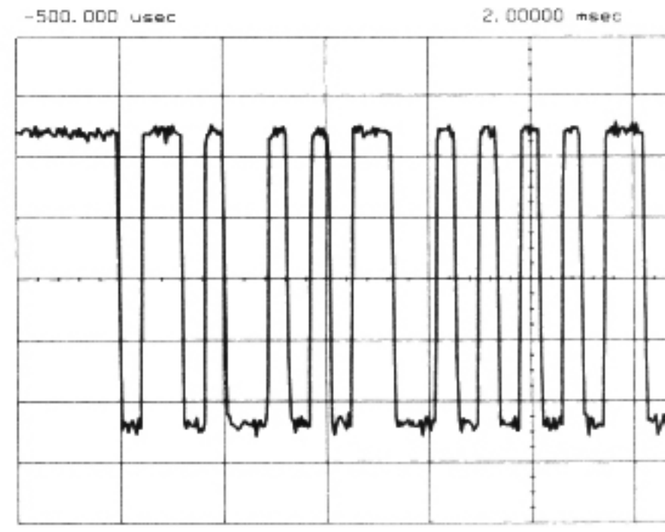
AR0



0:Rear panel interconnections

1 BOARD : AR1

TEST POINT : SKT7 & 8
SCOPE SETTING [DEFAULT]



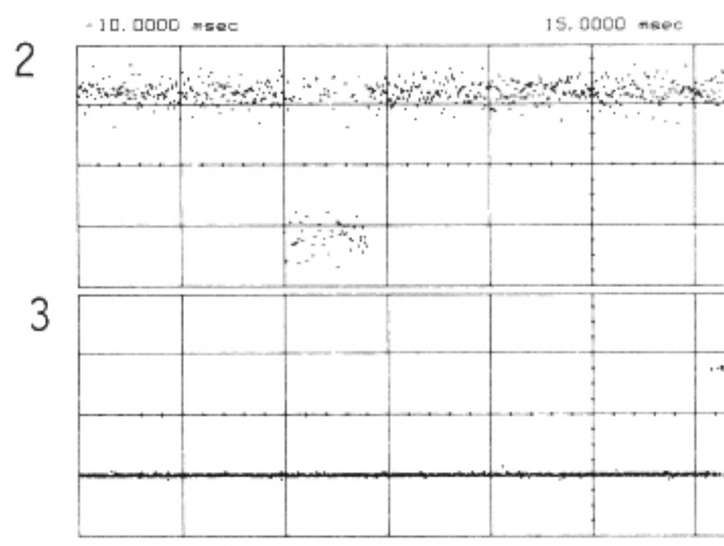
Ch. 1 = 200.0 mvolts/div
Timebase = 500 usec/div

PROCEDURE :

1. Press PRESET.

2
3 BOARD : AR1

TEST POINT : SKT7 & 8
SCOPE SETTING [DEFAULT]

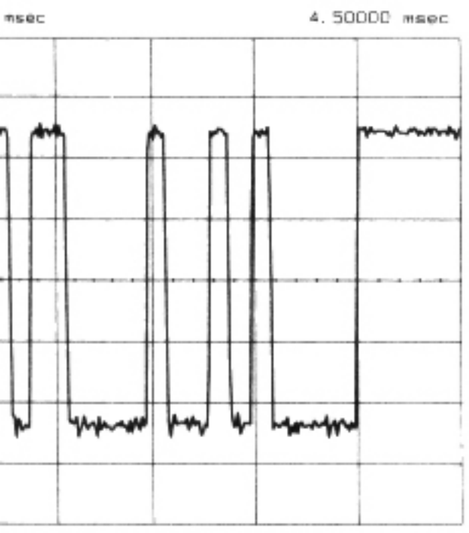


Ch. 1 = 400.0 mvolts/div
Ch. 2 = 10.00 volts/div
Timebase = 5.00 msec/div

TEST POINT : SKT 9 & 10

PROCEDURE :

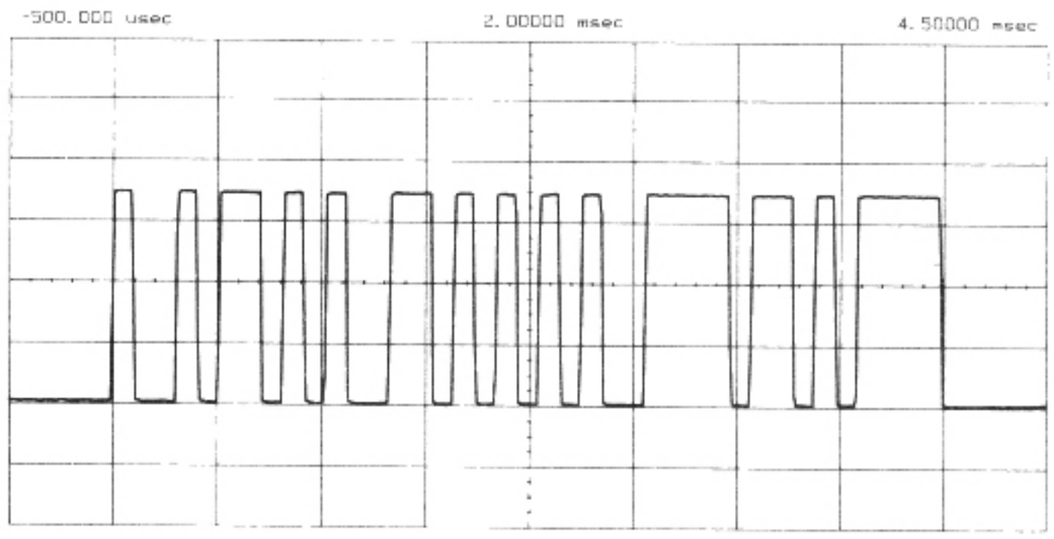
1. Press PRESET.



Offset = 600.0 mvolts
Delay = 2.00000 msec

4 BOARD : AR1

TEST POINT : SKT 9 & 10
SCOPE SETTING [DEFAULT]

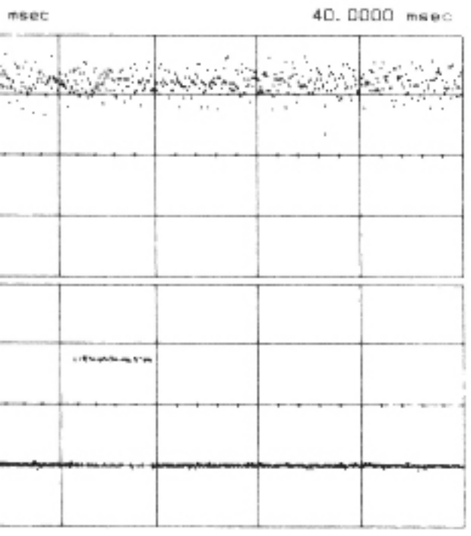


Ch. 1 = 5.000 volts/div
Timebase = 500 usec/div

Offset = 10.00 volts
Delay = 2.00000 msec

PROCEDURE :

1. Press PRESET.

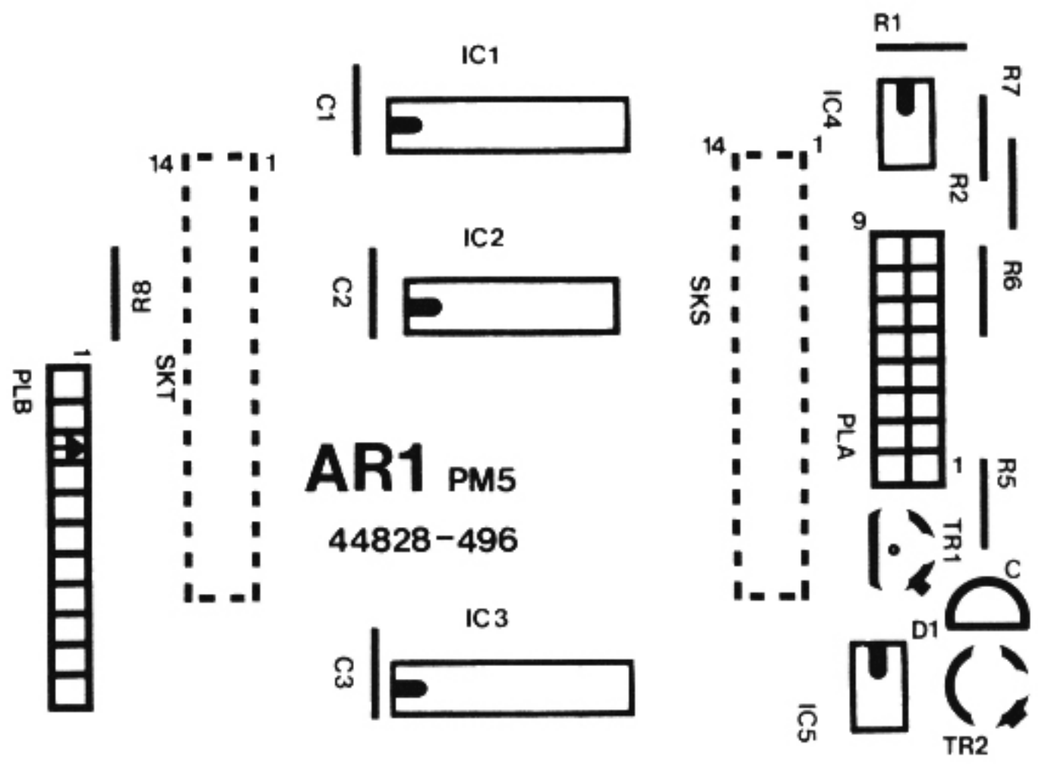


Offset = 600.0 mvolts
Offset = 10.00 volts
Delay = 15.0000 msec

Waveforms for AR1

Fig. 51a

May 86



Component layout for AR1

Fig. 51

May 86

AR1

44828-496P

‡ DATA FROM 2380

SKS

UNIT ADDRESS INCREMENTER

IC1 LS283

A1 A2 A3 A4 B1 B2 B3 B4 Σ1 Σ2 Σ3 Σ4

+5V

IC3(a) LS08

R8 4K7

UNIT ADDRESS LINE 0

UNIT ADDRESS LINE 1

UNIT ADDRESS LINE 2

5MHz

SERIAL DATA SYNC.

SERIAL DATA

EXT. STD. (L)

TRANSMIT CURRENT LOOP

RECEIVE CURRENT LOOP

EXT. STD. (L)

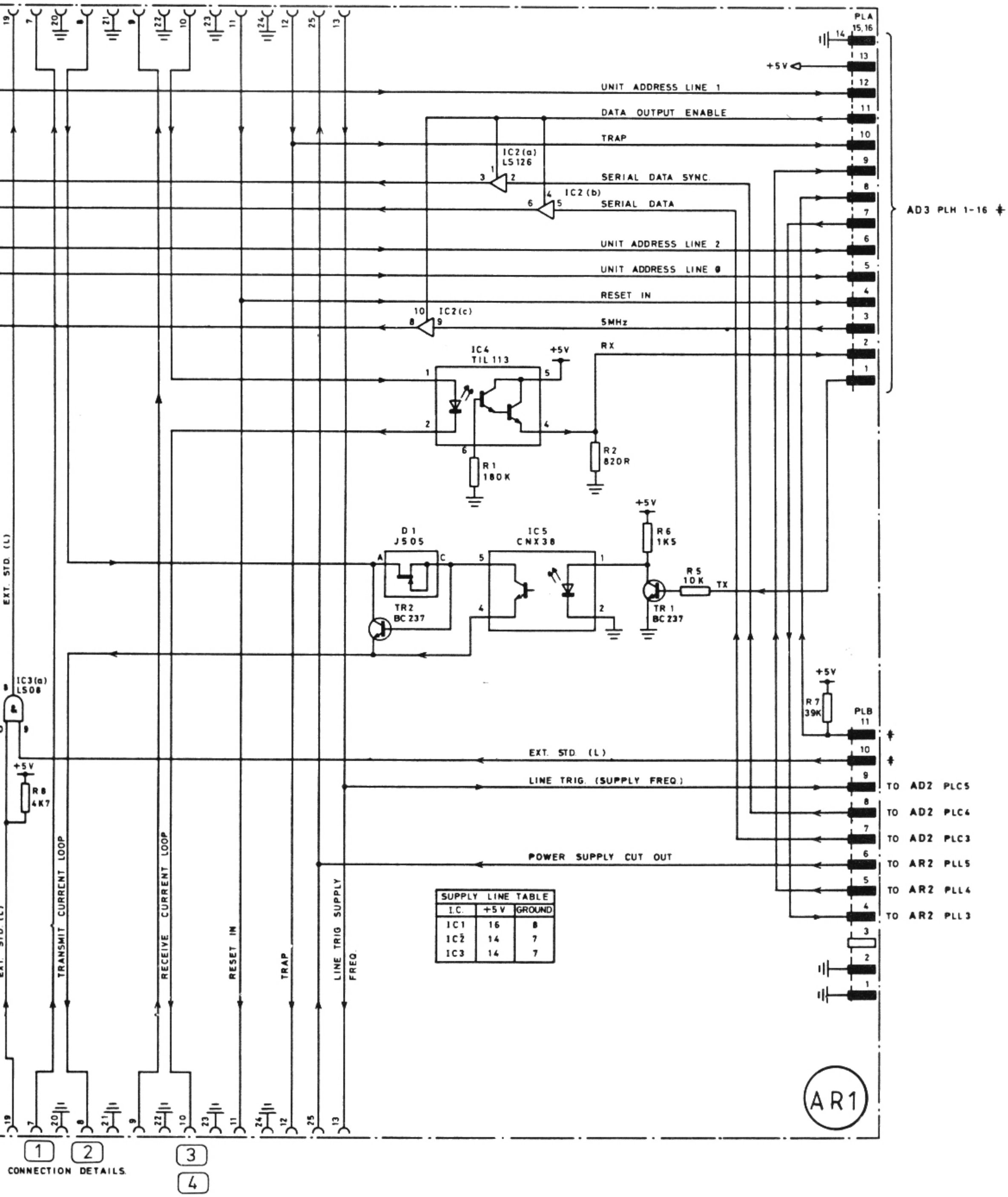
SKT

‡ DATA TO OTHER RF UNITS.

‡ SEE CIRCUIT AR0 FOR CONNECTION DETAILS.

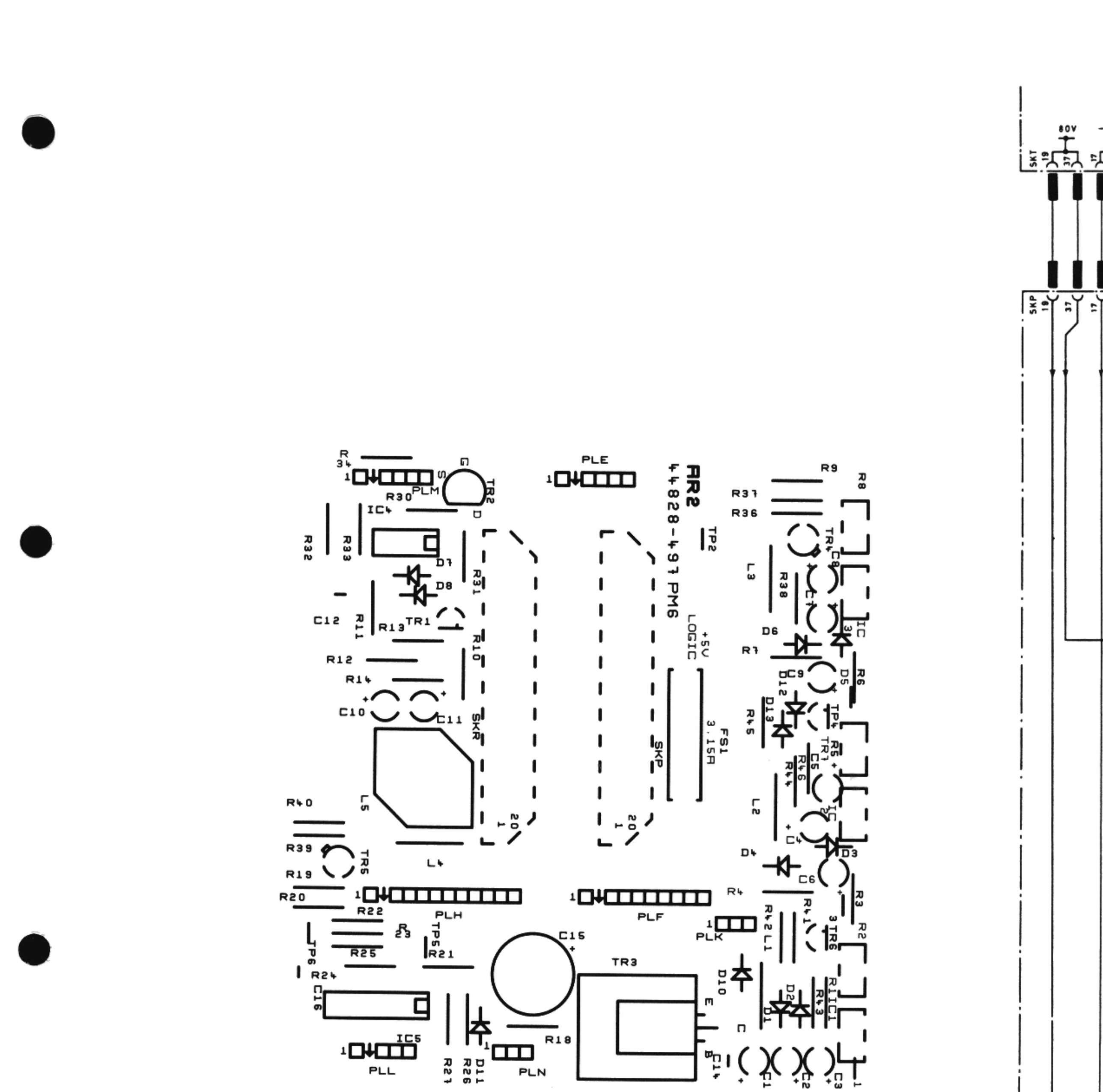
Drg. No. Z44828-496P
Sh. 1 Iss. 1

AR1 : Signal in



SUPPLY LINE TABLE		
I.C.	+5 V	GROUND
IC1	16	8
IC2	14	7
IC3	14	7

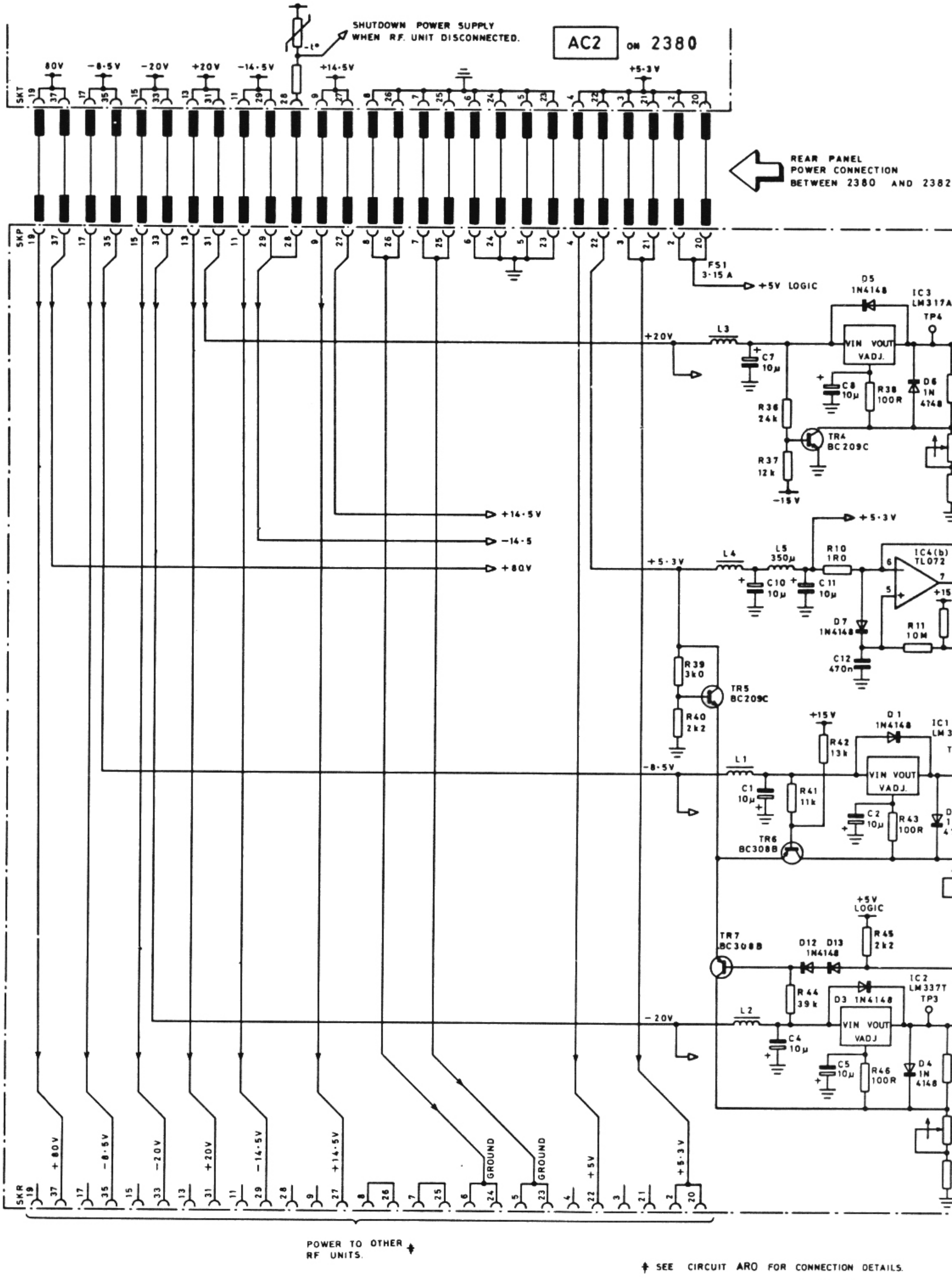
AR1 : Signal interface board



Component layout for AR2

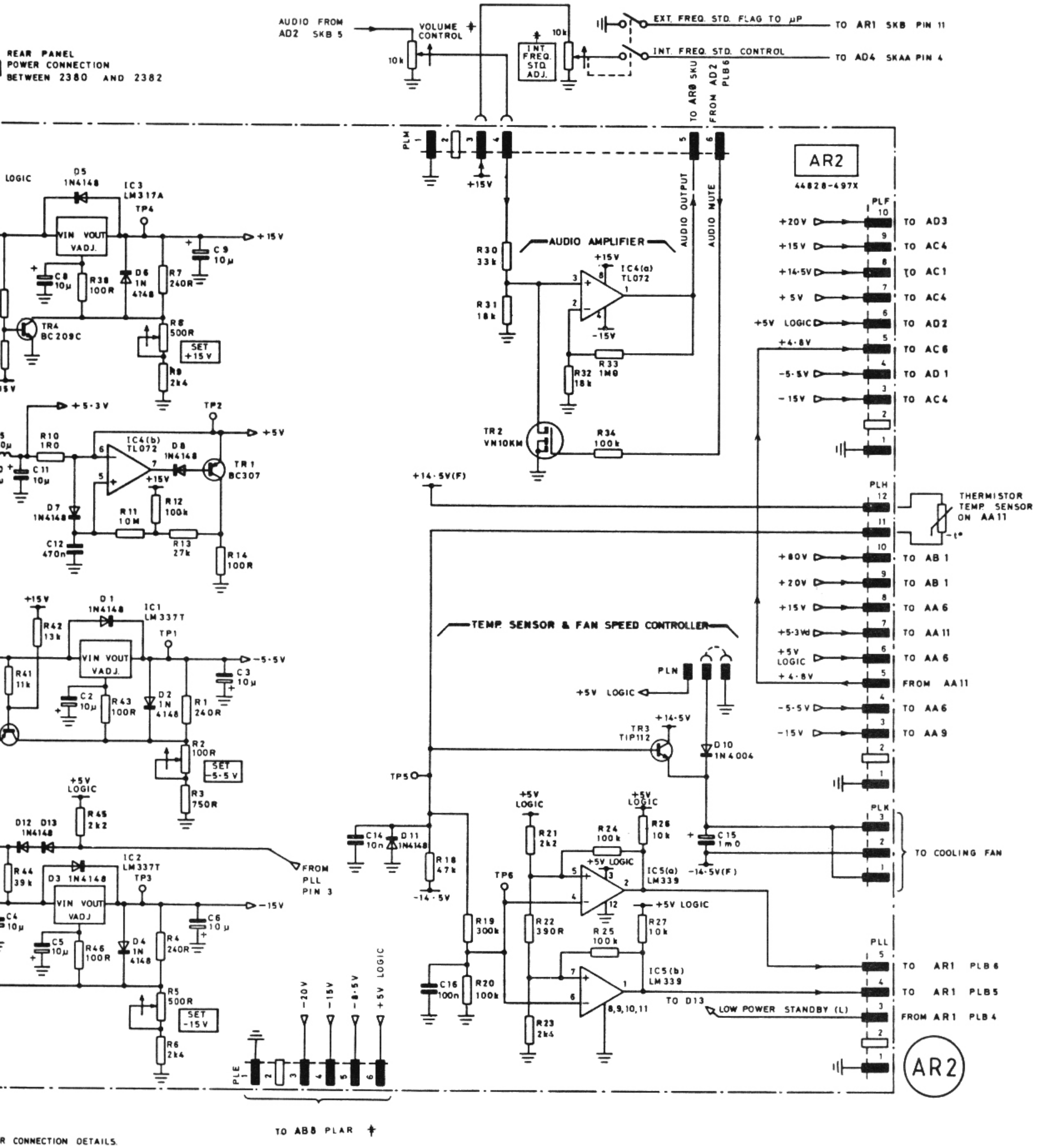
Fig. 52

May 86



Drg. No. Z44828-497X
Sh. 1 Iss. 3

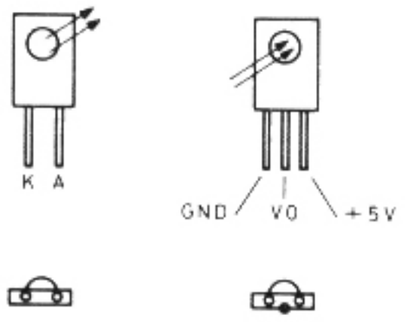
AR2: Power su

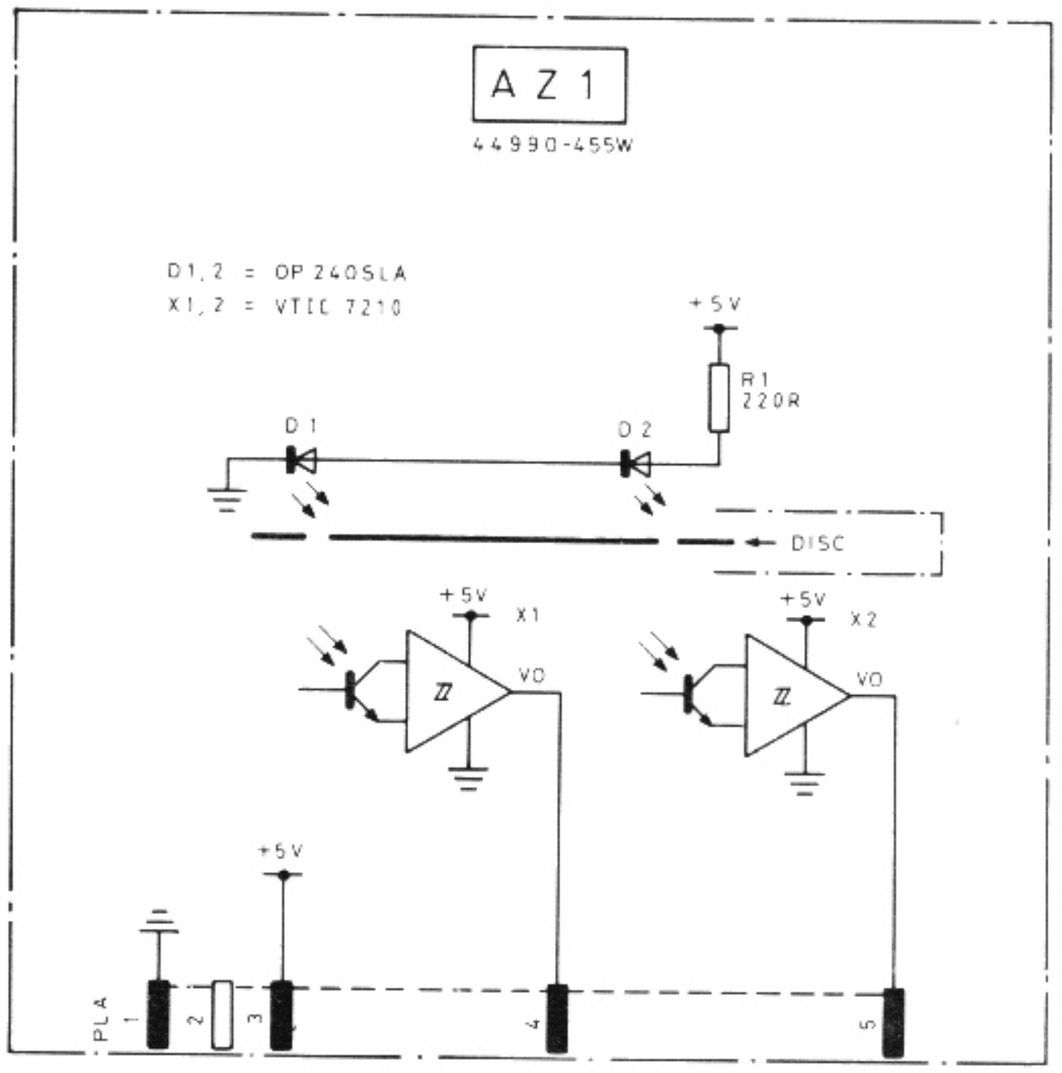


R CONNECTION DETAILS

AR2: Power supply interface

Fig. 52
Chap. 7
Page 113/114

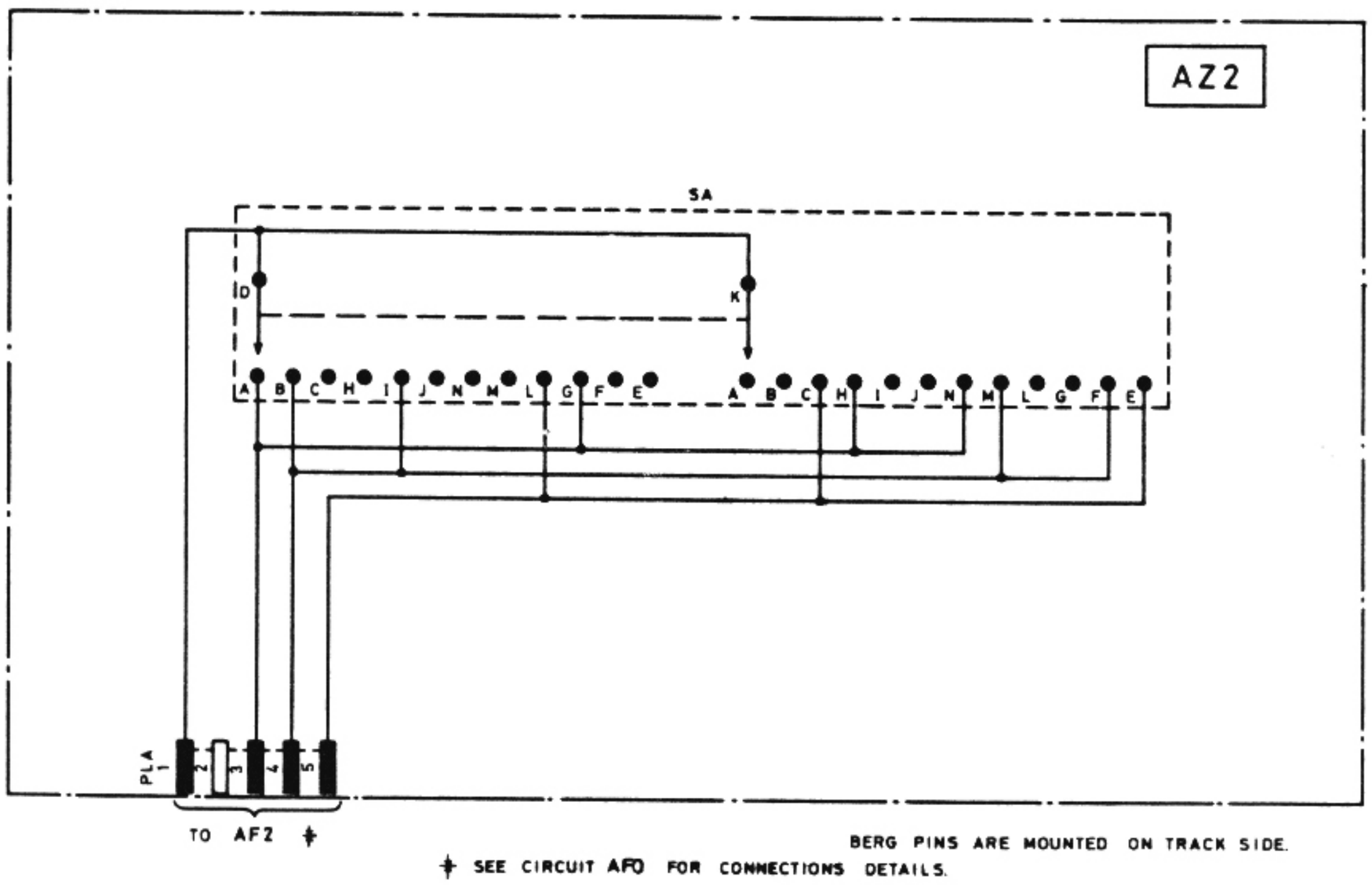




Drg.No. Z44990-455W
Sh.1 Iss.3

AZ1

AZ1 : Optical encoder



Drg. No. Z44828-498M
Sh. 1 Iss. 1

AZ2: Span switch board

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